6-16-2006

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Publication Info

Published in *Applied Physics Letters*, Volume 82, Issue 25, 2006, pages 4593-4595.

Chen, C. Q., Zhang, J. P., Adivarahan, V., Koudymov, A., Fatima, H., Simin, G., Yang, J., & Khan, M. A. (16 June 2003). AlGaN/GaN/AlGaN Double Heterostructure for High-Power III-N Field-Effect Transistors. Applied Physics Letters, 82 (25), 4593-4595.
http://dx.doi.org/10.1063/1.1587274

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Citation: Applied Physics Letters **82**, 4593 (2003); doi: 10.1063/1.1587274
View online: http://dx.doi.org/10.1063/1.1587274
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/82/25?ver=pdfcov
Published by the AIP Publishing

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(Received 10 February 2003; accepted 28 April 2003)

We propose and demonstrate an AlGaN/GaN/AlGaN double heterostructure (DH) with significantly improved two-dimensional (2D) confinement for high-power III-N heterostructure field-effect transistors (HFETs). The DH was grown directly on an AlN buffer over *i*-SiC substrate. It enables an excellent confinement of the 2D gas and also does not suffer from the parasitic channel formation as experienced in past designs grown over GaN buffer layers. Elimination of the GaN buffer modifies the strain distribution in the DH, enabling Al contents in the barrier region well over 30%. For the AlGaN/GaN/AlGaN DH design, the 2D electron gas mobility achieved was 1150 $cm^2/V\,s$ at room temperature and 3400 $cm^2/V\,s$ at 77 K, whereas the temperature independent sheet carrier density was $N_S \approx 1.1\times10^{13}$ cm^{-2}. Compared to a regular AlGaN/GaN structure, the channel mobility-concentration profiling shows significant improvement in the carrier confinement. Sample DHFETs with 1-μm long gates demonstrate the threshold voltage of 3.5 V, with a peak saturation current of 0.6–0.8 A/mm. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1587274]

Channel carrier confinement is key to achieving high-power performance of nitride-based heterostructure field-effect transistors (HEFTs). Due to extremely high sheet electron densities in III-N heterostructures, the electron spillover at high drain/gate voltages limit the achievable peak currents and rf power densities. This effect contributes significantly to rf current collapse due to trapping of the electrons spilling over the two-dimensional (2D) channel into barrier and buffer layers. We have proposed and demonstrated an AlGaN/InGaN/GaN double-heterostructure transistor (DHFET), where the electron confinement was significantly improved due to enhanced potential barriers at the AlGaN/InGaN and InGaN/GaN heterointerfaces.[1] Current collapse-free performance of the DHFET was demonstrated with the output rf powers of 6–7 W/mm.

It is of significant scientific and practical interest to extend the DHFET approach toward GaN confinement layer double heterostructure. The electron mobility in the GaN is usually higher than that in the InGaN channel. Due to a significant difference in the growth temperatures, In incorporation in the InGaN channel of the DHFET poses certain limitations on the DHFET structure parameters: (1) a maximum achievable In concentration in the channel, (2) composition uniformity, and (3) 2D carrier mobility. GaN-channel DHFET would provide further information on the polarization charges and band-gap offsets in the III-N heterostructures.

In this letter, we now propose and demonstrate a double-heterostructure design for high-power III-N HFETs. The heterostructure consists of high-quality AlGaN (15% Al) buffer layer grown directly on the AlN buffer over *i*-SiC substrate. This is followed by a thin GaN channel layer capped with the AlGaN (30% Al) barrier layer. The double heterostructures consisting of a GaN layer sandwiched between the two AlGaN layers were discussed earlier.[2,3] However, all previously proposed structures suffered from parasitic channel formation at the bottom AlGaN barrier/GaN buffer interface. The use of the thick GaN buffer layer comes from the need to achieve reasonably low defect concentration and surface morphology; otherwise, there is significant degradation. Recently, we demonstrated an approach to grow very high-quality high-Al-content layers using pulsed atomic layer epitaxy[4] and strain control techniques.[5,6] Due to unique low-defect-density AlGaN/AlN buffer, our design does not utilize the GaN buffer layer, thus eliminating the formation of the parasitic conducting channel. The absence of the GaN buffer also reduces and modifies the strain in subsequent AlGaN layers (changing it from tensile to compressive). This change, on the one hand, allows for higher Al fraction in the barrier layers, and on the other, results in a lesser depletion of the GaN channel from the underlying AlGaN layer. The AlGaN compositions for the bottom and top barriers have been optimized to achieve strong electron confinement, a sufficient sheet density of the 2D electron gas, and to suppress the formation of a hole accumulation layer at the lower GaN/AlGaN interface.

The results of one-dimensional simulations of the metal-AlGaN/GaN/AlGaN double heterostructure are shown in Fig. 1. The Schottky barrier height was taken as 0.8 eV. In this figure, we compare the band diagrams and electron distributions in a regular AlGaN/GaN HFET with several different DHFET structures. In all the cases, the Al composition in the top barrier layer is 30%. For the DHFETs, bottom AlGaN barrier is assumed to be coherently grown over the AlN buffer. All the AlGaN and GaN layers are assumed to have a Ga face, which is the case for a metalorganic chemical vapor deposition (MOCVD)-grown material. Correspondingly, we have chosen the spontaneous and piezopolarization charges at the interfaces.[7] Different curves show the effect of Al composition in the bottom barrier layer. All the layers are taken undoped, except for the case showing the effect of channel and bottom barrier doping marked with

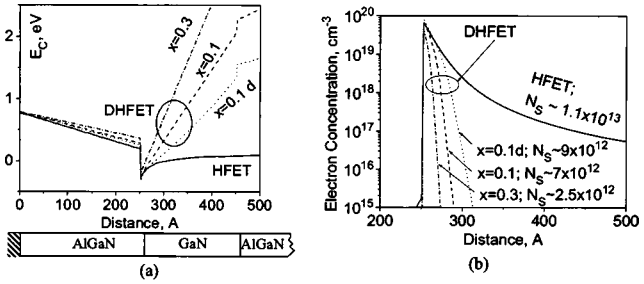

FIG. 1. Electron concentration profiles (a) and conduction band diagrams (b) for the proposed AlGaN/GaN/AlGaN double heterostructure. The Al fraction in the top barrier is 30%. The Al fraction in the bottom barrier is indicated as "*x*." The curves labeled as "*d*" correspond to the GaN channel and the bottom barrier doping of $N_D = 10^{18}$ cm^{-3}.

"*d*." At high Al fraction (30% Al) in the bottom barrier, the depletion due to negative polarization charges at the bottom barrier/GaN channel interface significantly decreases the sheet electron density down to $\sim 2.5\times 10^{12}$ cm^{-2}. The bottom barrier with 15% Al results in an optimum structure with the polarization-induced electron density of $\sim 7\times 10^{12}$ cm^{-2}. Note that the major difference in the total electron density of DHFET and regular HFET structures comes from the electrons spread over the GaN buffer. These electrons contribute little to device peak current, but may be responsible for the current collapse due to trapping in the GaN. As seen from the band diagrams of the Fig. 1(a), the conduction band edge of the AlGaN layer (15% Al) at the lower AlGaN/GaN interface is about 2.3 eV above the Fermi level. Since the band gap of the lower AlGaN layer is around 3.8 eV, it follows that the valence band edge is well below the Fermi level. and hence, there is no hole accumulation layer formation at this interface.

The sheet density in the DHFET can be further increased by the doping of the bottom barrier and GaN channel, which does not deteriorate the electron confinement in the DHFET structure. Due to a strong built-in electric field, all the electrons emitted by the donors are swept out toward the bottom of the quantum well. The electron distributions and the band diagrams corresponding to DHFET structure with GaN channel and bottom AlGaN barrier doped to $N_D = 10^{18}$ cm^{-3} are also shown in Fig. 1 (the curves labeled as "*d*"). While this letter was under preparation, the possibility of increasing the sheet electron density by doping the bottom AlGaN layer, regardless of the electron confinement in the DHFET structures, was also discussed.[8]

The epilayers for the proposed DHFET structure were grown on the (0001)-oriented semi-insulating 4H-SiC by using low-pressure MOCVD at 76 Torr. The substrates were annealed at 1100 °C for 5 min prior to growth. The growth temperatures for the top $Al_{0.3}Ga_{0.7}N$ cap layer (250 Å thick), 200-Å-thick GaN layer, $Al_{0.15}Ga_{0.85}N$ bottom barrier and 0.2-μm-thick AlN buffer were 1000, 1000, 1050, and 1100 °C, respectively. Reactant species used were triethylgallium, trimethylaluminum, and NH_3 with H_2 as the carrier gas. The sample shows a very smooth surface with a rms roughness around 0.31 nm from atomic force microscopy (AFM) measurements for a 2-μm$\times$2-μm scan area. The thickness of the bottom AlGaN layer was found to be a critical parameter determining the defect concentration in the structure, and correspondingly, in the 2D gas mobility. For the optimal thickness of the bottom barrier of about 0.3 μm, the measured Hall mobility and sheet carrier concentration were 1180 cm^2/V s and 1.1×10^{13} cm^{-2} at room temperature. At 77 K, the electron mobility increased up to 3500 cm^2/V s, while the sheet electron density remained constant. The sheet carrier density in the experimental structures is about 15% higher than found from the simulations. This difference may come from unintentional doping of the barrier/channel layers or from some uncertainty in the polarization/elastic constants used in our simulations. Prior to characterization, the samples were cleaned using diluted HF (HF:H_2O) to remove the native gallium oxide surface layer.

In regular HFET structures, the quantum-well profile that confines the 2D electrons depends on the carrier sheet density in the channel. Large variations of the sheet density result in electron spillover. Unlike the HFETs, in the DHFET structure the quantum well is determined mainly by the polarization charges, making the potential profile more stable. The electron confinement remains strong in a large range of gate/drain bias or pumping currents. In order to characterize the degree of electron confinement, we compared the mobility–concentration dependencies in the DHFET and conventional AlGaN/GaN HFET structures using the approach described before[9] for MOSHFET devices. The channel resistance $R_{\rm ch}$ and the gate capacitance C were measured as a function of gate–source bias on large-area transistors with the gate length of 60 μm, source–gate and gate–drain spacing of 10 μm, and gate width of 200 μm. The channel resistance measurements were carried out at a small drain bias of 0.1 V. The gate capacitance was measured at 1 MHz.

The thickness of the double-heterostructure barrier layers extracted from the capacitance measurements was 25 nm, a good corresponding to the estimated value from the growth parameters. The sheet concentration n_s can be found as a function of the gate voltage V_g, from measured gate capacitance per unit area C:

$$n_s = \frac{1}{q}\int_{V_{g1}}^{V_g} C dV_g, \tag{1}$$

where V_{g1} is the gate voltage taken well below the threshold voltage V_T. Since at $V_g < V_T$, the gate capacitance is very small, the exact value of V_{g1} does not significantly affect the dependence $n_s(V_g)$ given by the Eq. (1).

The electron mobility μ_n in the 2D channel as a function of the gate voltage can be extracted as follows:

$$\mu_n = \frac{L_g}{q n_s W R_{\rm Ch}}, \tag{2}$$

where $R_{\rm Ch} = R_{\rm tot} - 2R_c - R_s - R_d$, $R_{\rm tot}$ is the measured drain–source resistance at low drain bias. The contact resistance R_C and the series resistances R_s and R_d of the source–gate and drain–gate openings were extracted from the transmission line model test pattern with the ohmic contact width of $W = 200$ μm, and the spacing ranging from 2 to 20 μm. From Eqs. (1) and (2), we find the concentration dependence of 2D electron mobility. This dependence is shown in Fig. 2 for the proposed AlGaN/GaN/AlGaN DH. Figure 2 also shows the theoretical concentration dependence of the 2D gas mobility[7,10] (normalized to 1000 cm^2/V s at $n_s = 10^{12}$ cm^{-2}). As seen, the experimental $\mu(n_s)$ dependence

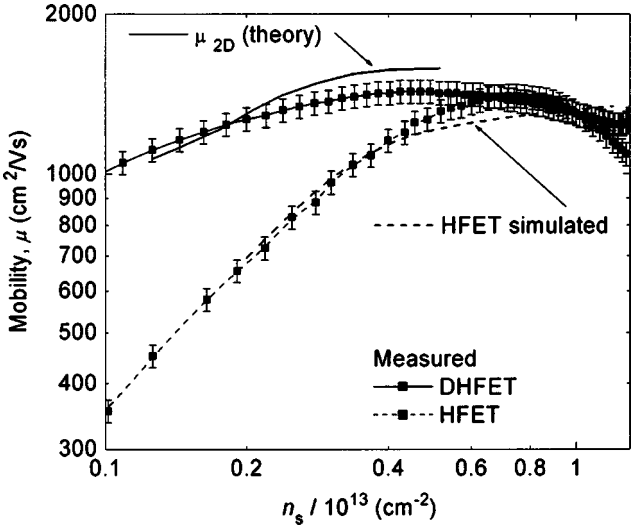

FIG. 2. Concentration dependencies of the electron mobility in the DHFET and regular HFET structures. The theoretical dependence for the 2D gas mobility after.[7,10] The $\mu_n(n_s)$ dependence for the HFET structure was simulated assuming the bulk electron mobility of 300 $cm^2/V\,s$.

follows closely the one predicted by the theory. For comparison, we also show a similar dependence extracted from a regular AlGaN/GaN HFET structure over SiC substrate. The simulated curve for the HFET structure also shown in Fig. 2 was modeled assuming the 2D channel with the $\mu_n(n_s)$ dependence after[10] being connected in parallel with a low-mobility ($\mu_n = 300\ cm^2/V\,s$) three-dimensional channel. As seen from the Fig. 2, μ_n first increases with n_s, reaches a maximum value, and then decreases with a further increase of n_s. The increase of μ_n with n_s can be explained by increased screening of ionized impurities and dislocations in the 2D electron gas.[11,12] The subsequent decrease of μ_n can be attributed to the electron's spillover from the 2D-channel to a parallel low electron-mobility parasitic conduction channel.[13,14] This concentration dependence for the mobility in DHFET is much less pronounced as compared to the HFET, which provides a clear evidence of the superior carrier confinement in the DHFET channel.

Sample DHFET devices with ~1.3-μm-long gate and 5-μm source–drain opening were fabricated from the epilayer structure described earlier using the fabrication procedure similar to that used for InGaN channel DHFETs.[1] All the layers were unintentionally doped. Ti(200 Å)/Al(500 Å)/Ti(200 Å)/Au(1500 Å) was used for source and drain ohmic contacts annealed at 850 °C for 1 min in nitrogen ambient. Ni/Au Schottky gates were then metalized. A reactive ion-etched mesa was used for the device isolation. The DHFET $I-V$ characteristics measured using HP 4156 parameter analyzer are presented in the Fig. 3. The devices have the peak saturation currents of 0.6–0.8 A/mm, with the threshold voltage of −3.5 V. These values are quite comparable with those typical for regular AlGaN/GaN HFETs. The knee voltage was 2.5–3 V at zero gate bias; the gate leakage current at $V_{GS} = -10$ V was around 3–5 μA/mm. Small and large signal rf characterization of the DHFETs is ongoing and the results will be published elsewhere.

In conclusion, we report an AlGaN/GaN/AlGaN double heterostructure that provides a highly confined 2D electron channel with high mobility and high sheet carrier density. The structure is promising for high-power current, collapse-free III-N DHFETs. A significant improvement in the carrier confinement was confirmed by the 2D electron-mobility–concentration dependence.

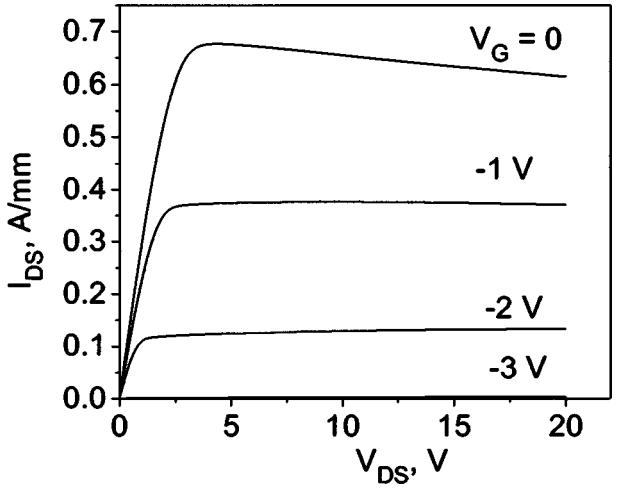

FIG. 3. $I-V$ characteristics of the sample DHFET with a 1.3-μm gate over a SiC substrate.

This work at USC was supported by Army SMDC Grant DASG 60-00-10003, monitored by F. Clarke and Kepi Wu, and by DARPA Grant DAAD19-02-10236, monitored by Dr. E. Martinez and Dr. A. Hung.

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