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Application of the Test for Memristor to Experimental Memory Devices

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Dedication

This thesis is dedicated to my parents who have been wonderful supporters and inspirations until my journey in South Carolina is completed, my brother who sent me funny memes every day and made me laugh throughout the hard times, and my beloved grandmother.

Acknowledgments

This thesis really happened with the kind support and help of many individuals. I would like to express my deepest gratitude to all of them.

Foremost, the completion of this thesis could not have been accomplished without my advisor Dr. Pershin with his continuous support and encouragement. And I also express thanks to Dr. Datta and committees with their advice to polish my final works. Finally, I would like to express the appreciation to the Department of Physics and Astronomy and all coordinators.

Without you all, this journey would not have been possible to be completed.

Abstract

In early seventies, the *memristor* was introduced as the fourth fundamental nonlinear two-terminal circuit element coupling the charge and flux by Dr. L. Chua. In 2008, the experimental discovery of the memristor was announced triggering significant interest in the development of resistance switching memory devices and their applications. According to Chua, the pinched hysteresis loop in the current-voltage characteristic of experimental memory devices is the fingerprint of memristors ("if it's pinched it's a memristor"). However, such loops are not an exclusive feature of memristors as they are also found in the response of other devices with memory that are not ideal memristors. Recently, an unambiguous test to find whether a resistive device with memory is a memristor or not has been proposed. In this thesis, the memristor test is applied experimentally to several devices that were previously claimed to be memristors. In particular, the test is applied to: (i) in-house fabricated Cu-SiO_2 cell, (ii) commercially available resistance switching memory cells, and (iii) so-called "Φ–memristor" (the latter was recently named as the "real memristor"). The results of the test indicate that all devices considered in this thesis are not memristors.

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Chapter 1

Introduction

1.1 Memristor as the forth fundamental circuit element

In 1971, Leon Chua – a professor of electrical engineering at UC Berkeley – proposed the use of the relations between circuit variables to define axiomatically the fundamental circuit elements [1]. He has demonstrated that the relations between the four circuit variables – the current (I), voltage (V), electric charge (q), and flux linkage (φ) [1] – not only define the traditional basic circuits elements (resistors, capacitors, and inductors) but also lead to a new circuit element, which he named as *memristor* [1]. In 2008, a group from Hewlett Packard (HP) directed by Stanley Williams announced the experimental discovery of the memristor [2].

In principle, there are six distinct pairs of four circuit variables: (I, V), (I, q), (I, φ), (q, V), (I, φ), and (V, φ). According to Chua [1], the relation coupling the current, I, and voltage, V, defines the resistor. The capacitors and inductors are defined by the relations coupling q and V, and φ and I, respectively. The relation coupling q and I does not define any element as the charge is the time integral of the current. The same situation holds for the pair (V, φ). The memristor has been defined by the remaining relation, which is between q and φ (see Fig. 1.1).

What is the electric response of memristors? To answer this question, consider the charge-controlled memristor defined by the following relation:

$$\varphi = f(q). \tag{1.1}$$

[1] The flux linkage is the time integral of the voltage.

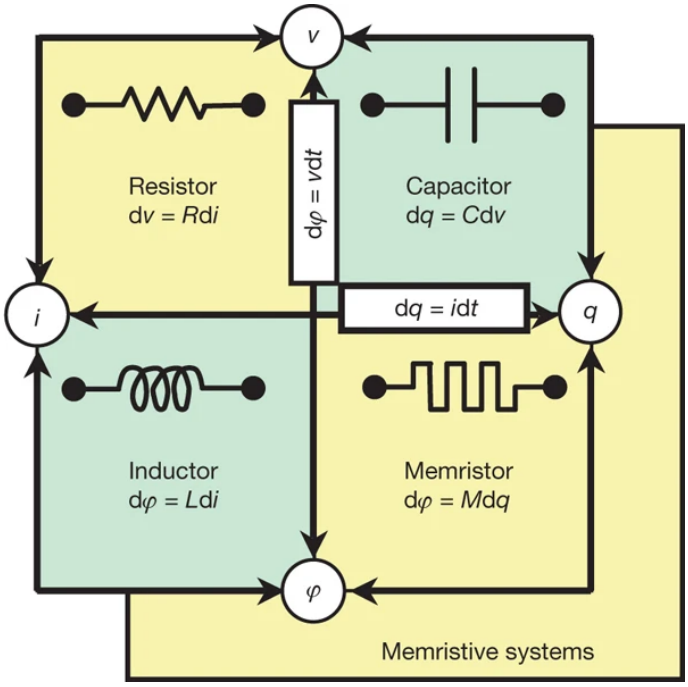

Figure 1.1 Diagram showing the definition of the fundamental circuit elements using pairs of circuit variables. The memristor is defined by the relation coupling q and φ. Reprinted with permission from [2] Copyright © 2008, Nature Publishing Group.

Here, $f(q)$ is a function of charge. The time derivative of Eq. (1.1) leads to

$$\frac{\mathrm{d}\varphi}{\mathrm{d}t} = V(t) = \frac{\mathrm{d}f(q)}{\mathrm{d}q}\frac{\mathrm{d}q}{\mathrm{d}t} \quad . \tag{1.2}$$

Defining the response function *M(q)* via

$$M(q) = \frac{\mathrm{d}f(q)}{\mathrm{d}q}, \tag{1.3}$$

and taking into account that the current is the time derivative of the charge, $\mathrm{d}q/\mathrm{d}t = I$, Eq. (1.2) can be rewritten as

$$V = M(q)I. \tag{1.4}$$

Eq. (1.4) describes a strange resistor whose resistance depends on the charge flowing through from the initial moment of time. Importantly, such a resistor remembers the amount of charge which has flowed and thus has a memory. It has been named the

Figure 1.2 The circuit symbol of memristor suggested by Dr. Chua [3].

memristor, which is the portmanteau formed by the combination of words memory and resistor. The response function $M(q)$ is known as the memristance (memory resistance). The symbol of memristor is presented in Fig. 1.2.

Alternatively, the constitutive relation (1.1) can be presented in the flux-controlled form. The solution of Eq. (1.1) with respect to q can be symbolically written as

$$q = g(\varphi), \tag{1.5}$$

where $g(\varphi)$ is a function of flux. The time derivative of Eq. (1.5) leads to the equation

$$I = G(\varphi)V, \tag{1.6}$$

where the response function $G(\varphi) = \mathrm{d}g(\varphi)/\mathrm{d}\varphi$ is the memductance (for memory conductance). In applications of the memristor model, the charge (in the charge-controlled memristors) or flux (in the flux-controlled ones) represents the dynamics of some internal degrees of freedom in physical devices.

When a non-zero voltage V is applied to memristor, the current flows through the device, and the charge q changes (the memristance $M(q)$ changes too since it is a function of charge). When the applied voltage V is zero, the memristance M does not change (it is "frozen"). This is how the memristor remembers its state. Such unique capability of memorizing the device state (and thus the history of applied signals) is what makes the memristor attractive for various applications (such as neuromorphic computing [4, 5, 6], in-memory logic [7, 8], etc.). Experimentally, the memory feature of memristors is manifested by pinched hysteresis loops [1] (an example is given below, see Fig. 1.4).

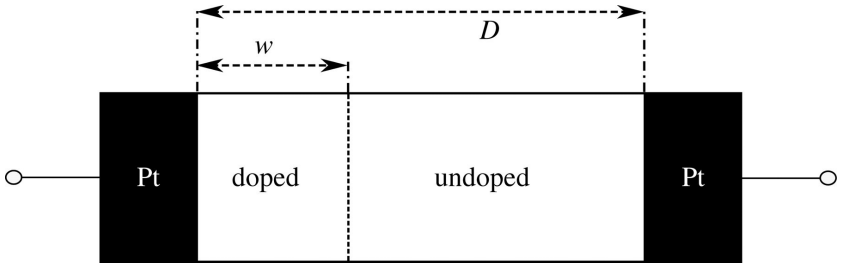

Figure 1.3 Schematic of HP memristor model. Here, D is the thickness of the insulator layer and w is the thickness of the doped region [12]. Adapted with permission from [2] Copyright © 2008; Nature Publishing Group.

1.2 HP MODEL OF MEMRISTOR

The authors of the seminal paper "The missing memristor found" [2] have argued that the resistance switching memory cells – nanoscale structures with memory which has been known since the sixties [9, 10] – are memristors. Such structures have a capacitor-like geometry consisting of an (initially) insulating layer sandwitched between two metal electrodes. According to the Hewlett-Packard (HP) model, the resistance of the central (insulator) layer is controlled by the time integral of the current through the structure or, equivalently, by charge. To explain the resistance switching behavior, it was proposed [2] that the central layer can be described as the combination of a doped region and undoped region, and the boundary between these regions moves as the current flows through the structure.

Physically, the devices fabricated and investigated by HP laboratories had $Pt/TiO_2/Pt$ structure [11]. Fig. 1.3 shows the separation of TiO_2 layer into the doped and undoped regions (characterized by a low and high resistivity, respectively). Let's denote the thickness of TiO_2 film by D, and the thickness of the doped (by oxygen vacancies) region by w. We emphasize that w plays the role of the internal state variable (the variable defining the device/resistance state). Its change is limited to the interval between 0 and D.

The instantaneous response of the structure in Fig. 1.3 can be presented by Ohm's law

$$V(t) = R_M(w)I(t), \tag{1.7}$$

where $R_M(w)$ corresponds to the memristance $M(q)$ in Eq. (1.4). The resistance $R_M(w)$ can be approximated by a two-resistor model, where the resistances of doped and undoped layers depend on w, which is generally a function of time. In the limiting cases of $w = D$ and $w = 0$, $R_M = R_{ON}$ and $R_M = R_{OFF}$, respectively. R_{ON} and R_{OFF} are known as the resistances in the ON and OFF states of the structure.

In the linear approximation, the resistance can be written as

$$R_M = R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right). \tag{1.8}$$

Using Eq. (1.8), the relation between the voltage and the current is given by

$$V(t) = \left[R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right] I(t). \tag{1.9}$$

Next, consider the dynamnics of $w(t)$. The authors of Ref. [2] used a first-order differential equation to describe the evolution of $w(t)$ with a linear relationship between $\mathrm{d}w(t)/\mathrm{d}t$ and $I(t)$:

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \mu_V \frac{R_{ON}}{D} I(t). \tag{1.10}$$

Here, μ_V is the migration rate of the doped region (dopant mobility). The time integral of Eq. (1.10) yields the following expression for the thickness of the doped region, $w(t)$,

$$w(t) = \mu_V \frac{R_{ON}}{D} q(t) + w_0, \tag{1.11}$$

where w_0 is the initial thickness (at $t = 0$). Eq. (1.11) indicates that the distribution of dopants in the device – described by $w(t)$ – is a linear function of the charge q passing through the device.

One can verify that the model given by Eqs. (1.9) and (1.11) is the model of a charge-controlled memristor, Eq. (1.1). Specifically, it corresponds to the constitutive

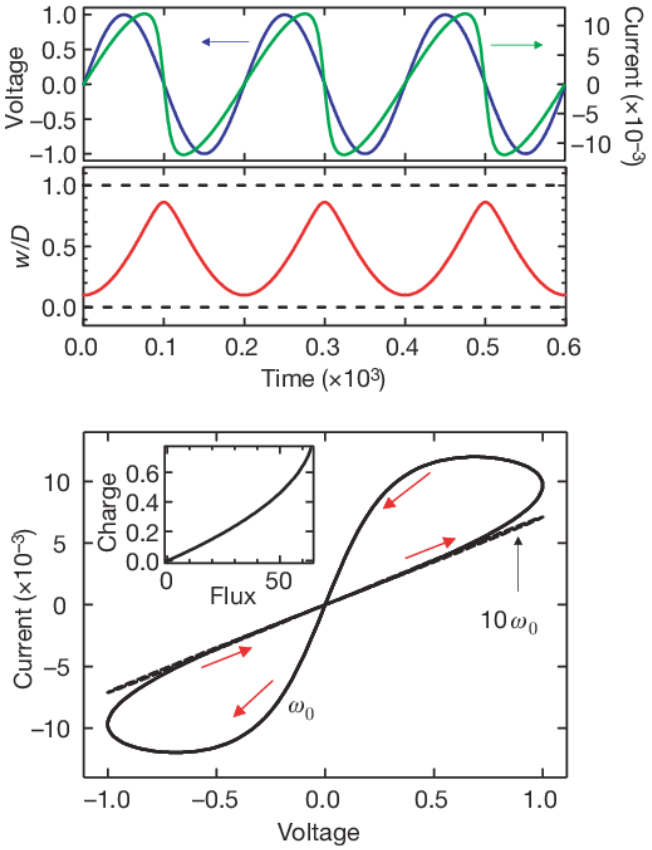

Figure 1.4 Pinched hysteresis loop (bottom graph) as a result of the sinusoidal voltage (blue line, top graph) applied to the device. The response current is shown in green (top graph). The applied voltage is $v_0 \sin(\omega t)$, where v_0 is the magnitude of the applied voltage and ω is the frequency. The inset in the current-voltage plot shows that the charge is a single-valued function of the flux, what is claimed to be a memristor. Reproduced with permission from [2] Copyright © 2008; Nature Publishing Group.

relation

$$\varphi = R_{OFF}\left\{q(t)\left[1+\frac{w_0}{D}\left(\frac{R_{ON}}{R_{OFF}}-1\right)\right]-\frac{\mu_V R_{ON}}{2D^2}\left(1-\frac{R_{ON}}{R_{OFF}}\right)q(t)^2\right\}+\varphi_0. \quad (1.12)$$

Indeed, by differentiating Eq. (1.12) with respect to the time, one can derive Eq. (1.7)

with

$$M = \frac{\mathrm{d}\varphi}{\mathrm{d}q} = R_{OFF}\left\{1 + \frac{w_0}{D}\left(\frac{R_{ON}}{R_{OFF}} - 1\right) - \frac{\mu_V R_{ON}}{D^2}\left(1 - \frac{R_{ON}}{R_{OFF}}\right)q(t)\right\}. \quad (1.13)$$

Clearly, Eq. (1.13) is exactly the same as Eq. (1.8) with $w(t)$ given by Eq. (1.11). Moreover, if $R_{ON} \ll R_{OFF}$, the memristance $M(q)$ simplifies to

$$M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2}q(t) - \frac{w_0}{D}\right). \quad (1.14)$$

The dependence of M on linear dimensions indicates that the resistance switching process depends on such parameters. Such parameters can be controlled at the fabrication stage. [2, 12, 13].

Fig. 1.4 demonstrates current-voltage characteristics of the HP memristor model when the memristor is driven by a sinusoidal voltage. At the driving frequency $\omega = \omega_0$, the current-voltage curve has the form of a pinched loop (eight-shaped geometry with self-crossing at the origin). The size of the loop depends on the frequency. At $\omega = 10\omega_0$, the loop shrinks to a line.

1.3 Memristive systems

1.3.1 General equations

The memristor model introduced in the section 1.1 is based on fairly abstract mathematical equations that are disconnected from the physics of electronic devices with memory. Therefore, there was a need for a better model that would take into account directly the physical processes in real devices. Such a model was developed in the mid-seventies by Chua and Kang [14].

In 1976, Chua and Kang suggested the concept of memristive systems [14] that generalizes the model of the memristor [1] to a broader class of nonlinear dynamical

systems. The memristive systems are defined by [14]

$$y(t) = g(\mathbf{x}, u, t)u(t) \ , \tag{1.15}$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, u, t) \ , \tag{1.16}$$

where u and y denote the *input* and *output* of the system, $\mathbf{x}$ represents the n internal state variables, $g(\mathbf{x}, u, t)$ is the response function, and $\mathbf{f}(\mathbf{x}, u, t)$ is the n-dimensional vector function describing the evolution of internal state. The relevance of dynamical models to physical devices significantly depends on the choice of internal state variables and their equations of motion. These are typically selected to represent physical processes taking place in real devices.

Eqs. (1.15) and (1.16) contain two types of memristive systems (differentiated by the choice of the input and output). An nth-order current-controlled memristive system is defined by [15]

$$V_M(t) = R(\mathbf{x}, I, t)I(t) \ , \tag{1.17}$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, I, t) \ , \tag{1.18}$$

where $V_M(t)$ and $I(t)$ represent the voltage across and current through the device, respectively. Note that $R(\mathbf{x}, I, t)$ is the generalized resistance (memristance). We note that the charge-controlled memristors (Eq. (1.4)) are the special cases of Eq. (1.17) with R depending *only* on charge. We emphasize that the memristive system equations describe a very broad class of memory devices that contains memristors as a special case.

The voltage-controlled memristive devices correspond to the opposite choice of the input and output:

$$I(t) = G(\mathbf{x}, V_M, t)V_M(t) \ , \tag{1.19}$$

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}, V_M, t) \ . \tag{1.20}$$

Here, $G(\mathbf{x}, V_M, t)$ is the *memductance* (see also Eq. (1.6)).

From Eqs. (1.17) and (1.19) it follows that $V_M = 0$ when $I = 0$ and vice versa (zero-crossing property). Moreover, when subjected to periodic input, the current-voltage curves of memristive devices have the form of pinched hysteresis loops [14].

1.3.2 Example of memristive model

TEAM and VTEAM models [16, 17] are popular memristive models that describe realistically the response of physical memristive devices. They are particular realizations of memristive models introduced in Sec. 1.3.1 above. In contrast to the ideal memristor models (such as the HP model [2] or Φ-memristor model [18] discussed in next subsection), TEAM and VTEAM involve a threshold (in the current or voltage, respectively) that is typically observed in the response of experimental resistance switching cells. According to Kvatinsky et al. [16, 17], with thresholds, the models are more accurate compared to other models. Because of their efficiency, generality and sufficient accuracy, TEAM and VTEAM models fit the experimental response of memristive device better than previously proposed models, and are also suitable for the computer-assisted design of memristive circuits.

Let's discuss the VTEAM model [17] in more detail. VTEAM stands for Voltage ThrEshold Adaptive Memristor model. This model takes into account the threshold voltage observed in the switching characteristics of many memristive devices (see examples presented in Fig. 1.4 (from Refs. [2, 19, 20]) and Fig. 1.5 (from [21])). The VTEAM model belongs to the class of voltage-controlled memristive systems (Eqs. (1.19) and (1.20)).

In VTEAM, the derivative of the state variable is described by

$$\frac{\mathrm{d}w(t)}{\mathrm{d}t} = \begin{cases} k_{off} \cdot \left(\frac{V_M(t)}{v_{off}} - 1\right)^{\alpha_{off}} \cdot f_{off}(w), & 0 < v_{off} < V_M \\ 0 & v_{on} < V_M < v_{off} \\ k_{on} \cdot \left(\frac{V_M(t)}{v_{on}} - 1\right)^{\alpha_{on}} \cdot f_{on}(w), & V_M < v_{on} < 0 \end{cases} \tag{1.21}$$

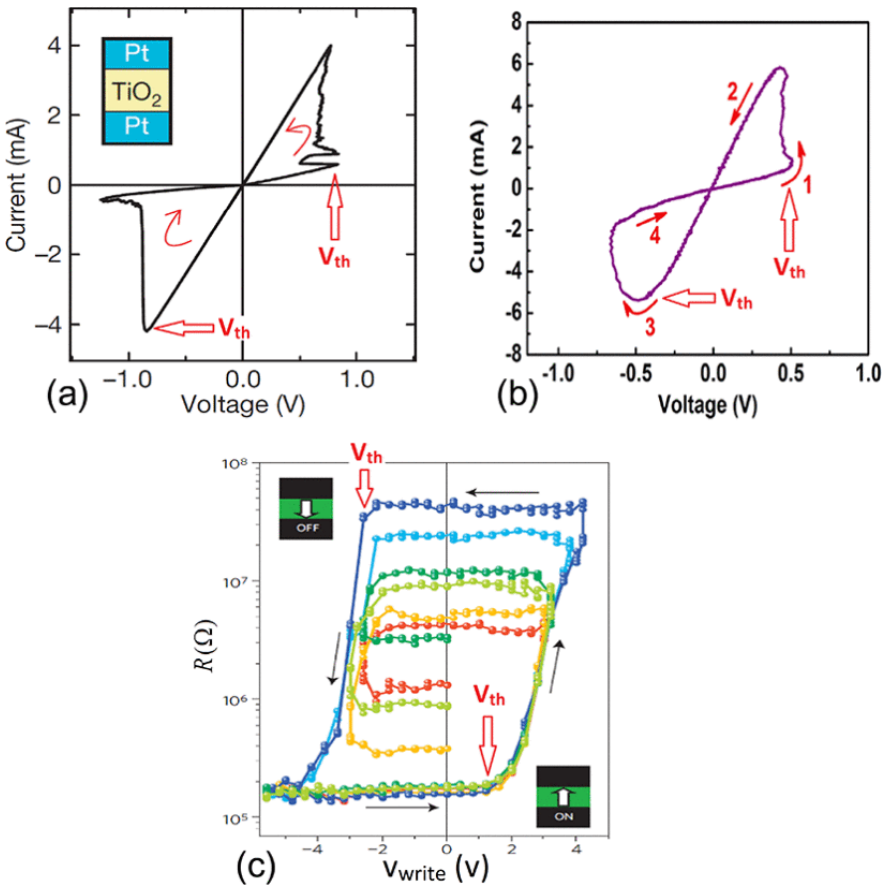

Figure 1.5 Selected experimental results that show the threshold, V_{th}, in the current-voltage curves of memristive devices. (a) $Pt/TiO_2/Pt$ memristor [2]. (b) Ag-a-LSMO-Pt memristor. Reprinted with permission from [19] (Copyright © 2013, American Chemical Society). (c) Ferroelectric memristor. Reproduced from [20] Copyright © 2015; IEEE.

where $k_{off} > 0$, $k_{on} < 0$, α_{off}, and α_{on} are constants, and v_{on} and v_{off} are threshold voltages. $f_{off}(w)$ and $f_{on}(w)$ are window functions [22, 23, 24, 25] used to limit the evolution of w to the allowed region (typically, the state variable is bound: $w \in [w_{on}, w_{off}]$).

There is a freedom in the choice of $G(w, v)$. For instance, in the case of a linear dependence of memristance on w, Ohm's law is written as

$$I(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{off} - w_{on}} \cdot (w - w_{on}) \right]^{-1} \cdot V_M(t) \tag{1.22}$$

where w_{on} and w_{off} are the bounds of the internal state variable w, and R_{ON} and

R_{OFF} are the resistances of the device when the state variable is w_{on} and w_{off}, respectively. On the other hand, an exponential dependence of the state variable w can also be assumed [26]. The relationship between the current and voltage then is

$$I(t) = \frac{e^{-\frac{\lambda}{w_{off}-w_{on}}\cdot(w-w_{on})}}{R_{ON}} \cdot V_M(t) \ . \tag{1.23}$$

Here, λ is a fitting parameter, and $e^{\lambda} = R_{OFF}/R_{ON}$.

1.4 Experimental memristive devices

In this section, different types of memristive devices are introduced according to their switching mechanisms. There are three frequently discussed redox (reduction and oxidation) based resistive switching mechanisms - electrochemical (cation-based), valence-change (anion-based), and thermochemical (both cation- and anion- based) abbreviated as ECM, VCM and TCM, respectively [27, 28]. Moreover, we introduce Φ-memristor, which was recently considered the "true memristor" [18]. It is important to understand the operational principles of these devices, which form the basis for their modeling and applications.

1.4.1 Electrochemical metallization cells

Electrochemical metallization (ECM) cells [29, 30] are one of the most recognized classes of resistive random access (ReRAM) memory cells. The mechanism of resistance switching in ECM cells is based on the electrochemical growth and dissolution of conductive metallic filament in an insulating matrix. This mechanism involves the charge transfer with the metallic cations (e.g. Ag and Cu) and their migration. Once the device is formed, it can be switched between the low resistance state (LRS) and high resistance state (HRS) back and forth under the applied bias. Generally, the architecture of ECM cells consist of a thin film layer of insulating materials such as binary oxide (e.g. SiO_2 [21, 31], Ta_2O_5 [32], ZnO [33, 34] and GeSe [35]). SiO_2 is often

employed as the active switching medium in ECM cells making them compatible with the conventional semiconductor fabrication process. Such ECM cells are considered for use in high-density memory applications [21].

The selected oxide medium is sandwiched between an eletrochemically active electrode (e.g. Ag, Ni or Cu) and inactive (inert counter) electrode (e.g. Pt or W, etc.) [36, 37, 38, 39]. The initial dissolution of active electrode is required and performed by the application of, say, positive bias voltage (electroforming). Then the dissolved active electrode cations migrate through the oxide film (assuming a sufficient electric field) and this process is called SET. The active electrode cations are reduced at the surface of the inert counter electrode and form a conductive filament. Once the metallic filament has grown and made contact from the inert counter electrode to the opposite active electron, the cell switches to the ON state. The cell retains the ON state until a high enough voltage of opposite polarity is applied to the cell. In the $RESET$ phase, the electrochemical dissolution of the metallic filament disconnects the contact between the electrodes and the active cations return to their electrode [40]. This cycle of processes repeats assuming that the voltage and current are within safe bounds. To prevent potential damage to the device, the compliance current is usually used in experiments [41].

Let us now consider the resistance switching processes in ECM cells in detail. We will use the example of a Cu/SiO_2/Pt cell, whose structure and characteristics were investigated by C. Schindler *et al.* [21]. Fig. 1.6 shows the switching schematics in a single cycle of voltage sweep with an exhibition of threshold voltage. The process of the resistance switching in this cell can be described as follows:

(A) Positive bias voltage applied to the Cu electrode: Anodic dissolution of Cu (Cu $\rightarrow$ $Cu^{z+} + ze^{-}$) from Cu electrode produces the metal cation of Cu, Cu^{z+}. The Cu^{z+} cations then drift across the SiO_2 medium under the action of an electric field by the applied voltage (SET).

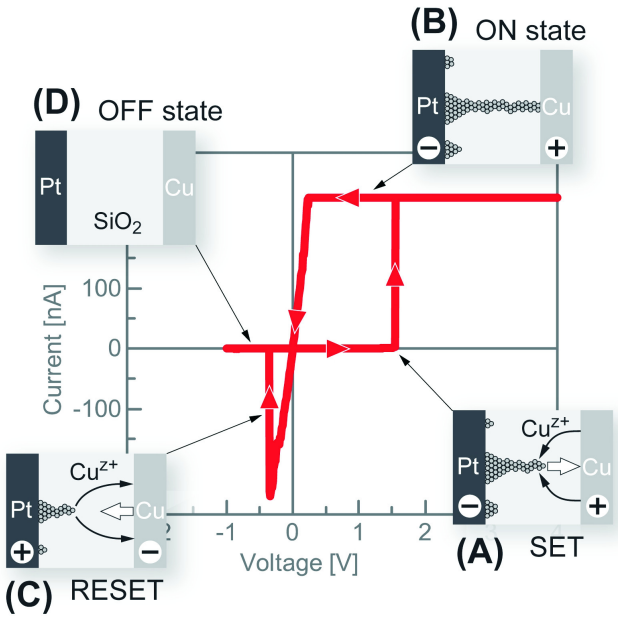

Figure 1.6 Current-voltage characteristics of a $Cu/SiO_2/Pt$ electrochemical memory (ECM) cell indicate the bipolar switching regime. Figures (A)-(D) present four stages of formation and dissolution of Cu filament. Reproduced from [21] Copyright © 2009; AIP Publishing

(B) The formation of Cu electrodeposits according to the reaction, $Cu^{z+} + ze^{-} \rightarrow Cu$, causes a cathodic reaction on the inert electrode Pt. This Cu filament creates a connection between Cu and Pt electrodes so that the current can flow across the device (ON state).

(C) Negative voltage is applied to the copper electrode: As the applied voltage decreases, Cu^{z+} cations begin to drift back to the Cu electrode ($RESET$).

(D) Eventually, the filament is dissolved and disconnected. The state will be turn to the OFF state.

1.4.2 Valence change memories

Valence change memory (VCM) cells are another major class of ReRAM cells (besides the ECM cells). The VCM cells involve metal oxides (e.g. HfO_x, TiO_x, and TaO_x) [42, 43, 44] that play a role of insulator layer between electrodes. Typically, these electrodes consist of metals with different affinities. The electro-active electrode (e.g. Pt or TiN) [40] with a high work function and low oxygen affinity forms a Schottky-type contact with the oxide [45]. The opposite electrode, which is electro-inactive (ohmic electrode), has a low working function and consists of oxidizable metals (e.g. Hf, Zr, Ta, and Ti) [46, 47]. The process of resistance switching involves a partial reduction of the cation sublattice by partial oxidation of the ohmic electrode. In the oxide material, the oxygen vacancies (see Fig. 1.7 where V_O^- refers to the oxygen vacancy [48]) play a crucial role as a dopant, which lowers the resistance of the oxide. Thus, the oxygen exchange between the electrodes and binary oxide results in the resistive switching in VCM cells [49, 39].

Initially, an electroforming step is *required* to enable the switching functionality. The application of a voltage V_{FORM} (higher than the operating voltage) induces a soft breakdown of the oxide, within which oxygen vacancies are generated. The transition to the low resistance state (LRS) occurs [50]. When the formation of a conductive filament of oxygen vacancies causes LRS, the process is called SET and in this step, the compliance current is usually applied to prevent the destruction of the device. The filament can be dissolved by the voltage of the opposite polarity (it causes HRS and this process is known as $RESET$). The growth direction and rate depend on the forming voltage, materials and the relation between oxygen exchange rate and ion migration. Consequently, the main steps of VCM switching are: electroforming process starting with the initial pristine state, generation of oxygen vacancies and growth of conductive filament that makes a connection between electrodes (SET process, ON state), and disconnection of the filament caused by the voltage of the

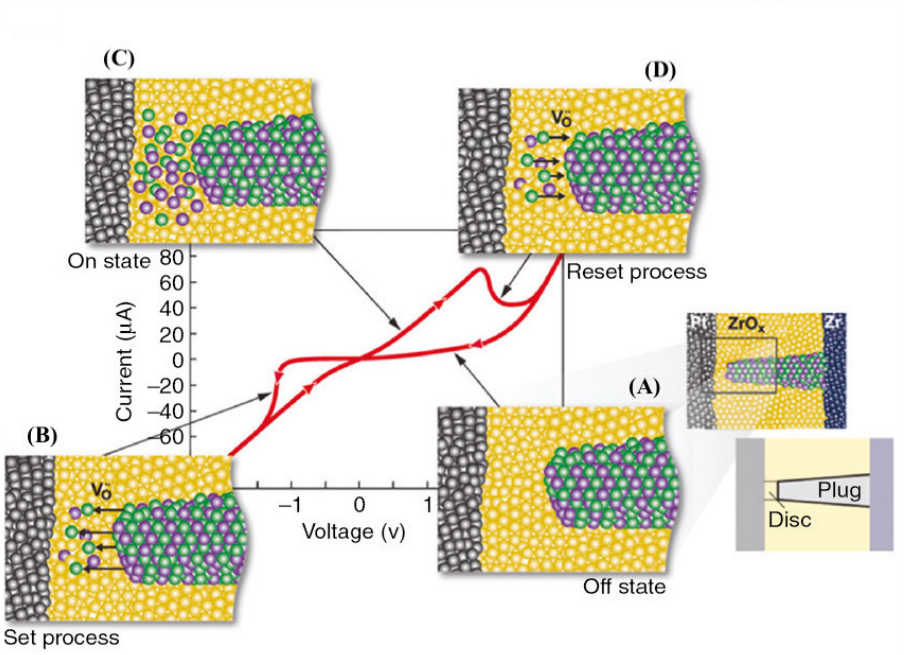

Figure 1.7 Schematics of the resistance switching in a Pt/ZrO_x/Zr valence change memory (VCM) cell. In this cell, Pt is the active electrode and Zr is ohmic contact metal. Reprinted with permission from Ref. [51] Copyright © 2012; John Wiley and Sons, Inc.

opposite polarity (*RESET*).

Fig. 1.7 illustrates schematically the resistance switching process in a periodically driven Pt/ZrO_x/Zr stack [51]. In the stack structure shown to the right, the grey color to the left depicts the active Pt electrode, while and the ohmic (inert) Zr electrode is shown to the right. In Fig. 1.7, the oxygen vacancies are indicated by the green dots, whereas the violet dots represent the metal ions. As shown in this figure, the threshold-type bipolar switching is observed. The current-voltage curve is explained using the following steps:

(A) In the initial state, the filament is incomplete. The cell is thus in the HRS (*OFF* state).

(B) When negative voltage is applied, the active Pt electrode attracts the positively

charged vacancies, what results in a valence change with the filamentary cation sublattice formed (SET process).

(C) Eventually, Pt and Zr electrodes are connected by the filament (LRS or ON state).

(D) The positive applied voltage leads to $RESET$ in which the vacancies are repelled from Pt electrode. The filament becomes incomplete.

1.4.3 Thermochemical memories

The resistance switching in thermochemical (TCM) cells depends on thermal effects in which a current-induced temperature leads to a fuse-antifuse process. In TCM cells, the thermochemical redox processes dominate over electrochemical effects [40]. The study of Ielmini *et al.* [53] employs NiO as a dielectric layer material (NiO is often used in TCM cells). The mechanism is based on the thermal effects, such as Joule heating that governs local redox reactions according to the precisely controlled temperature, and a certain amount of release of oxygen causes the formation of metallic filament. Similarly to ECM and VCM cells, the switching mechanism is also filamentary [54] but TCM cells exhibit unipolar switching curves (the switching characteristics of ECM and VCM cells are bipolar) [55, 56].

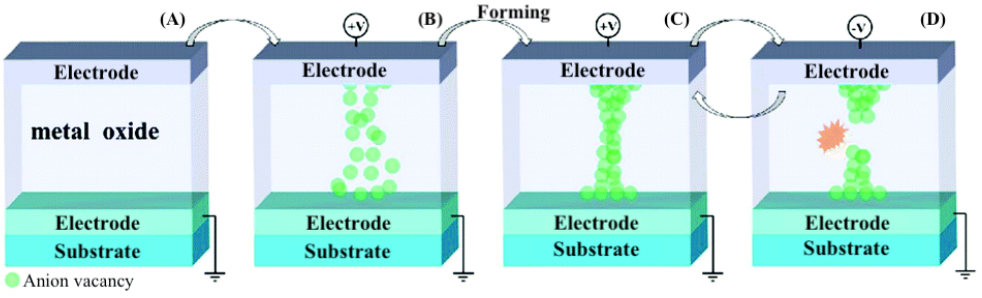

Figure 1.8 Schematics of the filament formation and disruption in the thermochemical memory cell. Reproduced with permission from Ref. [52] Copyright © 2020; Journal of Materials Chemistr).

The switching process in TCM cells involves the following states and steps (see Fig. 1.8):

(A) Initial pristine state (OFF state).

(B) Oxygen ions start to drift in the dielectric layer as the applied voltage increases to form a conductive filament composed of oxygen vacancies and metallic interstitials (SET).

(C) Formed filament connects electrodes (ON state).

(D) Joule (local) heat is generated and breaks the filament ($RESET$, transition to OFF).

1.4.4 Φ-MEMRISTOR

Wang *et al.* [18] claimed that they invented a new type of memristor, namely, the Φ-memristor, and that the Φ-memristor is ideal. The operation of the Φ-memristor is based on the direct interaction of the magnetic flux φ and electric charge q. The design of the Φ-memristor involves a current-carrying wire and magnetic core combined such that the voltage is induced by the controlled physical flux. The name Φ-memristor is a symbolic one: the ring in "Φ″ indicates a magnetic lump and the vertical bar in "Φ″ represents a wire going through the magnetic lump (core). Moreover, Φ can represent the magnetic flux φ, which was not involved in other memristor designs.

Fig. 1.9 illustrates the schematic of a Φ-memristor having the magnetization $\mathbf{M}$ interacting with the charge in the wire. According to Oersted's law, the field generated by the current, I, rotates the magnetization, $\mathbf{M}$, of the lump. The switched flux φ induces a voltage v across the conductor, resulting in the memristance M. According

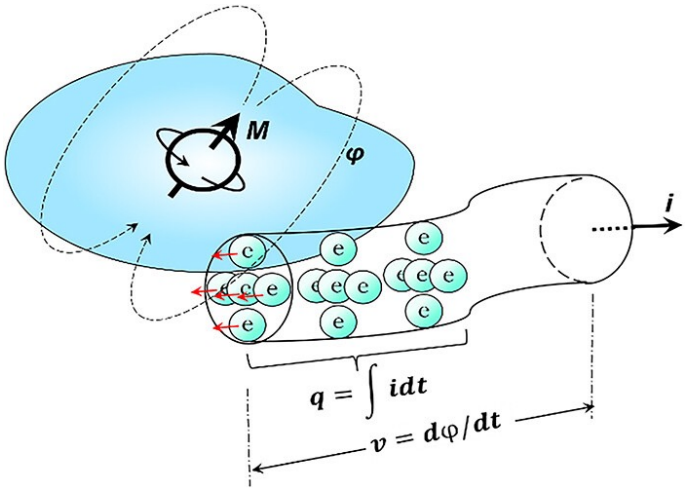

Figure 1.9 Illustration of the Φ memristor that involves a physical coupling of the flux φ and charge q. **M** is the magnetization of the lump. Reprinted with permission from [18] Copyright © 2009; AIP Publishing.

to [18], the memristance is the function of charge according to

$$M(q) = \frac{\mathrm{d}\varphi}{\mathrm{d}q} = \frac{\mu_0 \mathrm{S} M_\mathrm{s}}{\mathrm{S_W}} \operatorname{sech}^2\left(\frac{q}{\mathrm{S_W}} + \tanh^{-1} m_0\right) \geq 0. \tag{1.24}$$

Here, μ_0 is the permeability of free space, S is the cross-sectional area, M_s is the magnitude of saturation magnetization, $\mathrm{S_W}$ is the switching coefficient, and $m_0 = M_z(t=0)/M_s$.

Fig. 1.10 shows the experimental response of a Φ-memristor. The authors of Ref. [18] claimed that such response is compatible with the ideal memristor model.

1.5 Memristor test

In 1971, L. Chua introduced memristors as a specific class of device satisfying Eq. (1.1) or, equivalently, Eq. (1.4). In 2014, he claimed that pinched hysteresis loops can be used to distinguish memristors from non-memristors [57]. But is it a good test for memristors? The answer is no, since the devices belonging to a very broad class of memristive systems (discussed in Sec. 1.3) do also exhibit pinched hysteresis loops.

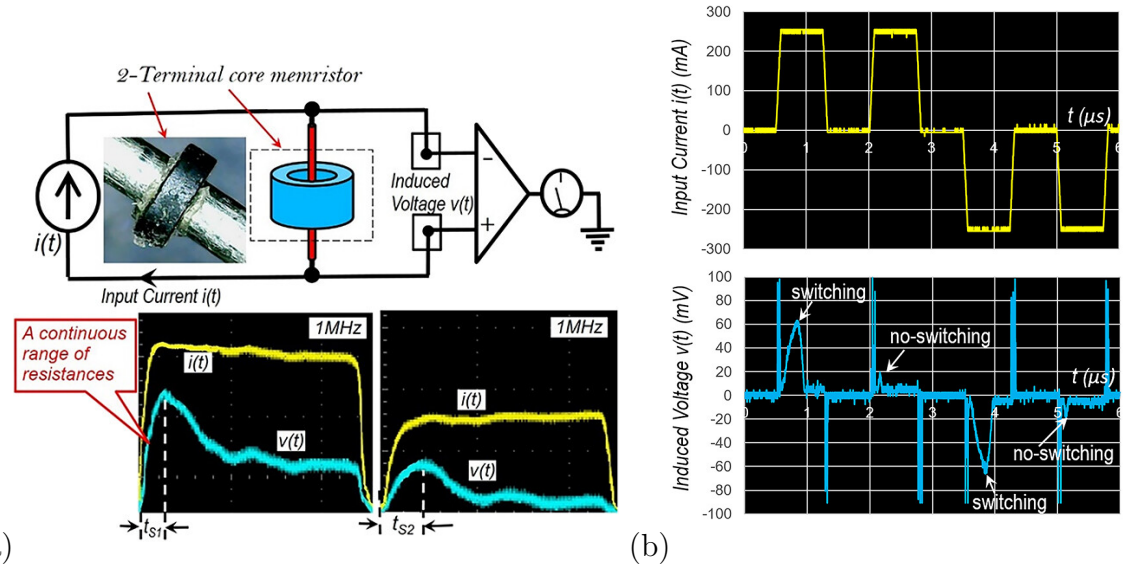

Figure 1.10 (a) Experimental circuit and picture of Φ-memristor. The response to current pulses that is supposed to verify the Φ-memristor model. (b) Voltage induced by a series of current pulses. The voltage response exhibits a yes-no-yes-no reversal pattern. The horizontal scale is 1 μs/div. The certical scales are 100 mA/div (upper) and 50 mV/div (lower). Reprinted with permission from [18] Copyright © 2009; AIP Publishing.

Consider, for instance, the memristor described by

$$R_M(q) = R_0 + \alpha(q - q_0)^2 \quad , \tag{1.25}$$

where R_0 is the minimal value of R_M, α is a constant, and q_0 is used to define the initial value of R_M, and the memristive system described by the equations proposed in [58]:

$$I(t) = R_M^{-1} V_M(t) \tag{1.26}$$

$$\frac{\mathrm{d}R_M}{\mathrm{d}t} = \begin{cases} \beta(V_M - V_t) & \text{if } V_t < V_M \\ \beta(V_M + V_t) & \text{if } V_M < -V_t \\ 0 & \text{otherwise} \end{cases} . \tag{1.27}$$

Here, the memristance R_M is chosen as the internal state variable ($x = R_M$ from Eq. 1.20), β is the switching rate, V_t is the threshold voltage value. Also, it is assumed

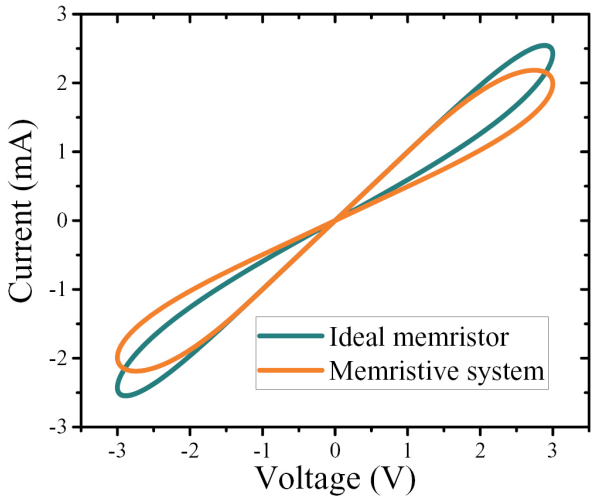

Figure 1.11 Current-voltage characteristics of the ideal memristor and a threshold-type memristive system driven by a sinusoidal voltage source $V(t) = V_0 \sin(2\pi\nu t)$. The ideal memristor plot (green curve) is based on Eq. (1.25), while the memristive system plot (orange curve) is based on Eq. 1.26 and Eq. 1.27. For more details see Ref. [59]. Reprinted with permission from [59] Copyright © 2018; IOP Publishing Ltd.

that R_M is in the range of $[R_{ON}, R_{OFF}]$, where R_{ON} and R_{OFF} are the low and high resistance states of the typical memristive system, respectively [58]. Fig 1.11 shows pinched hysteresis loops for both models, which are practically indistinguishable. Therefore, the pinched hysteresis test [57] can not be used as the test for a memristor.

Recently, Pershin *at al.* [59] introduced a simple memristor test to *unambiguously* distinguish ideal memristors (that satisfy the fundamental equation (1.4)) from all other devices that show the pinched hysteresis loop behavior, but whose memristance does not depend on the charge (as in Eq. (1.4)). The suggested setup consists of a capacitor and memristor connected in-series (see Fig. 1.12(a)). This measurement utilizes the fact that the capacitor that is initially uncharged progressively charges as the charge flows through the memristor. Once the charged capacitor discharges through the memristor and the final charge on the capacitor is zero, the state of the

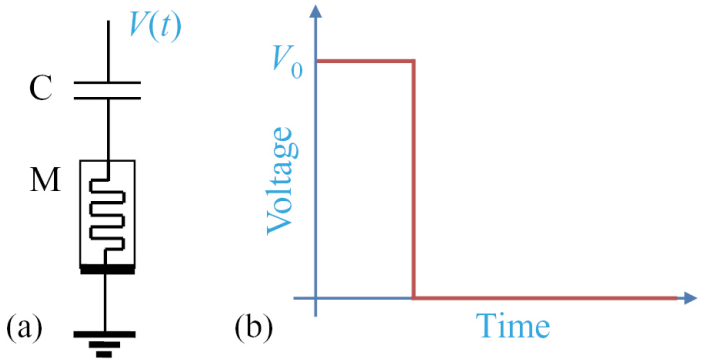

Figure 1.12 (a) Setup of the memristor test. (b) Simplest voltage waveform, $V(t)$, for the memristor test. Reprinted with permission from [59] Copyright © 2018; IOP Publishing Ltd.

memristor is measured. If the memristor is ideal, the initial and final memristances should be identical for *any* form of the voltage as long as enough time is given for the capacitor to discharge. In this regard, the simplest form of the voltage is the rectangular pulse followed by zero bias (depicted in Fig. 1.12(b)). This measurement method is fairly simple and accessible enough to be performed at any research laboratory.

Therefore, the selected device passes the test if the final state is the same as the initial state (within experimental accuracy) for a broad range of applied voltage waveforms.

1.6 Objectives

In this thesis, the memristor test [59] is applied experimentally to several devices that were claimed to be memristors in the literature [2, 60, 18].

Specifically, in the next paragraph, the test is applied to an (i) in-house fabricated Cu-SiO_2 cell, and (ii) commercially available resistance switching memory cells. Such

devices exhibit pinched hysteresis loops in their response and, thus, according to the criterion of Chua [57], must be memristors. We challenge this conclusion by performing the recently suggested memristor test [59] .

Next, the memristor test [59] is appleid to the Φ-memristor. In order to evaluate this type of device, a Φ-memristor was fabricated according to the documented structure and parameters [18], and its behavior and response are analyzed using several amplitudes of the applied voltage.

Chapter 2

Test application to Electochemical metallization cells

2.1 Experiment description and goals

According to the memristor test [59], an experimental device is a memristor if its final and initial states are the same under the condition of zero net charge flowing through the device. In this Chapter, the ideal memristor test is applied to resistive random access memory cells using ECM cells as representative devices. The experimental steps were as follows:

(i) Experimental ECM cells (Cu-SiO_2-Ru) were fabricated using the magnetron sputtering deposition technique. See the inset diagram in Fig. 2.1(a) for the details of device structure.

(ii) Commercially available ECM "memristor" devices, Knowm BS-AF-W memristor with dopant W and Knowm Self-Directed-Channel (M+SDC) memristor with dopant Cr [61] were secured for our experiments.

(iii) Typical current-voltage characteristics of "memristors" were obtained for the in-house fabricated cells and commercial devices. Fig. 2.1 presents five $I - V$ loops measured for Cu-SiO_2, BS-AF-W, and M+SDC Cr devices.

(iv) Ideal memristor test was applied to the Cu-SiO_2 device and commercial devices.

The goal of these experiments is to find whether ReRAM cells are memristors or not. As these devices show pinched hysteresis loops in their response to a periodic voltage or current, according to the arguments of Chua [60, 57], they must be memristors. However, as was mentioned above, the pinched hysteresis loops are also observed in the response of devices that are not memristors. To find whether ReRAM cells are memristors or not, we apply the memristor test [59] to these devices, wherein the initial and final states are compared under various driving conditions in the capacitor-DUT circuit (DUT stands for a device under test).

2.2 Fabrication of Cu-SiO_2 cells

For our studies, a metal/oxide/metal ECM cell – one of the most basic and promising ReRAM devices – was fabricated using a Cu-SiO_2 material combination [62]. We used the magnetron sputtering deposition technique on a silicon substrate for nanofabrication. 5 nm Ti layer was deposited on the surface of Si substrate as an adhesion layer. On the Ti surface, 30 nm Ru was deposited as an inert (inactive) electrode. Then the oxide layer (SiO_2) was deposited with a thickness of 10 nm on the Ru electrode using a shadow mask with 10 X 10 mm square openings. On the SiO_2 layer, a 30 nm Cu top electrode was deposited using the other type of shadow mask with openings of various sizes and shapes. Then the Cu top electrodes were coated by 5 nm CoCrPt to protect them from oxidation and to prevent from physical damage on the surface. Lastly, the device was thermally treated at 580 °C for 1 hour in a He environment to introduce Cu atoms into SiO_2. This step was suggested in Ref. [62]. The results presented below were obtained from the circular top electrode of radius of 710 μm.

2.3 Current-Voltage Measurements

Once the in-house fabricated cells and commercial devices became available, the measurements of their current-voltage characteristics were conducted. The measurement

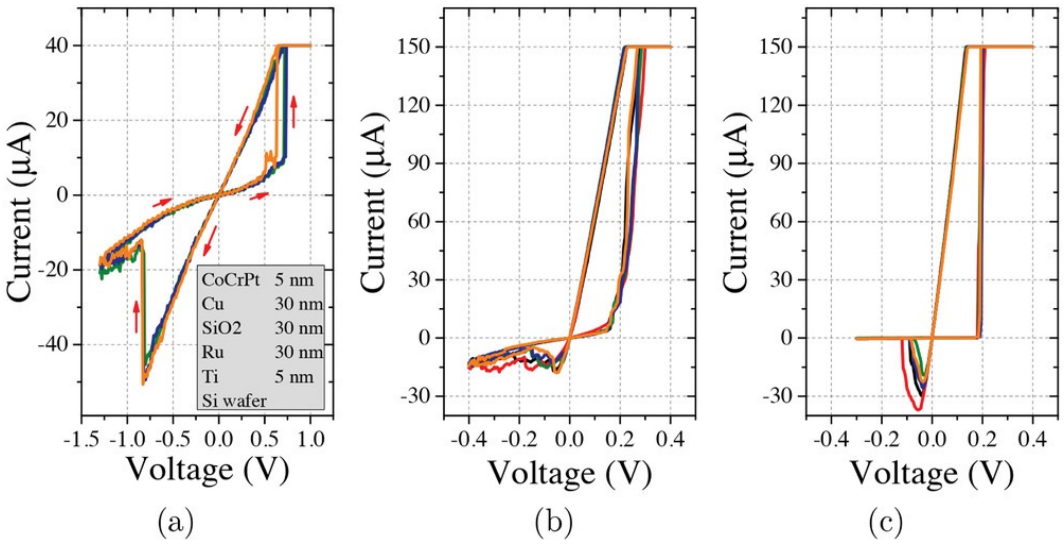

Figure 2.1 (a) Current-voltage characteristics of Cu-SiO_2 cell for several cycles of the voltage sweep 0 V to +1 V to -1.3 V to 0 V at the compliance current of 40 μA. (b), (c) Current-voltage characteristics of Knowm BS-AF-W and M+SDC Cr with the compliance current of 150 μA. From [63].

for the Cu-SiO_2 device was done under the voltage application from 0 to +1 V to -1.3 V and back to 0 for one complete cycle. Also, the compliance current of 40μA was used in order to prevent the potential damage to the device by Joule heating. Fig. 2.1(a) shows several voltage sweeps obtained with selected the Cu-SiO_2 device. This device exhibits a bipolar hysteresis loop twisted at the origin with well-defined threshold voltages. From the current-voltage plot, the following values are estimated: $R_{ON} \simeq 19.5$ kΩ, $R_{OFF} \simeq 150$ kΩ, $V_{th,+} \simeq 0.7$ V, and $V_{th,-} \simeq -0.8$ V (note: $V_{th,+}$ and $V_{th,-}$ are threshold voltages).

Next, Fig. 2.1(b) and (c) demonstrate I-V characteristics of Knowm BS-AF-W and M+SDC Cr cells, respectively. Their operation mechanism is based on the drift of Ag atoms through a stack of chalcogenide layers with Ge_2Se_3 layers doped either by W (BS-AF-W device) or Cr (M+SDC Cr device). These measurements were performed at the compliance current of 150 μA. The resultant curves show typical hysteresis behavior with thresholds, whose values can be approximately identified as

$V_{th,+} \simeq 0.2$ V, and $V_{th,-} \simeq -1.0$ V.

Consequently, the response of all devices is typical to bipolar ReRAM cells. We conclude that the selected devices function properly and can be used in the ideal memristor test.

2.4 Ideal memristor test

Here we describe the application of the ideal memristor test, whose purpose is to evaluate whether the device under test is an ideal memristor or not. For the test, a particular measurement procedure is required. The main experimental circuit is inspired by the ideal memristor test suggested by Pershin *et al.* [59]. The schematics of the test is illustrated in Fig. 2.2(a). The circuit consists of the device under test (indicated by the symbol of memristor), in-series connected capacitor (non-polarized 10 μF), and relay (part number HI05-1A66, Standex-Meder Electronics). By closing the relay, the capacitor is shunted so that the source measure unit (whose output is $V(t)$; Keysight B2911A) is connected directly to the device under test. In this configuration, the device under test can be initialized or its state can be recorded.

2.4.1 Cu-SiO_2 devices

In the test, the compliance current of 40 μA was used. To perform the test, the relay was opened so that the voltage source was connected to DUT through the capacitor. A triangular voltage pulse (Fig. 2.2(b)) with the amplitude of $V_0 = 0.4$ V or $V_0 = 1.0$ V was applied. After the pulse, a waiting period was introduced to ensure that the initial charge and final charge on the capacitor are the same (as required by the test procedure). Two measurements were performed in series, so that the final state after the application of $V_0 = 0.4$ V served as the initial state for the measurement with $V_0 = 1.0$ V. The initial and final resistances were measured in each test in the series.

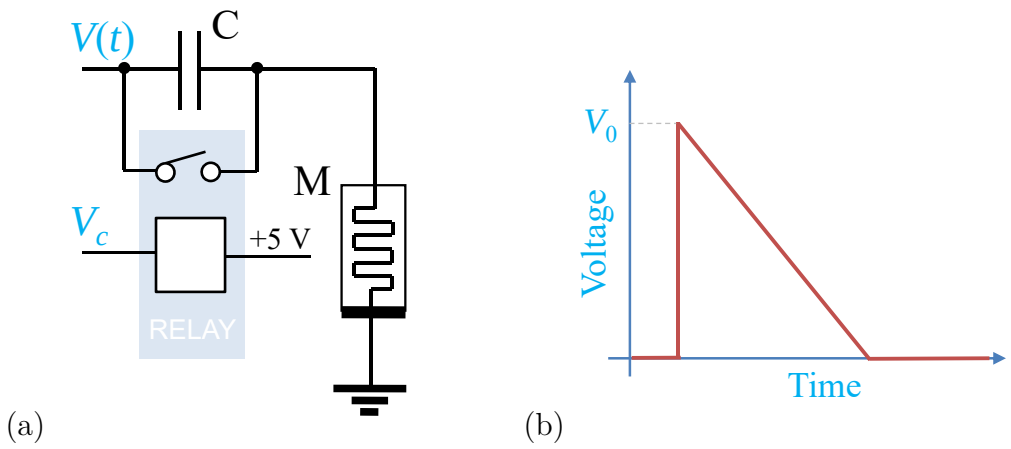

Figure 2.2 (a) Capacitor-resistive memory circuit employed in the experiment. Here, a relay is used to shunt the capacitor, C, to initialize and read the state of DUT denoted by M. (b) Triangular shape of the testing voltage $V(t)$ employed in the present work. From [63].

Fig. 2.3 shows the first test sequence performed with $V_0 = 0.4$ V. The slope of a fitting line in Fig. 2.3(a) represents the initial resistance, $R_{M,i} = 53$ kΩ. Next, we applied the test voltage of $V_0 = 0.4$ V as shown in Fig. 2.3(b). It is observed that it took $t \approx 13.5$ s for the capacitor to discharge. Then, the final resistance $R_{M,f}$ is obtained from the fitting line in Fig. 2.3(c). It is found that the final resistance is not different from the initial one, $R_{M,f} = R_{M,i} = 53$ kΩ. This corresponds to the required (but not necessary) condition for the device under test to be an *ideal* memristor.

Fig. 2.4 shows the second test sequence performed with $V_0 = 1$ V. Here, the measurement of the final resistance gave an interesting result. Fig. 2.4(a) presents the initial resistance (also it is the final state from the first measurement with $V_0 = 0.4$ V) $R_{M,i} = 53$ kΩ. The memristor test at $V_0 = 1.0$ V is shown in Fig. 2.4(b). In this test, the length of triangular pulse was longer, $t \approx 26$ s. It is found that the final resistance is significantly lower than the initial one, $R_{M,f} = 19.5$ kΩ. Therefore, it is concluded that Cu-SiO_2 ECM device has not passed the ideal memristor test.

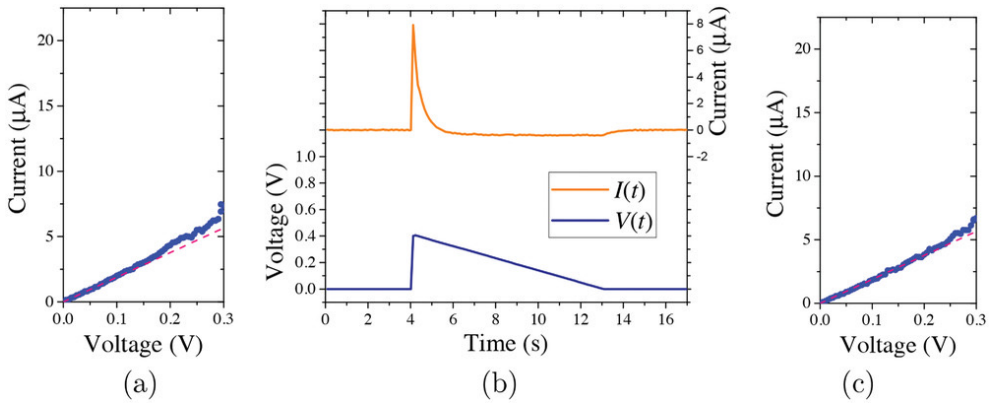

Figure 2.3 Experimental application of the ideal memristor test with $V_0 = 0.4$ V. (a) Measurement of the initial memristance with a closed relay. (b) Applied voltage (blue curve) and measured current (orange curve) versus time. The relay was open during this step. (c) Measurement of the final state. The fitting lines in (a) and (c) resulted in the same memristance $R_M = 53$ kΩ. From [63].

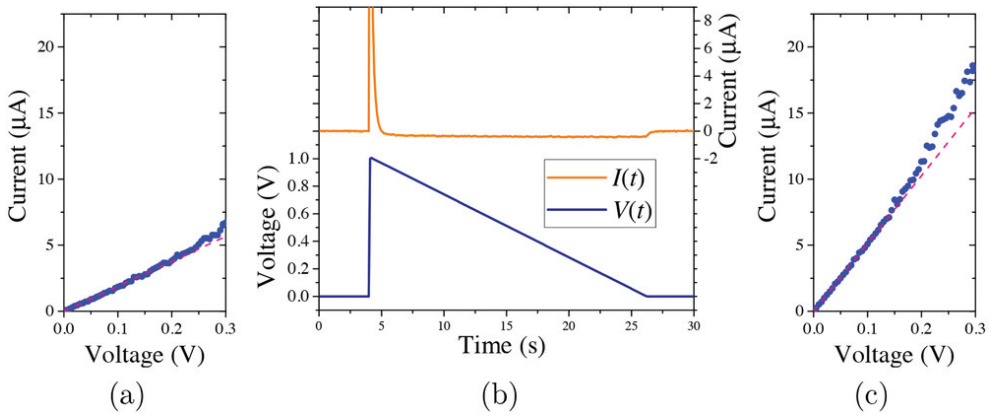

Figure 2.4 Experimental application of the ideal memristor test with $V_0 = 1.0$ V. (a) Measurement of the initial memristance with a closed relay. (b) Applied voltage (blue curve) and measured current (orange curve) versus time. The relay was open during this step. (c) Measurement of the final state. The fitting lines in (a) and (c) indicated different memristances in the initial, $R_{M,i} = 53$ kΩ, and final, $R_{M,f} = 19.5$ Ω, states. From [63].

2.4.2 Commercial devices

The ideal memristor test was applied to the commercial devices using a smaller capacitor $C = 1$ μF due to their higher resistance in the OFF state, $R_{OFF} \simeq 500$ kΩ.

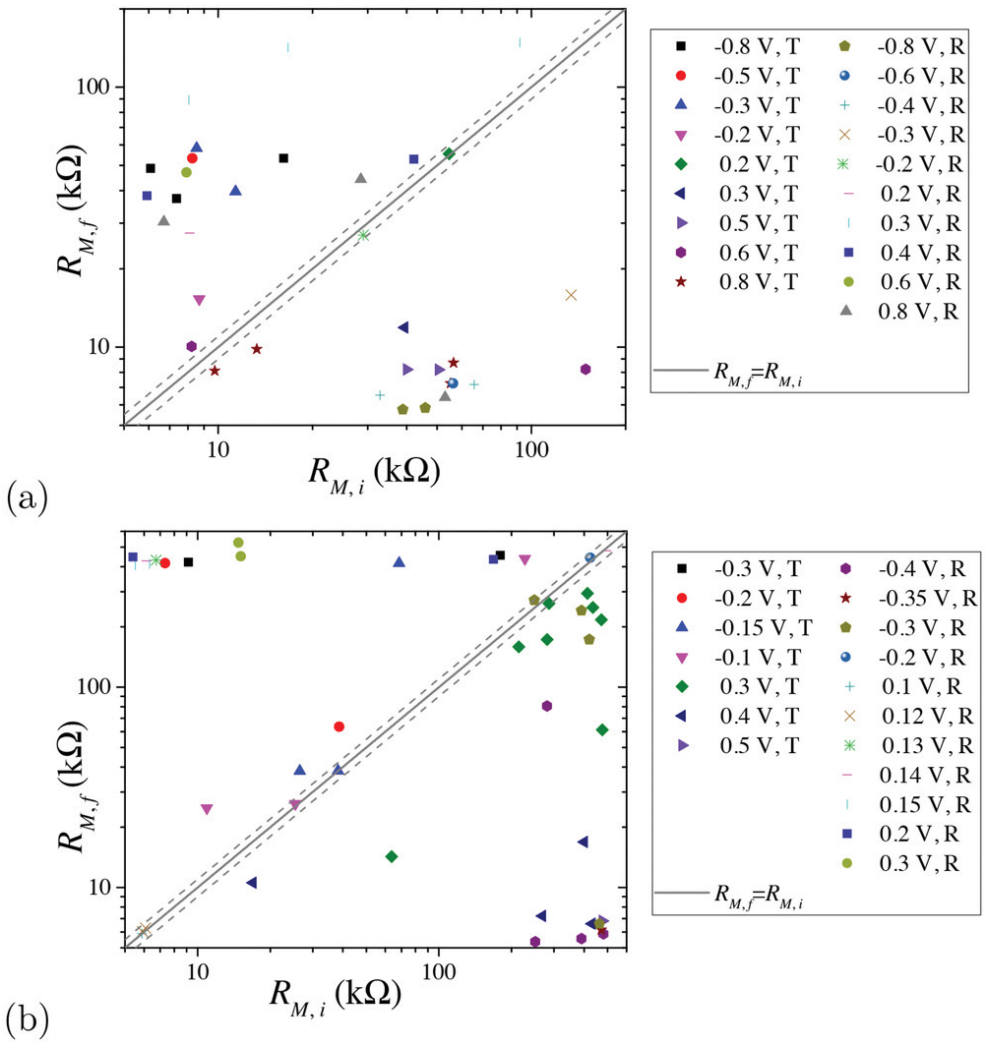

Figure 2.5 Results of the memristor test: Final memristance $R_{M,f}$ versus initial memristance $R_{M,i}$. In the legend boxes, **T** indicates the triangular applied pulse and **R** indicates the rectangular applied pulse. (a) Results for BS-AF-W cell. (b) Results for M+SDC Cr cell. From [63].

The major difference from the tests with Cu-SiO_2 cell is the use of a variety of widths and shapes of voltage pulses. In particular, the triangular pulse (like in Fig. 2.2(b)) with the slope of 0.025 V s^{-1} and rectangular pulse (like in Fig. 1.11(b)) with the width of 2 s of positive and negative polarities were used in an arbitrary order. More than thirty test sequences were applied to each BS-AF-W sample and M+SDC Cr sample and the waiting time in between each measurement was ≥ 3 s.

Fig. 2.5 presents the plots of the final resistance versus initial resistance found in the memristor tests with a BS-AF-W cell (Fig. 2.5(a)) and M+SDC Cr cell (Fig. 2.5(b)). In these plots, the final memristance, $R_{M,f}$, is plotted in the vertical direction, while the initial memristance,$R_{M,i}$, – in the horizontal one. The data points along the diagonal line represent the identical initial and final states, $R_{M,f} = R_{M,i}$ (the case of memristor). The dashed lines indicate 10% deviation, which can be considered as the acceptance interval. The resultant plots from both BS-AF-W and M+SDC Cr devices show that most of the data points are located outside of the dashed line interval. This indicates that these devices have not passed the test.

Chapter 3

Test application to Φ-memristor

3.1 Experiment description and goals

In order to prove that the Φ-memristor is a memristor, the following fundamental memristor relation should be verified [59]

$$V_M(t) = R_M I(t), \tag{3.1}$$

where

$$R_M = R(q). \tag{3.2}$$

Eq. (3.2) indicates that the memristance of the device R_M depends *only* on the charge q has flown through the device. Wang *et al.* [18] claimed that the Φ memristor is a new type of *ideal* memristor. In this chapter, the memristor test [59][63] is applied to the in-house fabricated Φ-memristor in order to determine whether this device is real memristor.

3.2 Device fabrication

To perform the memristor test suggested in Ref. [59] on the 'Φ memristor', the sample was fabricated according to the procedure specified in Ref. [18]. One lot of ferrite cores (made by VEB Elektronik Gera. German Democratic Republic in early 1980s) are used to form magnetic cores. Scanning electron microscopy (SEM) imaging method and energy dispersive X-ray (EDS) analysis were carried out using a TESCAN Vega-3 scanning electron microscope at the Electron Microscopy Center at the University

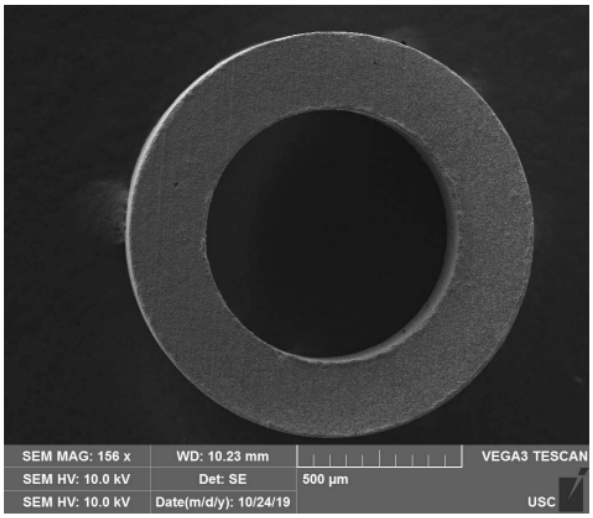

Figure 3.1 Scanning electron microscopy (SEM) image of the magnetic core. [64]

of South Carolina. The SEM image of the core is presented in Fig. 3.1. The EDS analysis was applied to three different points on the surface of the core with 4.5 kV accelerating voltage. The results of analysis demonstrate that the composition of the core includes ferrite doped by Mg and Mn atoms.

The physical design of the Φ memristor was slightly modified to increase the coupling between the magnetic core and current-carrying wire. An additional pick-up coil was added. 0.1 mm thin enameled copper wire was used for coils and two coils, where three loops around the magnetic core. The magnetization reversal is manifested as voltage peaks across the pick-up coil. The polarity of peaks indicates the direction of reversal.

3.3 Ideal memristor test

The electronic circuit for the memristor test is presented in Fig. 3.2. The pulse generator (Siglent SDG1025) generates voltage waveforms that are amplified by amplifier (HP 467A). The Φ-memristor is connected to the amplifier with a current-limiting resistor (47Ω) to limit the current. As the current-limiting resistor R is connected

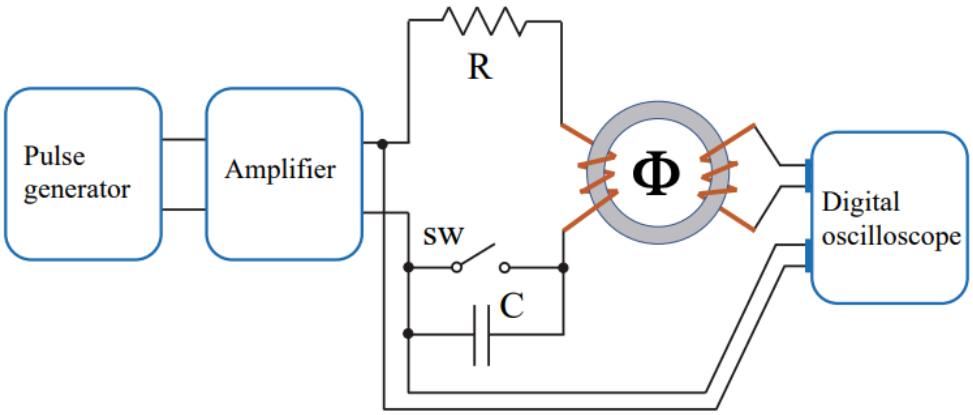

Figure 3.2 Experimental circuit setup for the test of Φ memristor. From [64]

in-series, it does not open any additional charge/discharge channels for the capacitor. Therefore, the duality property between the memristor state and capacitor charge is conserved. The capacitor (0.2 μF) is connected with a switch (labeled as SW in Fig. 3.2), so the capacitor can be shunted in some measurements.

Before running the memristor test, the functionality of the Φ-memristor was verified. The circuit in Fig. 3.2 with a shunted capacitor was driven by a sawtooth waveform of $V_0 = 10$ V amplitude and frequency $f = 50$ kHz as presented in Fig. 3.3(a) (see the green triangular waves). The red curve indicates the voltage across the pick-up coil; the magnetization reversal events correspond to the positive and negative voltage peaks. Such behavior confirms that the fabricated Φ memristor has typical response characteristics of similar devices (as in Ref. [18]). From the observation of exhibition of the resultant peaks, our device can be used in the memristor test. In addition, it is found that at smaller voltage amplitudes ($V_0 \lesssim 4$ V) no voltage signal is observed across the pick-up coil (see Fig. 3.3(b)).

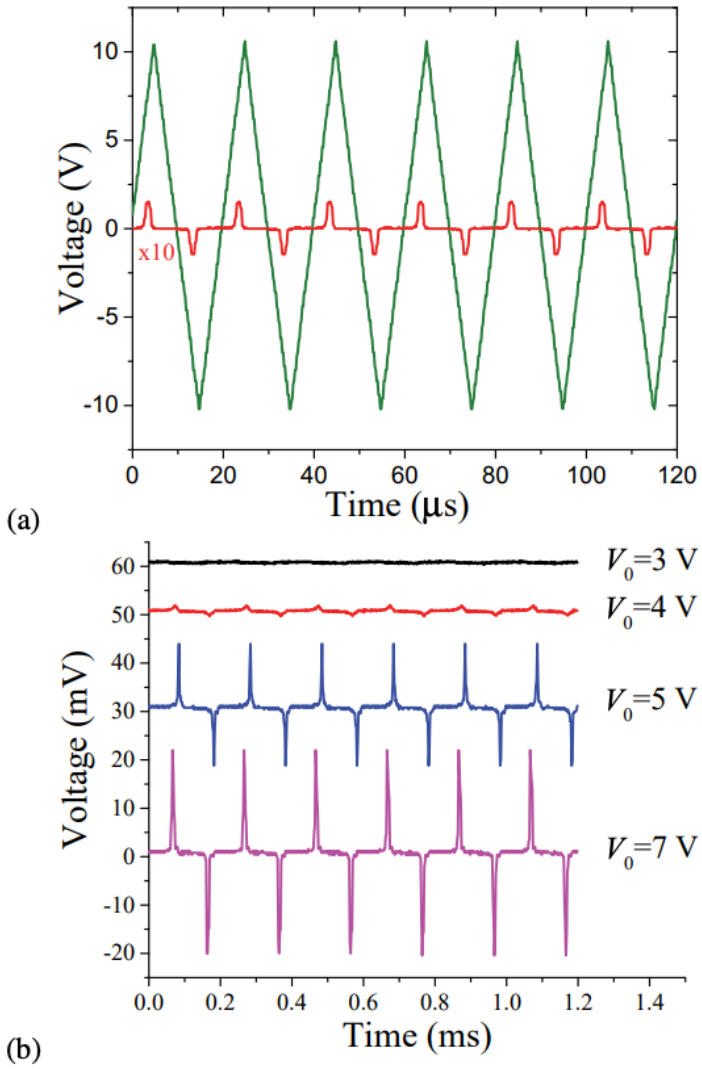

Figure 3.3 Characterization of the response of Φ-memristor. (a) Green peaks indicate the triangular voltage wave input with the amplitude of $V_0 = 10$ V and frequency of $f = 50$ kHz and the red peaks indicate the voltage across the pick-up coils. This measurement was performed in the circuit with a shunted capacitor. (b) Voltage across the pick-up coil for several different amplitudes, V_0, of a 5 kHz sinusoidal voltage waveform. The pick-up voltage increases with V_0. From [64].

3.4 Results

One may expect that the wire interacting with a magnetic core is an ideal memristor since the magnetic core has an internal state. The internal state variable of the core is its magnetization. We emphasize that at a constant applied voltage, the

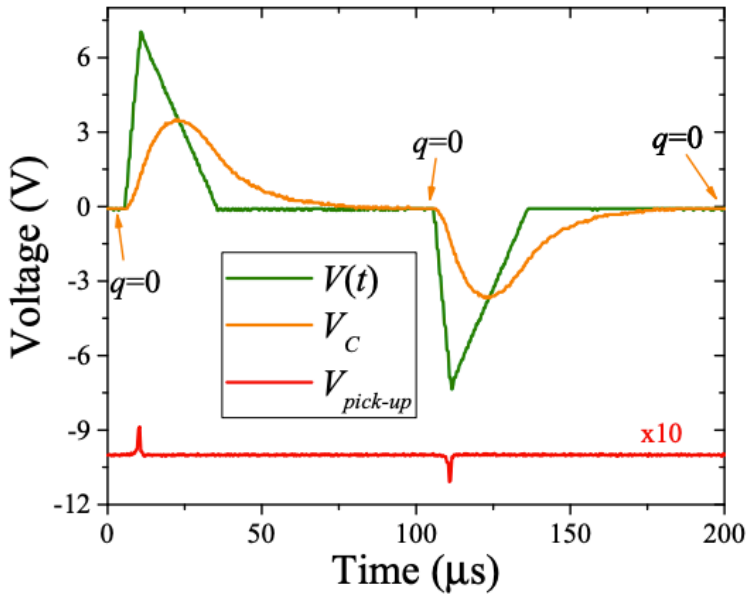

Figure 3.4 The memristor test to the 'Φ memristor' device. $V(t)$ is the applied voltage pulse, V_C is the voltage across the capacitor, and $V_{pick-up}$ curve is representing the resultant voltage across the pick-up coil. From. [64]

equilibrium resistance of the Φ-memristor is only defined by the wire resistance and does *not* depend on the core magnetization. This alone shows that the Φ-memristor is not a memristor. Despite this disqualification, the test is continued using the core magnetization as the internal state variable.

For the memristor test, the switch SW in Fig. 3.2 was opened. The measurement sequence is conducted with periodic asymmetric voltage pulses ($V(t)$ curves in Fig. 3.4) and each pulse (either positive or negative) initiates a single test. It is found that within a half cycle of the test sequence the voltage across the capacitor (V_C in a yellow curve in Fig. 3.4) returns to its initial value. This means that the capacitor is fully discharged before the initiation of an upcoming pulse. Consequently, the measurement is compatible with the required conditions for the memristor test. Hence, if the Φ-memristor is really a memristor then the core magnetization must return to its initial state before the next pulse (either negative or positive).

Meanwhile, the voltage across the pick-up coil ($V_{pick-up}$ in Fig. 3.4) shows a different behavior. The magnetization (as indicated by the peaks of $V_{pick-up}$) changes from one direction by a positive pulse and reverses to the opposite by the application of a negative pulse. Therefore, there is no duality between the state of the Φ-memristor and capacitor charge. Consequently, the Φ-memristor is not a memristor.

Chapter 4

Conclusion

In early seventies, the memristor was introduced theoretically as the forth fundamental circuit element using the relationship between flux linkage and charge. After a few decades, a group at Hewlett-Packard lab claimed that they found the missing *ideal* memristor. However, their arguments provoked discussions in the literature so that there was a need to further explore their validity. The structures that have been widely called as "memristors" have to be further inspected to see whether they indeed satisfy the *ideal* memristor definition – a well-defined mathematical relationship. In this thesis, several types of devices known in the literature as "memristors" were subjected to the memristor test, including home-fabricated devices (Cu-SiO_2 cells and Φ memristor) as well as commercially available devices. None of these devices has passed the test that, in the case of memristors, should lead to the same final state at the end of the test as the initial state. In multiple instances of the test, we have observed that the final states of memory devices deviate significantly from their initial states. Consequently, ECM cells and Φ-memristor do not work as they are supposed to work according to their name. The results of this study indicate that the devices under consideration are unambiguously **not** memristors, and cast further doubts on the physical existence of the fourth fundamental circuit element.

The results of this study have been published in Ref. [63]. Another research paper [64] has been submitted for publication.

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