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Ultrawide Bandgap Algan-Channel Metal Oxide Semiconductor Heterostructure Field Effect Transistors With High-*K* Gate Dielectrics

Md Abu Shahab Mollah

ULTRAWIDE BANDGAP ALGAN-CHANNEL METAL OXIDE SEMICONDUCTOR HETEROSTRUCTURE FIELD EFFECT TRANSISTORS WITH HIGH-*K* GATE DIELECTRICS

by

Md Abu Shahab Mollah

Bachelor of Science
Khulna University of Engineering and Technology, 2011

Master of Science
University of Alabama, 2017

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Accepted by:

Asif Khan, Major Professor

Grigory Simin, Major Professor

MVS Chandrashekhar, Committee Member

Milind N. Kunchur, Committee Member

Tracey L. Weldon, Interim Vice Provost and Dean of the Graduate School

DEDICATION

To my Family

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ABSTRACT

Ultra-wide Band Gap (UWBG) (E_G > 3.4 eV) $Al_xGa_{1-x}N$ channel devices are promising candidates for compact next-generation power electronics due to the scaling of the breakdown field with alloy composition. The huge opportunity in consumer electronics is the major driving force behind the recent developments of UWBG AlGaN-channel HEMTs. One of the most critical issues limiting the device performance at high power level is device degradation primarily caused by gate leakage current. Use of SiO_2 gate insulator is a standard method to suppress gate leakage but it causes threshold voltage shift towards more negative requiring more external voltage to turn off the device. The threshold shift becomes significant with the increase of oxide thickness which is not desired in many power electronics application. One potential solution to both gate leakage and threshold shift issue is the use of high-*k* dielectric as a gate insulator. It has been seen that, these high-*k* oxides also introduce charges in the oxide and oxide/barrier interface which are positive in nature, thus shifting the threshold voltage to practically un-usable range. The threshold voltage is almost 2× for an oxide thickness of 20 nm compared to similar geometry HFET (no oxide under the gate). In this dissertation we develop a novel processing technique to control the polarity of the interfacial charges that in return controls the threshold voltage. It was done by high temperature gate oxide annealing. To demonstrate the threshold shift mechanism, ZrO_2 MOSHFETs with different thicknesses were fabricated. Annealing enables excellent threshold voltage control thus minimizing the threshold voltage shift in these high-*k* MOSHFETs.

Gate insulators are expected to have higher bandgap (E_G) to superior leakage characteristics. Material bandgap is inversely proportional to the dielectric constant, so higher the k-value lower is the bandgap. To study the effect of E_G and *k* on UWBG AlGaN-channel MOSHFET performance, we choose three different dielectrics Al_2O_3 (k=9, E_G=8.8 eV), ZrO_2 (k=25, E_G = 5.8 eV) and TiO_2 (k=80, E_G=3.2 eV) with three distinct set of *k* and E_G values. Al_2O_3 with highest E_G shows lowest gate leakage while TiO_2 with lowest E_G shows highest leakage in these set of oxides. TiO_2 and ZrO_2 shows maximum positive threshold shift, while Al_2O_3 shows lower positive shift compared to others. High temperature operation of these devices shows promising results, thus making these MOSHFETs ideal candidate for next generation power electronics. To maximize both E_G and *k* value out of these materials we develop hybrid oxide stack by combining ZrO_2 and Al_2O_3.

The drain current density in typical depletion mode AlGaN-channel devices is well below 1 A/mm where for GaN-channel devices it is 1-2 A/mm. In this dissertation, incorporating the hybrid oxide with perforated channel geometry we fabricated depletion (D-) and enhancement (E-) mode $Al_{0.4}Ga_{0.6}N$-channel MOSHFETs. Perforated channel shows significant reduction in access resistance and hybrid oxide allows positive gate bias application as high as +12 V, that enable realization of drain current density of 1.3 A/mm and 0.48 A/mm respectively, for depletion and enhancement mode MOSHFETs while maintaining extremely low gate leakage. The superior device performance discussed in this dissertation demonstrates that UWBG AlGaN channel D- and E-mode devices are promising for power electronics.

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CHAPTER 1: INTRODUCTION AND BACKGROUND TECHNICAL INFORMATION

1.1 III-Nitride material properties:

Electronic products have become a major part of our daily lives. High electron mobility transistors (HEMTs) are tiny electronic switches that serves as cornerstone in many electronic products including computers, electric vehicles (EV's), cell-phones and 5G transmitters. One of the promising materials for the next generation power electronics are compound semiconductors formed from Group III metals and nitrogen (III-Nitrides). III-Nitrides are direct bandgap compound semiconductor material system that includes binary materials such as AlN, GaN, InN as well as their ternary and quaternary alloys. III-Nitride based switches have attracted attention due to their high-power handling capabilities for compact consumer electronic charging, III-Nitride based charger- which is designed for phones, tablets, laptops etc, the size is about half that of conventional chargers, while offering fast charging capabilities. Now III-Nitride devices are becoming major part of electric vehicle controls in modern transportation. Recently, a large number of hybrid and EV automakers are investing in III-Nitride technology that can enable higher power conversion efficiency, reduced system cost and weight compared to their traditional silicon counterparts. These materials are of wide interest due to the large range of available bandgaps ranging from 0.7 eV (InN) and 6.2 eV (AlN) [1][2]. The large range of available

bandgaps make these materials important for various applications ranging from optoelectronics, power electronics, and high frequency high power devices.

GaN, one of the most prominent materials from III-N group has already started making a remarkable impact in the area of power and RF electronics [3]. Over the last three decades, GaN based High Electron Mobility Transistors (HEMTs) have attracted intense research attention for high power and high frequency applications due to its attractive intrinsic material properties [4][5]. Lot of effort in both academia and industry is going on to utilize its full potential as high power and high frequency device. As a result, GaN-based RF power amplifiers are currently overtaking RF power amplifier market share. GaN is making an impact in the high-performance power electronics market as well, due to the low on-resistance and high breakdown voltages for GaN devices with smaller dimensions compared to Si devices, enabled by the higher critical breakdown field. These HEMTs work more reliably than Si in harsh environments, like temperatures beyond 300 °C, or in chemically non-inert environment which is belligerent to Si [6]. Accompanying this continuous effort, successful commercialization of GaN based HEMTs has already been started [6][7]. Among the semiconductors for which power devices are already available in the market, GaN has the widest energy gap, the largest critical field, and the highest saturation velocity, thus making it superior candidate for power electronics application [8]. Table 1.1 shows the comparison of different materials to design power semiconductor devices. SiC and GaN have large band gaps (E_G). These SiC and GaN are considered as wide bandgap materials. Wide bandgap results in very low intrinsic carrier concentration (n_i) following, $n_i = \sqrt{N_C N_V} e^{\frac{-E_G}{2KT}}$ [9]. Whereas Si based devices could not operate above ~200 ^oC efficiently, these wide bandgap materials ensure high temperature operations.

Table 1.1 shows that SiC and GaN both have higher critical electric fields (E_C) than Si. This is very crucial requirement for materials used in designing power semiconductor devices. Following equation shows the relation between material bandgap and critical electric field [4]

$$E_C = 1.73 \times 10^5 (E_G)^{2.5} \text{ (for direct band gap)} \qquad (1.1)$$

$$E_C = 2.38 \times 10^5 (E_G)^2 \text{ (for indirect band gap)} \qquad (1.2)$$

Breakdown voltage is one of the key metrics for power semiconductor devices that depends on critical electric field. Among the materials in Table 1.1, GaN has the highest critical electric field due to its large band gap (~3.4 eV). Compared to Si, the critical electric field is 10 times higher for GaN. This means that 10 times the voltage can be applied to GaN devices for a given device dimension compared to Si devices. If the device is switched on, the remaining on-state resistance R_{on} defines device losses at this condition. As the specific on resistance scales with the length of the device drift region to maintain a given breakdown voltage, the more compact GaN devices feature much lower on-resistance as possible with Si devices. Additionally, due to the electron transport properties of AlGaN/GaN HEMTs, the specific on-resistance is almost two orders of magnitude lower compared to Si power devices with the same voltage rating. Thus, GaN power devices demonstrate high breakdown voltage and high current density simultaneously and feature small semiconductor area.

Power switching devices based on different semiconductor materials are compared using their figure of merit (FOM). For vertical devices such as p-i-n diodes it is known as unipolar figure of merit (UFOM), often referred as Baliga figure of merit (BFOM) which

Table 1.1 Comparison of physical parameters of Epitaxial GaN layers as well as Bulk GaN crystals against Si and 4H-SiC at 300K

Properties	Si	4H-SiC	GaN (Epitaxial)	GaN (Bulk)
Bandgap, E_G (eV)	1.11 (indirect)	3.26 (indirect)	3.42 (direct)	3.42 (direct)
Intrinsic carrier concentration, n_i (cm^{-3})	1.5×10^{10}	5×10^{-9}	2×10^{-10}	--
Critical Electric Field, E_{crit} (MV/cm)	0.3	2.2	2	3.3
Relative dielectric constant, ε_r	11.9	10.1	9	9
Thermal Conductivity, k (W/K.cm)	1.5	4.9	1.3	2.3
Electron Mobility, μ_e(cm^2/Vs)	1350	900	1150 2000[a]	1150 2000[a]
Saturation velocity, V_{sat} (10^7 cm/s)	1	2	3	3
BFM_{Si}, $\varepsilon_r \mu_e E_{crit}^3$	1	223	190 330[a]	850 1480[a]
$BHFFM_{Si}$, $\mu_e E_{crit}^2$	1	45	36 63[a]	98 170[a]
$JFFM_{Si}$, $\frac{V_{sat}E_{crit}}{2}$	1	215	400	1090
Maximum estimated operation temperature, T_{max} (°C)	200	500	700	700

[a] Most of the GaN power devices realized today depends on the two-dimensional electron gas (2DEG) properties at the AlGaN/GaN interface, the 2DEG related data are presented with the letter a

can be derived based on the electric field versus the position curve shown in Figure 1.1. The area under the curve represents the breakdown voltage, V_{BR}, yielding $V_{BR} = \frac{E_C W_D}{2}$. Again, from Gauss' law, $\varepsilon E_C = qN_D W_D$. Combining these two equations the breakdown voltage can be expressed as, $V_{BR} = \frac{\varepsilon E_C^2}{2qN_D}$. Assuming that electron transport is due to drift only (hence the name "unipolar"), the resistance of the drift region times its area (termed the "specific on-resistance" with units of Ω-cm^2)is $R_{on-sp} = \frac{W_D}{q\mu_n N_D}$ where Ron-sp represents the specific on-resistance and μ_n is the bulk mobility in the drift region. Hence, the Baliga figure of merit, [10]

$$BFOM = \frac{V_{BR}^2}{R_{on-sp}} = \frac{\varepsilon \mu_n E_C^3}{4} \qquad (1.3)$$

This formula is applicable for vertical devices as it is derived using the vertical device geometry. However, for lateral devices a similar formula can be derived using lateral device geometry shown in Figure 1.2 that is known as the lateral FOM (LFOM) [11]. The top portion of the figure depicts the electric field profile between the gate and drain of the device (separated by a distance *L*), which is the region that supports the blocking voltage and is analogous to Figure 1.1. In this case, the electric field is uniform in position rather than a linear function of it. This is an idealization and in real devices the electric field tends to peak near the drain-side edge of the gate, although structures such as field plates are intended to make the field as uniform as possible. Thus, the profile shown is the optimum case. The bottom position of Figure 1.2 indicates a sheet density of electrons n_s (unit cm^{-2}) in the channel of the device, which flow parallel to the surface of the device, along the channel of length *L* (mentioned above) and width *W*. The key difference here compared to the vertical geometry described above is that the current

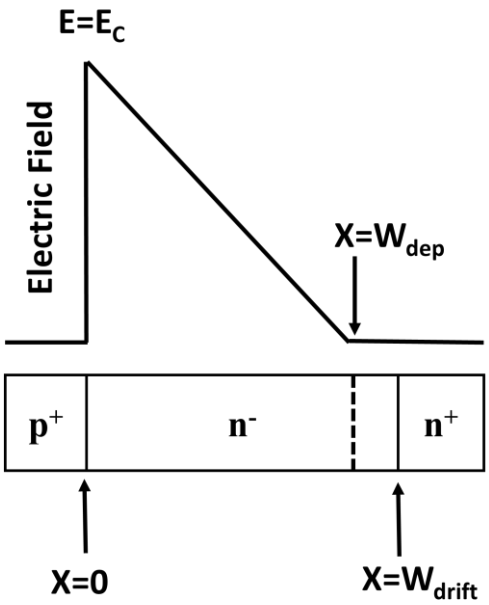


Figure 1.1 Plot of electric field vs position for a one-sided, uniformly doped junction, from which the definition of critical electric field is derived.

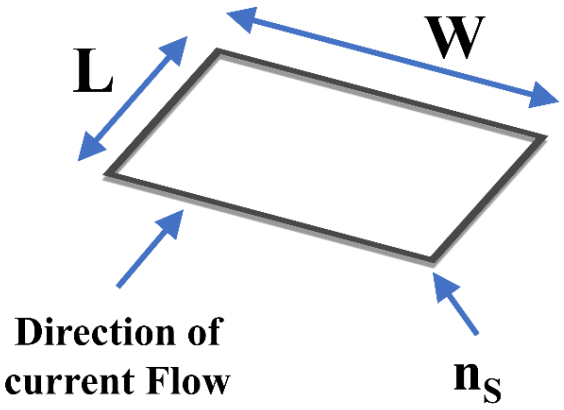


Figure 1.2 Geometry used for derivation of LFOM

direction is parallel to the cross-sectional area of the device LW rather than perpendicular to it as is the case for the vertical geometry. Based on the configuration depicted in Figure 1.2, the breakdown voltage is seen to be $V_B = E_C L$. Further, the specific on-resistance is given by $R_{on,sp} = L^2/q\mu_{ch}n_s$. Here, μ_{ch} is the *channel* mobility, which may not be the same as the bulk mobility. Combining these two expressions yields the expression for the LFOM

$$LFOM = \frac{V_{BR}^2}{R_{on-sp}} = qn_s\mu_{ch}E_C^2 \qquad (1.4)$$

In the power switching field, it is common to compare Si, SiC, GaN, AlN, and $Al_xGa_{1-x}N$ alloys even though Si and SiC are vertical devices and the III-N materials can be either lateral or vertical.

While noteworthy progress has been achieved in GaN electronics over the past two decades, for the research community it is high time to look for material systems that can overcome the limitations of GaN in terms of performance and power efficiency. Ultrawide-bandgap (UWBG) semiconductor materials ($E_G > 3.4\ eV$) such as AlGaN/AlN, diamond, Ga_2O_3, cubic BN etc are now materials of interest to the community. The AlGaN Alloys have very good fundamental physical properties. They have direct bandgap significantly wider bandgap (3.4 to 6.2 eV) than the 3.4 eV of GaN, high breakdown fields (>10 MV/cm for AlN), high electron mobility (bulk mobilities up to 1000 cm^2/V-s) and high saturation velocity (>10^7 cm s^{-1}) [12]. As seen from the BFOM and LFOM expressions, the device performance scale with increasing bandgap in a highly nonlinear manner, UWBG AlGaN materials have potential for superior performance than conventional WBG materials. Baca et. al presented that, Under the assumption n_s~1×10^{13} cm^{-2}, the room temperature LFOM is larger than GaN BFOM and both LFOM and BFOMs are larger than SiC BFOM (Figure

1.3 (a)) [10]. The trend is similar for other practical choices of n_s. However, the room temperature FOMs for $Al_xGa_{1-x}N$ alloys are smaller than GaN's for x < 0.5 for the BFOM and for x < 0.8 for the LFOM. Figure 1.3 (a) also shows that the BFOM is favored over the LFOM at x > 0.5. The FOM analysis favors the $Al_xGa_{1-x}N$ alloys at all compositions at 500 °C, as illustrated in Figure 1.3 (b). Both the lateral and vertical device FOMs are greater than those for GaN. In addition, both the BFOM and LFOM are better that the 25 °C BFOM for SiC. The true potential for HEMTs based on the $Al_xGa_{1-x}N$ alloys lies in the high Al-content compositions of x > 0.8 at room temperature or at all x for 500 °C.

The above discussion shows the potential of Ultra-wide Band Gap (UWBG) (E_G > 3.4 eV) $Al_xGa_{1-x}N$ channel devices for compact next-generation power electronics [12][13]. The huge opportunity in consumer electronics is the major driving force behind the recent developments of UWBG AlGaN-channel HEMTs.

1.2 Polarization Induced 2-D Electron Gas in III-Nitride material system:

One of the unique features of III-nitride system is its polarization effect as a consequence of the non-centrosymmetry of its wurtzite structure and the high degree of ionicity of the covalent metal-nitrogen bonds. Experimental and theoretical investigations have shown that macroscopic polarization effect have great influence on the characteristics, performance, and response of nitride heterostructure devices grown on c-plane.

Figure 1.4 Shows the wurtzite crystal structure of Ga and N- face GaN. In the absence of external electric fields, the total macroscopic polarization P of a GaN or AlGaN layer is the sum of the spontaneous polarization P_{SP} in the equilibrium lattice, and the strain induced or piezoelectric polarization P_{PE}. As the spontaneous polarization depends on the

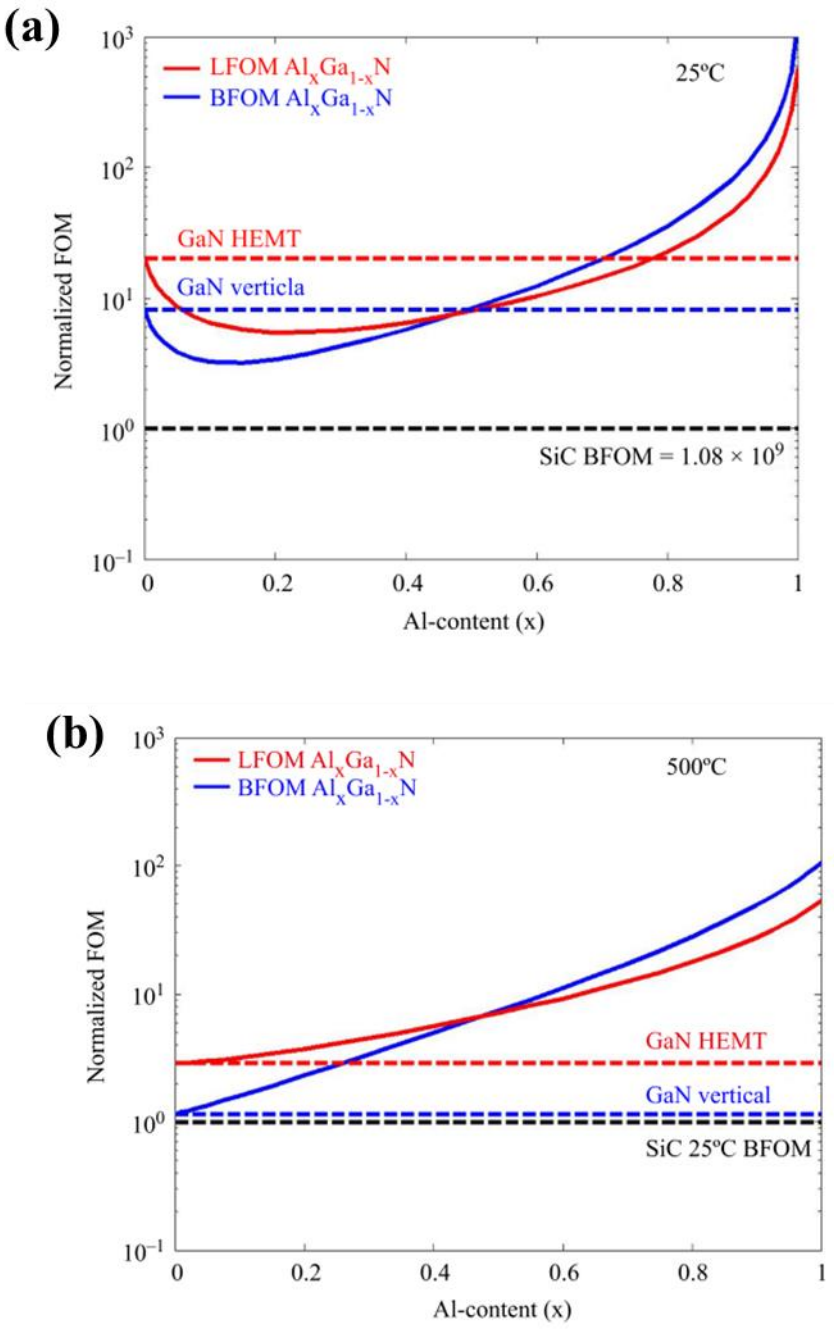


Figure 1.3 (a)Room temperature LFOM and BFOM versus Al content for AlGaN-channel HEMTs, normalized to the 25 °C SiC BFOM value [10]. (b) 500 °C LFOM and BFOM versus Al content for AlGaN-channel HEMTs, normalized to the 25 °C SiC BFOM value [10].

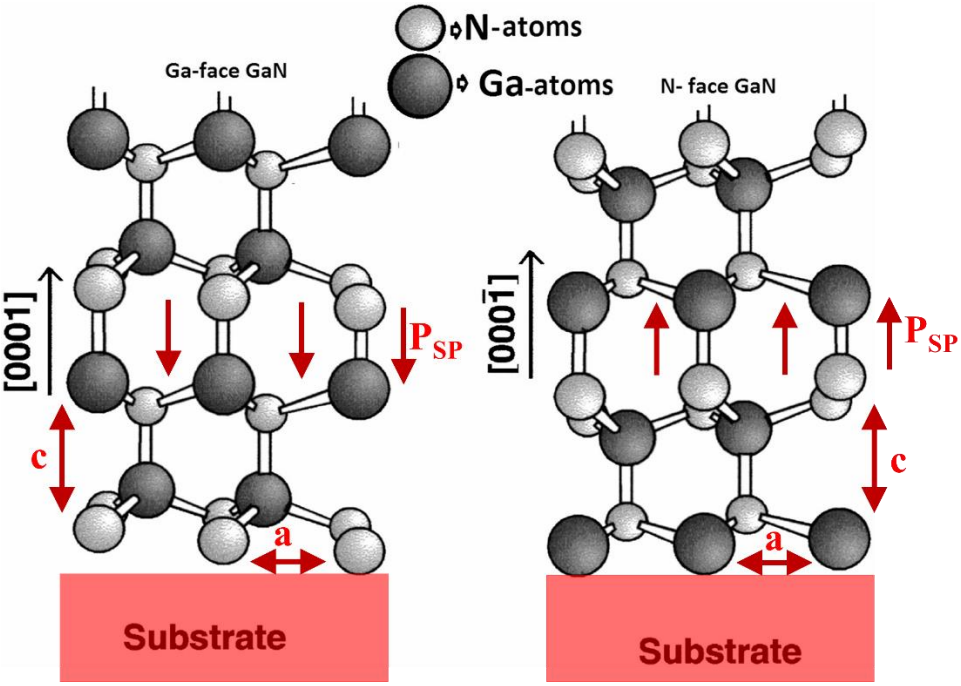


Figure 1.4 Atomic orientation of the wurtzite Ga and N-face GaN

structural parameters, there are some quantitative differences in the polarization of GaN and AlN. The increasing nonideality of the crystal structure going from GaN to AlN corresponds to an increase in spontaneous polarization. Polarizations are considered in [0001] directions, since this is the direction along which epitaxial films and AlGaN/GaN heterostructures are grown. The spontaneous polarization along the c-axis of the wurtzite crystal is $\boldsymbol{P_{SP}} = P_{SP}\mathbf{z}$. The piezoelectric polarization can be calculated with the piezoelectric coefficients e_{33} and e_{31} as [14],

$$P_{PE} = e_{33}\boldsymbol{\varepsilon}_z + e_{31}\left(\boldsymbol{\varepsilon}_x + \boldsymbol{\varepsilon}_y\right) \qquad (1.5)$$

where a_0 and c_0 are the equilibrium values of the lattice parameters, $\boldsymbol{\varepsilon}_z = \frac{c-c_0}{c_0}$ is the strain along the *c*-axis, and the in-plane strain $\boldsymbol{\varepsilon}_x = \boldsymbol{\varepsilon}_y = \frac{a-a_0}{a_0}$ is assumed to be isotropic. The relation between the lattice constants of the hexagonal GaN is given by,

$$\frac{c-c_0}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{a-a_0}{a_0} \qquad (1.6)$$

where C_{13} and C_{33} are elastic constants. Using the equations (1) and (2), the amount the amount of piezoelectric polarization in the c-axis can be determined by,

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad (1.7)$$

For any composition of AlGaN, the part $\left[\ e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right]$ <0, thus the piezoelectric polarization is negative for tensile and positive for compressive strained barriers, respectively. The spontaneous polarization for GaN and AlN is negative, meaning that for Ga-face heterostructures the spontaneous polarization is pointing towards the substrate. As a result, the alignment of the piezoelectrical and spontaneous polarization is parallel in the

case of tensile strain, and antiparallel in the case of compressively strained top layers. If the polarity flips over from Ga-face to N-face material, the piezoelectric, as well as the spontaneous polarization changes its sign. At the interface of a top/bottom layer (AlGaN/GaN or GaN/AlGaN) heterostructure the total polarization charge can decrease or increase within a bilayer, causing a polarization sheet charge density defined by,

$$\sigma = P_{top} - P_{bottom}$$

$$= \{P_{SP,top} + P_{PE,top}\} - \{P_{SP,bottom} + P_{SP,bottom}\} \quad (1.8)$$

If the polarization induced sheet charge density is positive ($+\sigma$), it will attract equal number of free electrons to compensate the polarization induced charge in order to maintain the charge neutrality. These electrons will form a 2DEG with a sheet carrier concentration n_S. A negative sheet charge density ($-\sigma$) will cause an accumulation of holes at the interface.

Figure 1.5 shows six different possible combinations of spontaneous and piezoelectric polarization for Ga and N-face AlGaN/GaN structure. For a Ga-face AlGaN on top of GaN heterostructure, the polarization induced sheet charge is positive. Even if the heterostructure is relaxed (AlGaN thickness >> 65 nm), electrons will be confined at the interface because of the difference in spontaneous polarization of GaN and AlGaN. If this heterostructure is grown pseudomorphic（Figure 1.5 (b)) the piezoelectric polarization of the tensile strained AlGaN barrier will increase the difference P_{AlGaN} - P_{GaN}, so as the sheet charge + σ and the sheet carrier concentration n_S. For N-face AlGaN/GaN heterostructures, the spontaneous and piezoelectric polarization have opposite directions

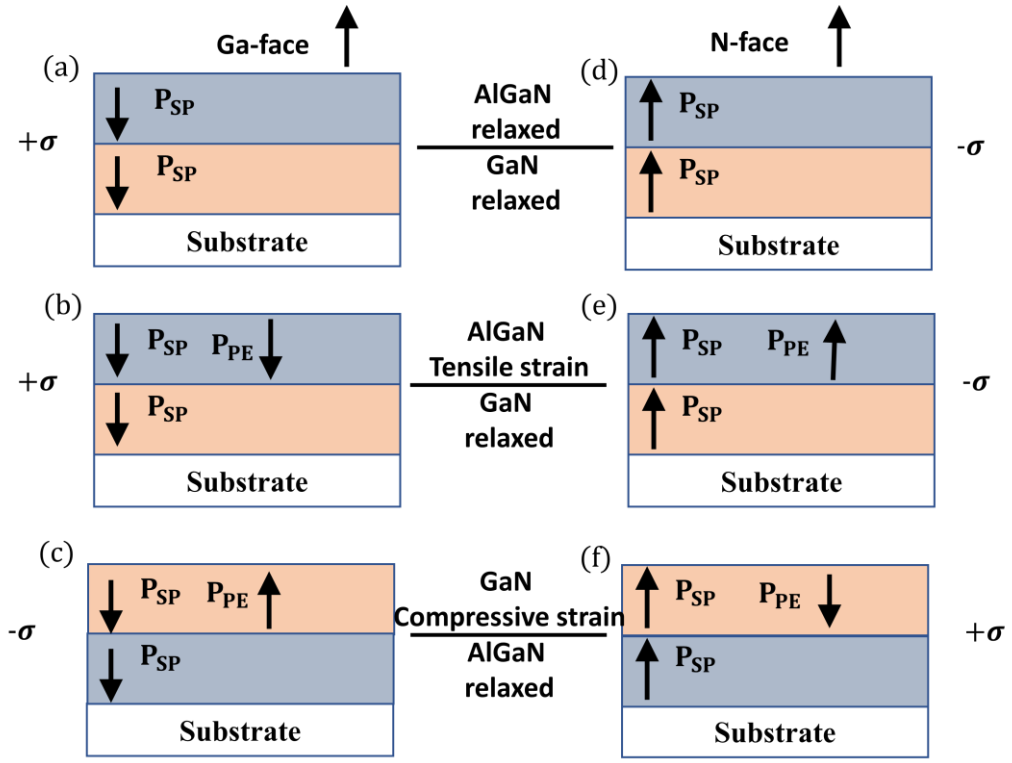


Figure 1.5 Polarization induced sheet charge density and direction of spontaneous and piezoelectric polarizations in strained and relaxed Ga and N- face AlGaN/GaN epilayers.

in comparison to the Ga-face structure. The polarization induced sheet charge is negative, and holes can be accumulated at this interface （Figure 1.5 (d) and (e)). In N-face heterostructures, electrons will be confined if GaN is grown on top of AlGaN, due to the positive sheet charge which will be formed in this case Figure 1.5 (f). The amount of polarization induced sheet charge density at the AlGaN/GaN interface for any x value of $Al_xGa_{1-x}N$ can be estimated using the following formulas:

Lattice constant:

$$a(x) = 3.189 - 0.077x \text{ (Å)}, \tag{1.9}$$

Elastic constants:

$$C_{13}(x) = (5x + 103)\ GPa, \tag{1.10}$$

$$C_{33}(x) = (-32x + 405)\ GPa, \tag{1.11}$$

Piezoelectric constants:

$$e_{31}(x) = (-0.11x - 0.49)\frac{C}{m^2}, \tag{1.12}$$

$$e_{33}(x) = (0.73x + 0.73)\frac{C}{m^2} \tag{1.13}$$

Spontaneous polarization:

$$P_{SP}(x) = (-0.052x - 0.029)\frac{C}{m^2} \tag{1.14}$$

The total polarization induced sheet charge density in an undoped pseudomorphic N-face GaN/AlGaN/GaN heterostructure can be estimated using the above equations:

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)|$$

$$|\sigma(x)| = \left|2\frac{a(0)-a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} + P_{SP}(x) - P_{SP}(0)\right| \qquad (1.15)$$

1.3 Sheet carrier concentration and mobility in AlGaN/GaN heterostructure:

Based on the above discussion, a charge distribution profile of an AlGaN/GaN heterostructure is presented in Figure 1.6, where $\pm\sigma_{AlGaN}$ is the $Al_xGa_{1-x}N$ polarization induced charge, $\pm\sigma_{GaN}$ is the GaN polarization induced charge. Beside these two dipoles, another dipole is present in the structure which is due to the 2DEG and ionized surface charge σ_S. These three dipoles are equivalent to three planar plate capacitors C_1, C_2 and C_3 respectively. Each of these capacitors has nonzero electric field between its two parallel planes and has no effect on electrons outside its inner body. The internal electric field intensity of a planar plate capacitor is given by $E = \sigma/\varepsilon$, where σ is the number of total charges on opposite planes, ε is the dielectric constant of the dielectric medium of the capacitor. In the area where two or more pairs of charged planes overlap, the total electric field is the algebraic sum of individual electric fields. Thus, the net electric field in the AlGaN layer is determined by the electric fields across C_1 and C_2, i.e., the sum of electric fields due to AlGaN polarization-induced charge and the 2DEG [15]:

$$\frac{\Delta V_{AlGaN}(x)}{d} = \frac{\sigma_{AlGaN}(x)}{\varepsilon(x)} - \frac{qn_S(x)}{\varepsilon(x)} \qquad (1.16)$$

where ΔV_{AlGaN} is the potential drop across the conduction band of the $Al_xGa_{1-x}N$ surface and the AlGaN/GaN interface, d is the thickness of AlGaN layer, σ_{AlGaN} is the polarization-induced charge in the $Al_xGa_{1-x}N$ layer, n_S is the sheet charge density of the 2DEG, q is the electron charge and ε is the dielectric constant of the $Al_xGa_{1-x}N$ layer. As seen from the band diagram (Figure 1.6), the potential drop can be expressed as

$$\Delta V_{AlGaN}(x) = q\varphi_b(x) + E_F(x) - \Delta E_C(x) \qquad (1.17)$$

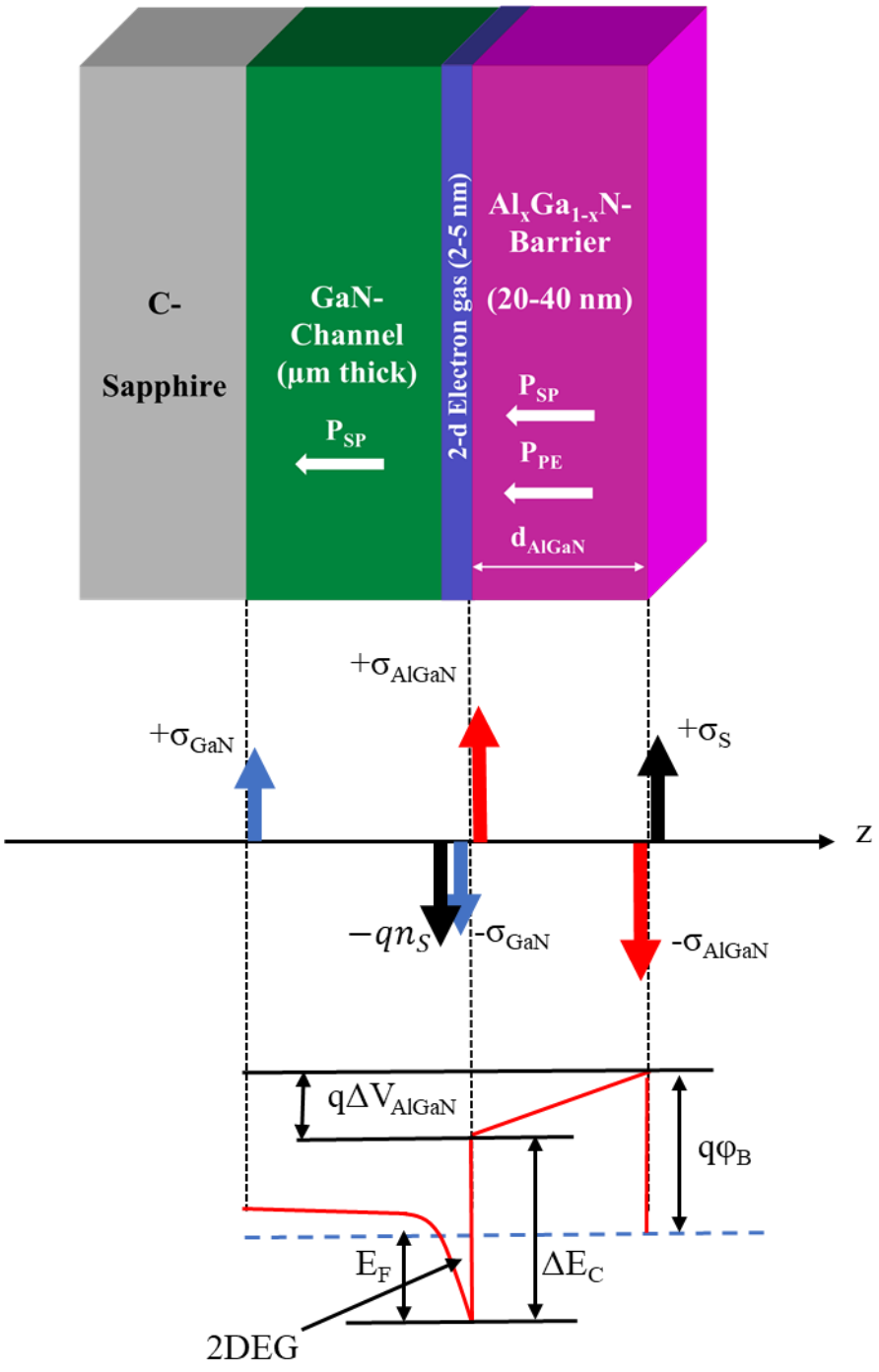


Figure 1.6 Charge distribution profile of a AlGaN/GaN heterostructure and corresponding conduction band diagram.

where φ_b is the surface barrier height, E_F is the Fermi level position with respect to the GaN conduction band edge at the AlGaN/GaN interface and ΔE_C is the conduction band discontinuity between GaN and AlGaN at the interface. Based on equations (1.16) and (1.17), the 2DEG sheet charge density can be expressed as,

$$n_S(x) = \frac{\sigma_{AlGaN}(x)}{q} - \frac{\varepsilon(x)}{qd^2}\left(q\varphi_b(x) + E_F(x) - \Delta E_C(x)\right) \qquad (1.18)$$

Figure 1.7 shows typical 2DEG density as a function of the $Al_xGa_{1-x}N$ barrier thickness for x=0.35. The 2DEG starts forming at a barrier thickness of ~ 25 Å and saturates at ~ 250 Å.

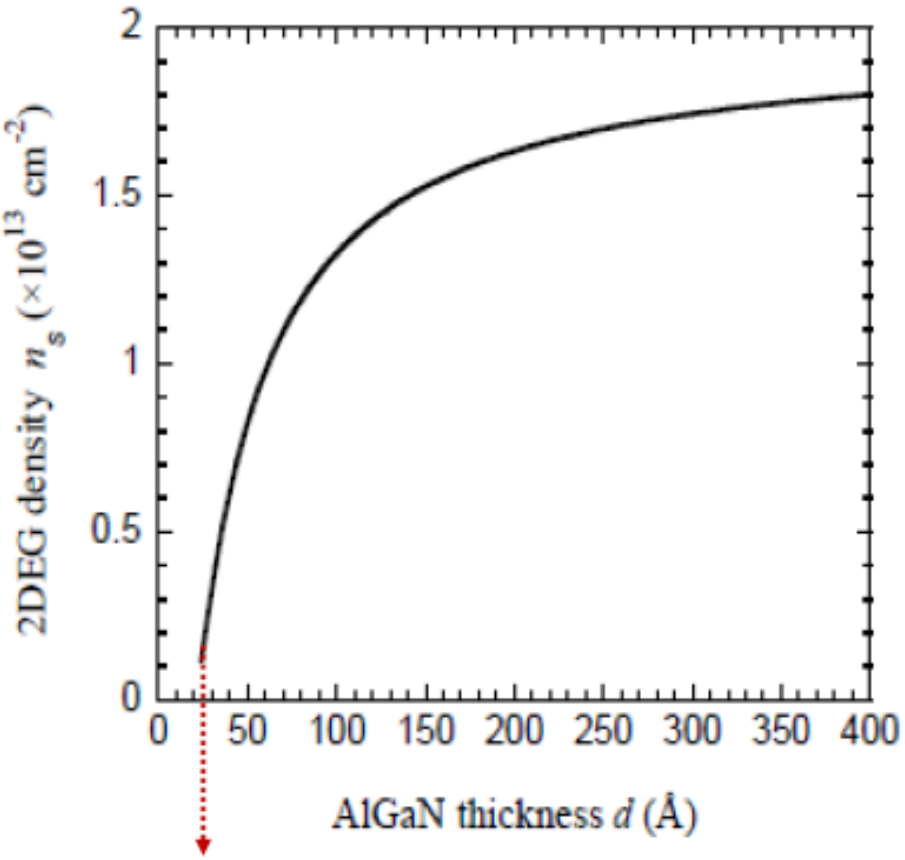


Figure 1.7 Density of two-dimensional electron gas (n_S) as a function of AlGaN barrier thickness [16].

1.4 III-Nitride Heterostructfure Field Effect Transistor (HFET) operation:

The operation principle of an AlGaN/GaN HEMT is similar to an n-channel depletion mode Si-MOSFET with AlGaN replacing the SiO_2 and the 2DEG replacing the n-channel. Unlike any other field effect transistors, the AlGaN/GaN HEMTs do not need any doping for conduction. Due to the presence of the polarization fields, as discussed in the previous section, a 2D potential well is formed at the hetero interface attracting all the electrons from the barrier and thereby confining them in the narrow potential well (see Figure 1.6). For AlGaN/GaN HFET, the 2DEG is located in the i-GaN close to the AlGaN-GaN interface as shown in Figure 1.6.

AlGaN/GaN HFETs are depletion mode or normally-ON field effect transistors, therefore these transistor devices do not require any gate bias for drain current conduction. The drain current can be controlled by applying a negative/positive bias on the gate. A negative bias on the gate will deplete the electrons in the 2D channel thereby reducing the drain current. The schematic layout of a typical AlGaN/GaN and an $Al_yGa_{1-y}N/Al_xGa_{1-x}N$ (y>x) HFET is shown in Figure 1.8. Typically, the barrier Al composition is 20-30% higher than the channel Al composition.

When a bias is applied across the drain and source, the conduction takes place through electrons in the 2DEG resulting in drain current, I_{ds}. The amount of the drain current flowing in the device can be controlled by the gate bias applied to the gate terminal.

The drain saturation current of an HFET at zero gate bias is given by the equation [17]:

$$I_{ds,0} = \frac{V_T^2}{1+\beta R_S V_T + \sqrt{1+2\beta R_S V_T + \frac{V_T^2}{V_L^2}}} \qquad (1.19)$$

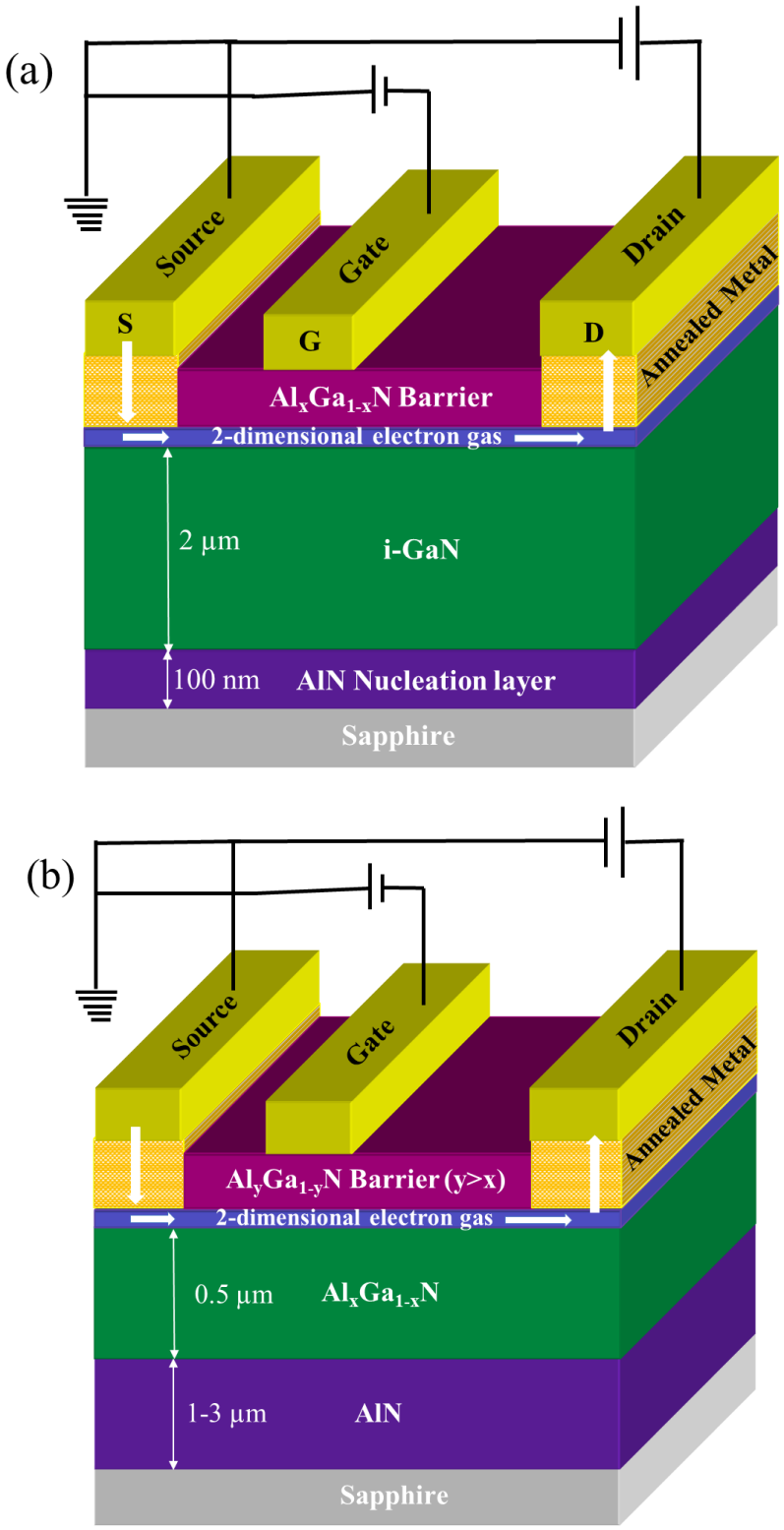


Figure 1.8 Schematic of (a) AlGaN/GaN HFET (b) $Al_yGa_{1-y}N/Al_xGa_{1-x}N$ (y>x) HFET with typical bias arrangement

where $\beta = {\mu C_i}/{L_G}$, C_i is the gate to channel capacitance per unit area and L_G is the gate length, μ is the electron mobility in the 2DEG, R_S is the source to gate series resistance

$V_L = {v_S L_G}/{\mu}$, v_S is the electron saturation velocity

V_T is the transistor threshold voltage

The threshold voltage of an AlGaN/GaN HFET can be estimated from the equation:

$$V_T = \frac{q n_S d}{\varepsilon \varepsilon_0} \qquad (1.20)$$

Where q is the charge of an electron (1.6×10^{-19} C), n_S is the 2DEG charge density in cm^{-2}, d is the AlGaN barrier thickness, ε is the dielectric constant of the AlGaN barrier and ε_0 is the permittivity in vacuum (8.85×10^{-14} F/cm).

Figure 1.9 (a) and (b) show the typical DC IV characteristics of an AlGaN/GaN and an $Al_yGa_{1-y}N/Al_xGa_{1-x}N$ HFET respectively. For the AlGaN-channel HFET the channel and barrier Al composition are 65% and 85% respectively. As seen from the figures, the peak drain current density for GaN-channel and $Al_{0.65}Ga_{0.35}N$-channel HFETs are ~ 750 mA/mm and ~45 mA/mm respectively.

1.5 Role of Ohmic Contact Resistance in HEMT Performance:

In power switching application, transistors are switched between their off and on states as shown in Figure 1.10. These devices are the centerpiece of power electronic circuits. Two important parameters of a power switching transistor are the off-state blocking voltage as known as breakdown voltage (V_{br}), and on-state resistance (R_{on}), many times given as the specific on-resistance, $R_{on}.A$ ($R_{on,sp}$), to take into account the total area of the transistor (A). The vertical and horizontal red lines in Figure 1.10 shows the ideal

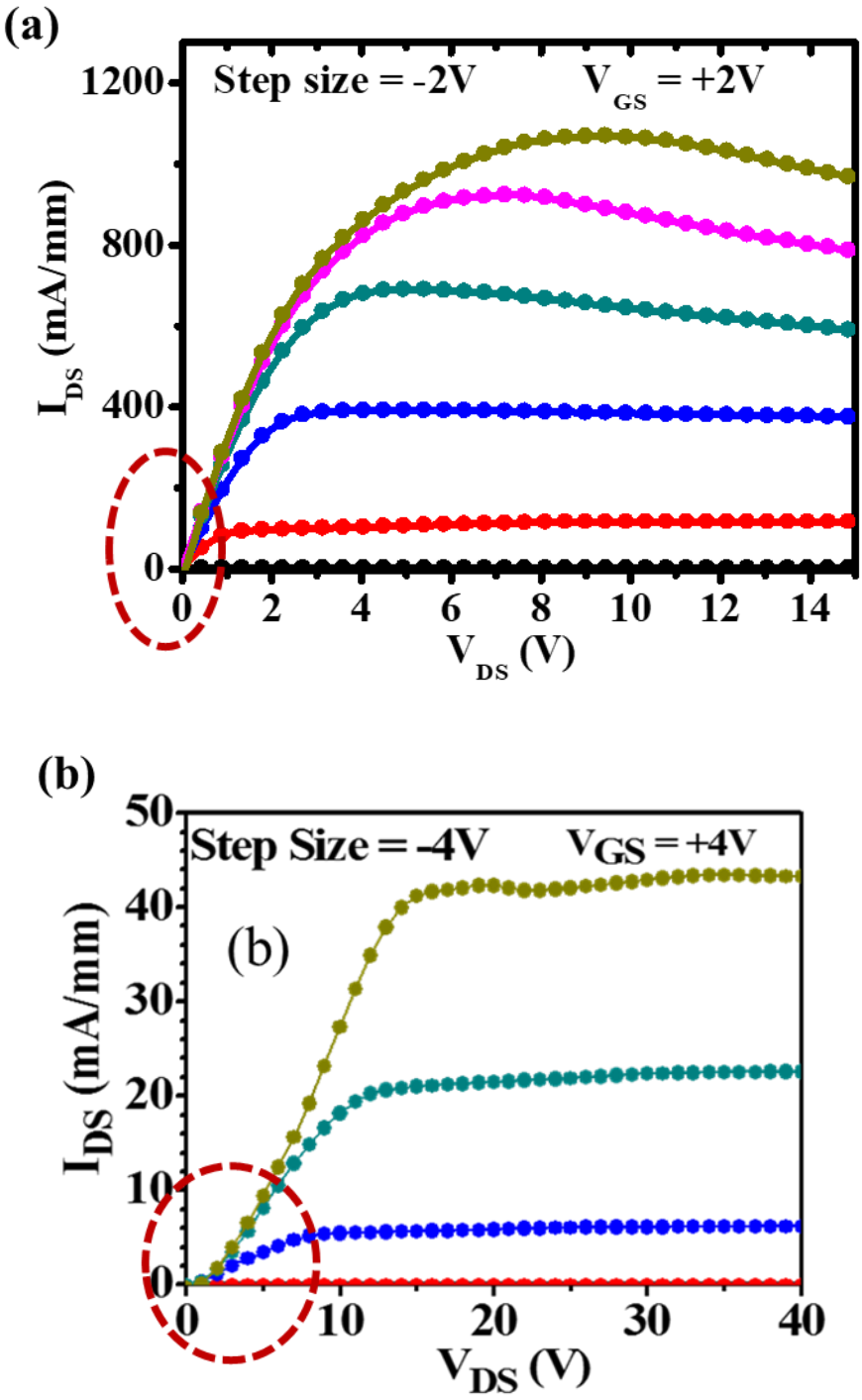


Figure 1.9 DC IV characteristics of an (a) AlGaN/GaN and (b) $Al_{0.85}Ga_{0.15}N/Al_{0.65}Ga_{0.35}N$ HFET

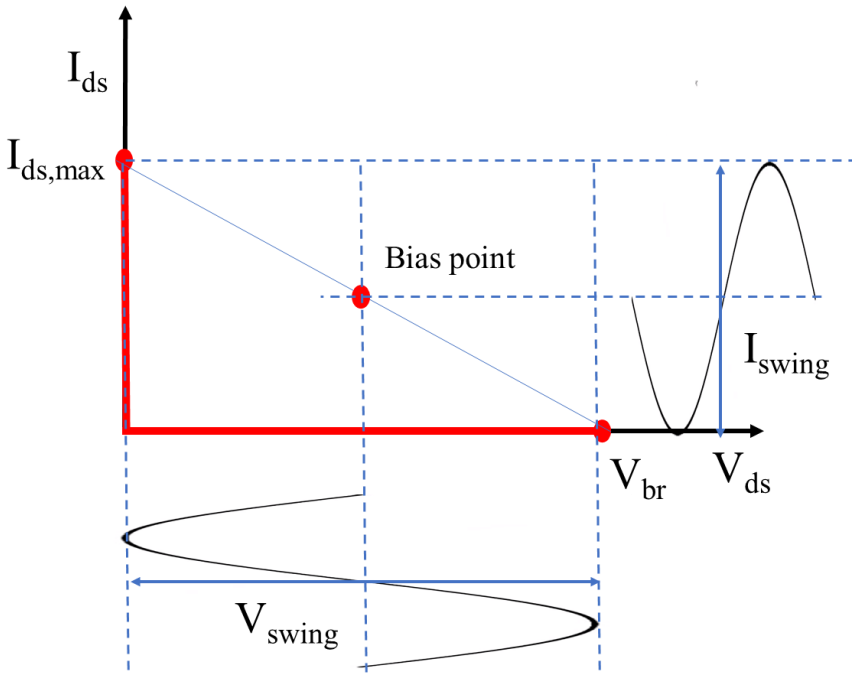


Figure 1.10 On-off states of an ideal power switching transistor and power triangle for calculating output power.

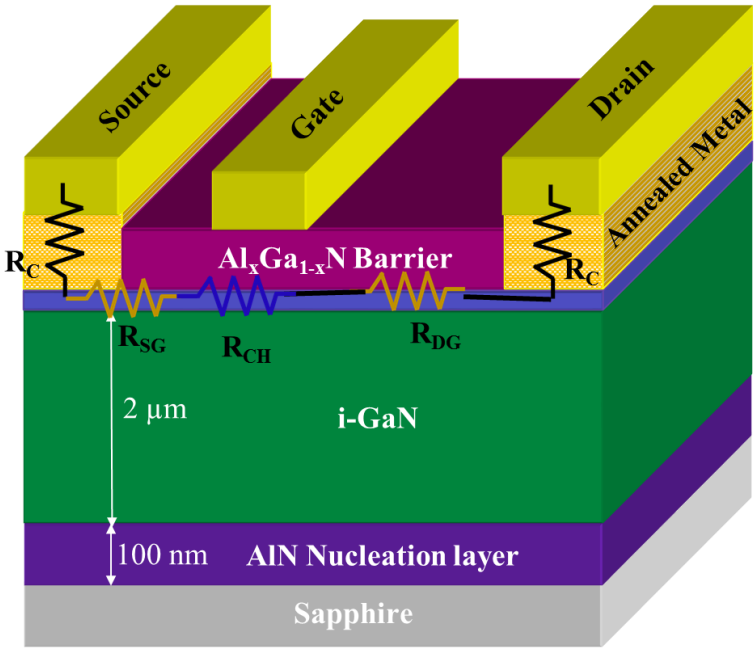


Figure 1.11 Schematic showing total device resistance

switching condition: in the on state the R_{on} should be as low as possible, thus allowing maximum drain current and in the off state the device should offer maximum possible blocking voltage.

$$P_{out,max}^{linear} = \frac{V_{swing} \times I_{swing}}{8} \quad (1.21)$$

$$V_{swing} = V_{br} - V_{knee} \quad (1.22)$$

As seen from the above equation the maximum output power depends on the product of V_{swing} and I_{swing} which are R_{on} dependent. Figure 1.11 shows that the total resistance

$$R_{total} = 2R_C + R_{SG} + R_{CH} + R_{GD}$$

$$= 2R_C + R_{access} + R_{CH}$$

$$= R_{series} + R_{CH} \quad (1.23)$$

1.5.1 Requirement of Ohmic Contact Formation:

Following are two basic requirements for ohmic contact formation: i) High channel electron affinity or matching metal work function and ii) High doping density that results in small tunneling barrier width for electrons. As shown in Figure 1.12 (a), in conventional AlGaN/GaN HEMT, it has relatively high electron affinity (χ_S =4.1 eV) thus resulting in low barrier height ($\Phi_B = \Phi_m - \chi_S$). Also, the metals with similar work function result in small tunneling barrier. The typical ohmic contact is highly linear (see circled portion in Figure 1.9 (a)) with contact resistance (R_C) ~0.1 Ω-mm. As a consequence, the current density is very high (typically > 1 A/mm) in GaN-channel HFETs. Figure 1.12 (b) shows that the barrier height at metal-high Al composition AlGaN junction is much higher than that for

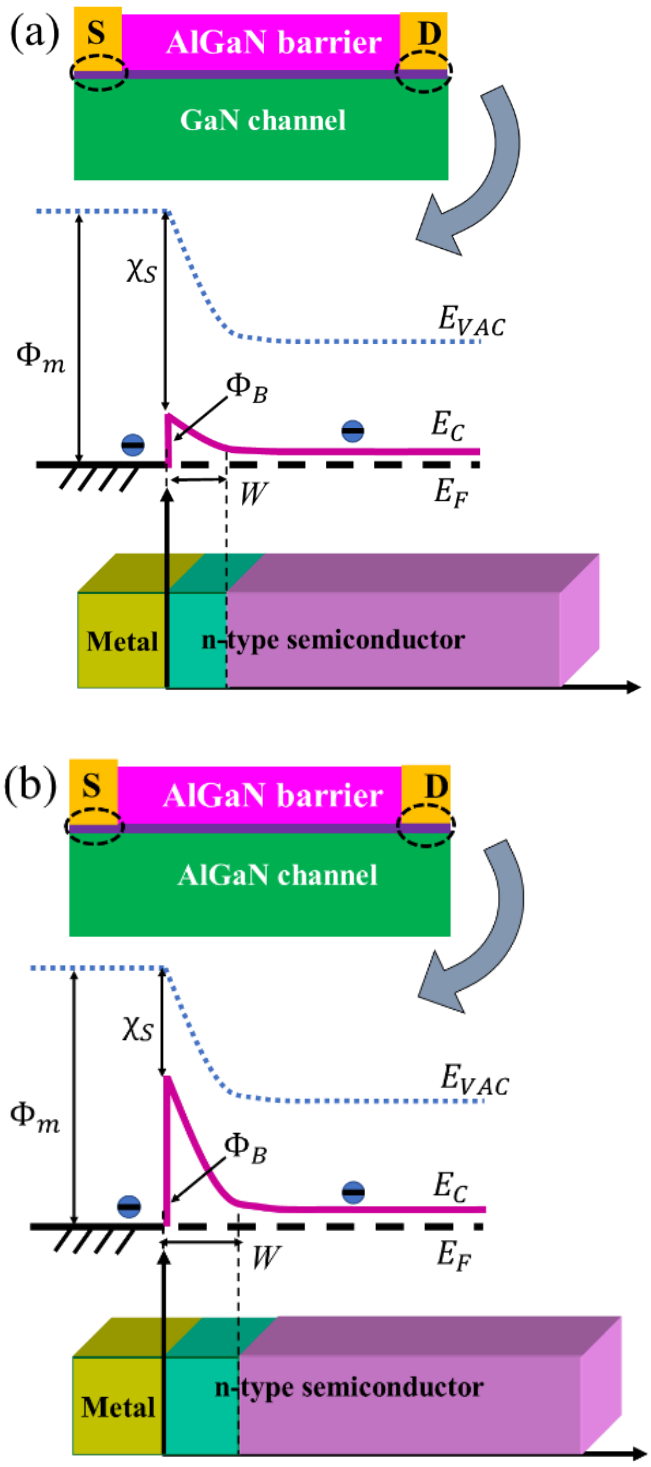


Figure 1.12 Schematic presentation of source drain ohmic contact of GaN (a) and AlGaN-channel (b) devices. Corresponding band diagram showing the Schottky barrier height and depletion width.

GaN-channel due to its low electron affinity (χ_S). As a result, the contact on undoped high-Al AlGaN is non-linear (Schottky) type as opposed to linear ohmic contact. High doping density results in reduction of the depletion width (W) at the metal semiconductor junction thus allowing electrons tunnel through the barrier that results in linear or ohmic contact.

1.6 Gate Leakage in HFET:

The next important parameter of an HFET is the gate leakage current. Figure 1.13 shows the Schottky gate IV characteristics of an AlGaN-channel HFET. Ni/Au is widely used as the Schottky contact for these AlGaN/GaN HFETs due to its high work function and superior sticking properties compared to other metals. III-Nitride HFET devices suffer from high gate leakage currents due to inevitable high density of surface states present at the AlGaN surface. The high-density barrier doping for making ohmic contact in high-Al AlGaN HFETs further increase the gate leakage current. Gate leakage current limits the device performance at high power level by device degradation. In large signal operation, HFET based circuits suffers from distorted output signal that arises from large signal overshoot due to limited forward gate swing.

1.7 Metal Oxide Semiconductor Heterostructure Field Effect Transistor (MOSHFET):

To solve the issue of high gate leakage current, significant progress has been made on metal-insulator-semiconductor-heterostructure-field-effect-transistor (MISHFET) and metal-oxide-semiconductor-heterostructure-field-effect-transistor (MOSHFET). In this approach the gate metal is separated from the AlGaN barrier surface by inserting a layer of insulating dielectric material thereby avoiding the high tunneling currents through the Schottky barrier. Figure 1.14 shows the cross-section schematic of an insulated gate

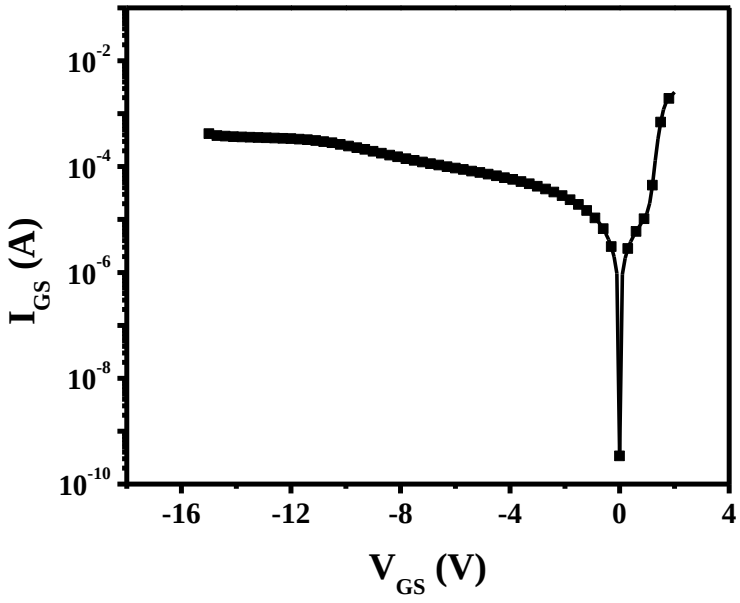


Figure 1.13 Gate leakage current of an AlGaN-channel HFET

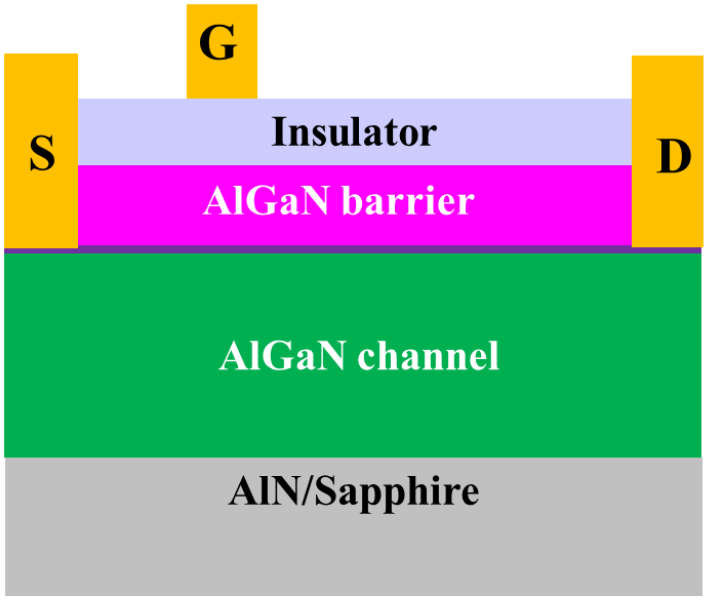


Figure 1.14 Schematic cross section of an insulated-gate HFET

HFET device. Khan et.al has demonstrated the first insulated gate structure on AlGaN/GaN HFETs using PECVD SiO_2 [18]. Figure 1.15 (a) shows the comparative gate leakage current of $Al_{0.4}Ga_{0.6}N$-channel HFET and MOSHFET fabricated on same wafer [19]. It shows the gate leakage in MOSHFET is suppressed by ~3 orders of magnitude compared to HFET in both forward and reverse gate voltage direction. Low gate leakage in the reverse direction increases the MOSHFET breakdown voltage compared to that for HFET. This approach also allows higher forward gate voltage swing compared to HFET while maintaining very low gate leakage. High forward gate voltage swing enables handling large signal overshoot. Figure 1.15 (b) shows the transfer characteristics (I_{DS}-V_{GS}) characteristics of the $Al_{0.4}Ga_{0.6}N$-channeld HFET and SiO_2 MOSHFET. As seen from the figure, the use of 10 nm SiO_2 enables forward gate voltage swing up to +6 V, thus enabling 1.5× drain current compared to HFET.

1.7.1 MOSHFET characteristics:

In a SiO_2 MOSHFET device, the gate is isolated from the barrier AlGaN surface by a SiO_2 film deposited using PECVD. The key parameters that determine the performance of a MOSHFET devices are:

(a) Threshold voltage

(b) Gate-source capacitance

(c) Gate leakage current

The threshold voltage of a MOSHFET depends on the thickness of the SiO_2 film. The equation used to estimate MOSHFET threshold voltage is [20]:

$$V_{T,MOSHFET} = V_{T,HFET}\left(1 + \frac{d_{ox}\varepsilon_{AlGaN}}{\varepsilon_{ox}d_{AlGaN}}\right) \qquad (1.24)$$

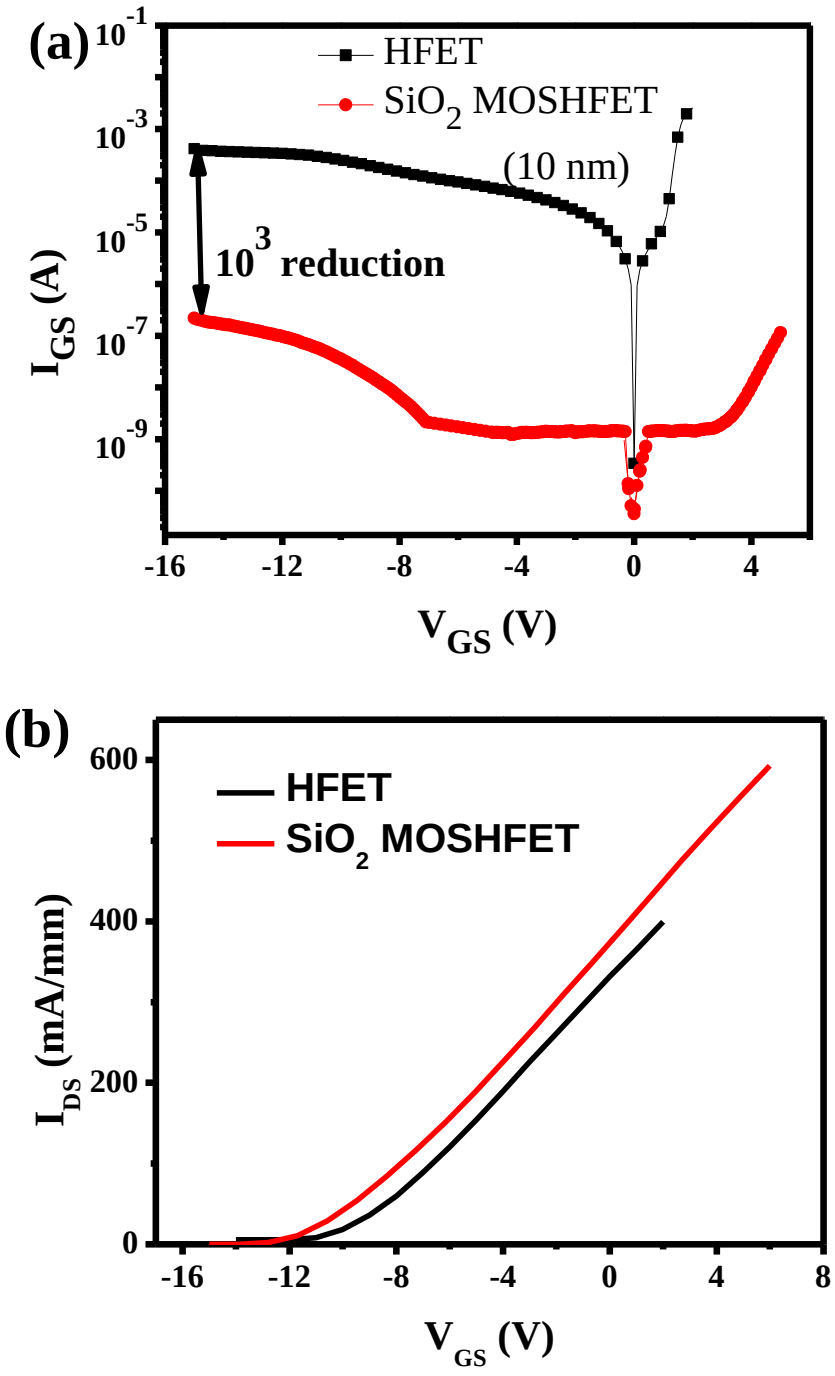


Figure 1.15 (a) Gate leakage characteristics of $Al_{0.4}Ga_{0.6}N$-channeld HFET and SiO_2 MOSHFET fabricated on same wafer. (b) Transfer characteristics of $Al_{0.4}Ga_{0.6}N$-channeld HFET and SiO_2 MOSHFET.

where are SiO_2 and AlGaN barrier thickness respectively, ε_{AlGaN} is dielectric constant of AlGaN barrier (8.8 eV) and ε_{ox} is dielectric constant of SiO_2 (3.9 eV). From the above equation is it evident that, the MOSHFET threshold voltage increases with SiO_2 thickness, that means the gate require more negative voltage to deplete the 2D channel. Figure 1.16 (a) shows the GaN-channel MOSHFET threshold voltage dispersion as a function of oxide thickness estimated from above equation and Figure 1.16 (b) shows experimental data on GaN-channel MOSHFET [17]. In the calculation the barrier thickness is considered as 20 nm and the HFET threshold voltage as -4 V, typical value for GaN HFET devices.

The addition of an oxide layer adds an additional capacitance in series with the barrier capacitance, thus reducing the overall input capacitance according to the following formula:

$$\frac{1}{C_{MOS}} = \frac{1}{C_{HFET}} + \frac{1}{C_{ox}} \qquad (1.25)$$

Figure 1.17 shows capacitance-voltage characteristics of an $Al_{0.4}Ga_{0.6}N$-channel HFET and MOSHFET fabricated on the same wafer. The MOSHFET device has 10 nm thick SiO_2 under the gate. It is clearly seen that the input capacitance dropped by more than two times compared to that of HFET. Another important device performance parameter is the transconductance, G_M. It is defined as the ratio of change in the drain current for a given change in the gate bias, $G_M = {dI_{ds}}/{dV_{gs}}$. The larger the transconductance figure for a device, the greater the gain it is capable of delivering, when all other factors are held constant. The transconductance is a direct function of the device input capacitance. Thus, lower input capacitance leads to lower value of transconductance compared to that of HFET.

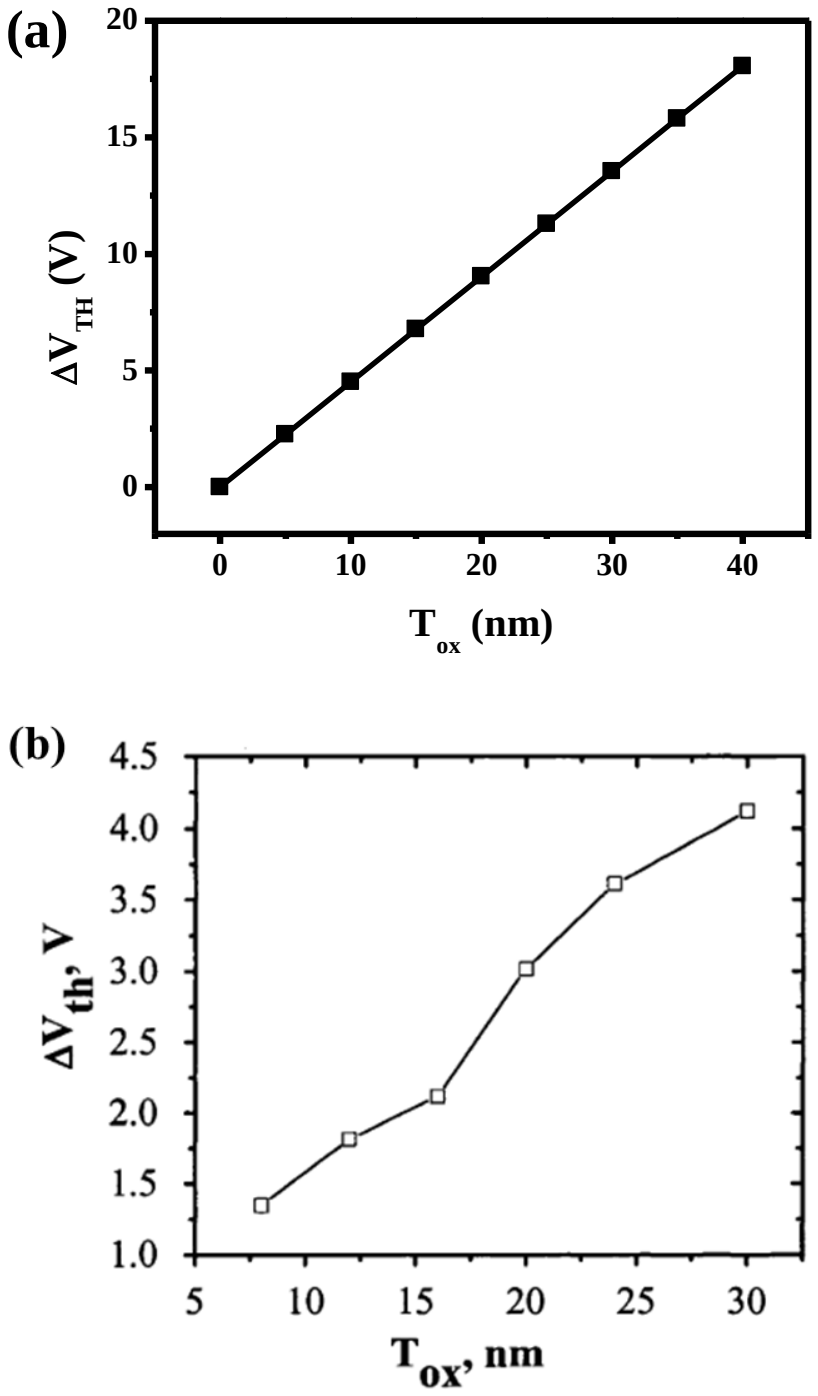


Figure 1.16 (a) Calculated threshold voltage dispersion in MOSHFET as a function of SiO_2 thickness (b) Experimental data on threshold dispersion from reference [16]

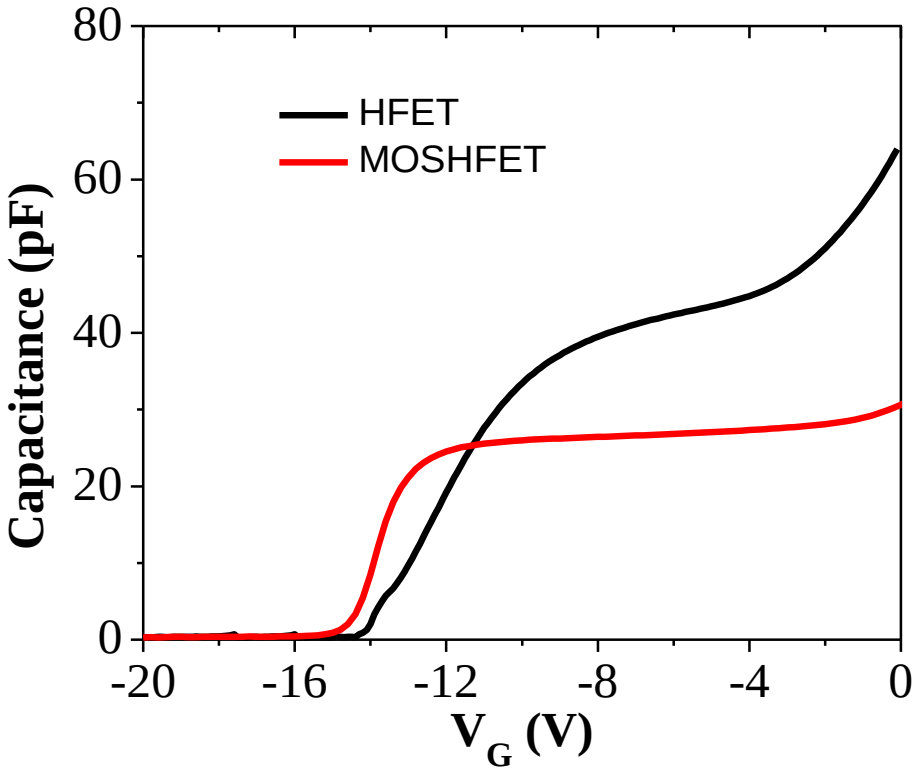


Figure 1.17 Capacitance-voltage characteristics of HFET and SiO_2-MOSHFET

1.8 Problem Identification and Technical Approach:

(1) In previous section we have discussed that, SiO_2 MOSHFET devices suppress the gate leakage, but it comes with more negative threshold voltage shift compared to HFETs. MOSHFET device with low gate leakage as well as low V_{TH} are required for medium power amplifier and several power electronics circuits [20]. The V_{TH} shift in GaN-channel devices are not that severe for two reasons: i) V_{TH} in GaN-channel is lower, so even increased V_{TH} in MOSHFET is acceptable and ii) the dielectric thickness in GaN-channel MOSHFET can be smaller because of better morphology. But the V_{TH} sift in AlGaN-channel MOSHFETs must be controlled in order to make the device practically useful. Equation 1.24 shows that MOSHFET V_{TH} can be lowered decreasing the dielectric thickness d_{ox} or by using dielectric material with higher value of ε_{ox}. Reducing the gate oxide thicknesses leads to increased gate leakage due to tunneling which in turn leads to device degradation. Therefore, the alternate approach of using high-*k* dielectrics is a more promising approach to lower the V_{TH} while maintaining low gate leakage currents. The dielectric constant, '*k*' refers to a material's ability to concentrate an electric field. As demonstrated in Figure 1.18 (a), if one gate oxide has twice the dielectrtic constant of another, a given gate voltage will draw twice as much charge into the channel. Hence, having a higher dielectric constant means the insulator can provide increased capacitance between two conducting plates, thus storing more charge for the same thickness of insulator. Alternately, it can provide the same capacitance with a thicker insulator [21]. Figure 1.18 (b) shows that, use of high-*k* ZrO_2 (k=25) of same thickness of that of low-*k* SiO_2 (*k*=3.9) results in higher capacitance. In GaN-channel MOSHFETs, high-*k* dielectrics ($k > 20$) have showed

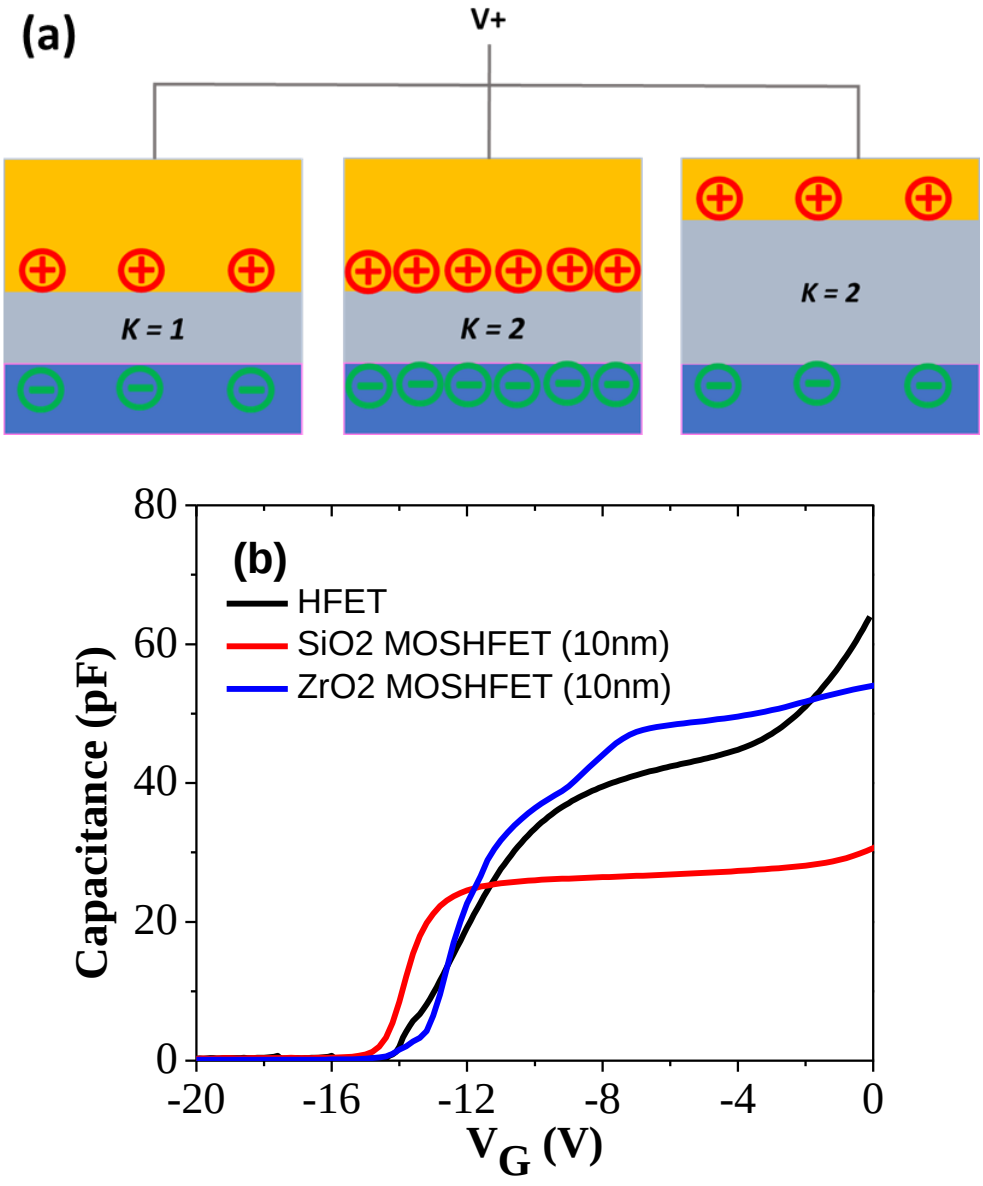


Figure 1.18 (a) charge storing capacity in materials with different dielectric constant. (b) Capacitance-voltage characteristics of HFET and MOSHFETs with same thickness of SiO_2 and ZrO_2

advantage for good channel controllability which leads to high ON/OFF current ratio, low sub-threshold slope. These characteristics enable low power loss at OFF-state and high efficiency in the power conversion system [22]. It is reasonable to expect the same benefits from high-*k* in AlGaN- channel devices, but this needs to be studied. This dissertation aims to develop high-*k* oxides for controlling the threshold voltage in ultrawide bandgap $Al_xGa_{1-x}N$ (x>0.4)-channel MOSHFETS while simultaneously maintaining extremely low gate leakage current and high enough input capacitance.

(2) Despite the higher BFOM due to of its' high breakdown field, AlGaN devices have much lower peak currents as compared to GaN channel devices due to higher channel and contact resistances. The state-of-the-art peak current density prior to this work was 0.8 A/mm while the typical values in GaN-channel devices are 1-2 A/mm. Thanks to high-*k* dielectrics, it allows large forward gate swing compared to HFET, leading to ~1.5-2× increase in drain current density. The higher is the current, the higher is the voltage drop across parasitic resistances thus increasing the channel temperature that in turns reduce the drain current. Hence it is important to minimize all components of access resistances by every means. Equation 1.23 shows that the total device resistance is composed of channel resistance (R_{CH}) under the gate and series resistance. Again, series resistance has two parts- contact resistance and access resistance. To minimize the access resistance and subsequent increase in drain current density beyond 1 A/mm in UWBG AlGaN-channel devices, this dissertation aims to develop processing approaches with following innovations:

    (i) Perforated-channel geometry, which have shown significant access resistance reduction in GaN-channel devices.

(ii) hybrid gate insulator design (ZrO_2/Al_2O_3) combined with perforated channel geometry that enables realization of record high current depletion (D-) and enhancement mode (E-mode) UWBG AlGaN-channel MOSHFETs.

1.9 Thesis Outline:

The next six chapters provide a detailed description of various approaches that have been adopted to solve the above mentioned issues in high-Al composition UWBG AlGaN channel devices and the state of the art results obtained by the adoptation of these novel approaches.

Chapter 2 discusses the state of the art AlGaN-channel device performance prior to this work.

Chapter 3 starts off with a description of epilayer that is used to fabricate ZrO_2 MOSHFET. The chapter then goes to discuss the MOSHFET fabrication process with high-*k* ALD ZrO_2 and subsequent annealing to understand the mechanism of threshold control. This chapter further discusses performance of AlGaN-channel MOSHFETs based on three different high-*k* dielectrics: ZrO_2, Al_2O_3 and TiO_2 and establishes hybrid oxide (ZrO_2/Al_2O_3) for next generation devices. The techniques established in this chapter forms the essential backbone that enables the device results in the next chapters.

Chapter 4 disscusses the improvement of series resistance in AlGaN channel devices. To achieve a high current density it is extremely important to take care of all components of series resistance. The initial part of the chapter describes development of pseudomorphic epilayer structure to reduce the relaxation that potentially reduces the

scattering as well as channel resistance. The chapter then describes the application of a perforated channel approach in AlGaN channel devices to reduce access resistance that was previously used in GaN channel devices. Incorporating the perforated channel technique with the hybrid oxide in the pseudomorphic structure enable realization of state of the art UWBG $Al_xGa_{1-x}N$ (x>0.4) channel devices with current density exceeding 1 A/mm.

In chapter 5, the importance of normally off devices in power electronics is discussed followed by literature survey for the state of the art normally off UWBG devices. The chapter then discusses the fabrication and characterization of enhancement mode (E-mode) UWBG $Al_xGa_{1-x}N$(x>0.4)-channel devices with performance levels (peak current and threshold voltage) well over those reported in literature based high current E-mode devices that can open the door for AlGaN based ICs. Similar to depletion-mode devices, the high current E-mode devices were fabricated using perforated channel technique and hybrid oxide.

Chapter 6 discusses temperature dependent device characteristics such as mobility, sheet carrier concentration, drain current density and threshold voltage. It provides a detailed analysis of temperature dependent threshold instability in D- and E-mode devices and explains potential mechanism of V_{TH} shift.

Chapter 7 summarizes the discussion followed by future work suggestions based on the state of the art AlGaN-channel device results.

CHAPTER 2: STATE OF THE ART AlGAN-CHANNEL DEVICE PERFORMANCE PRIOR TO THIS WORK

Since early 2000, there has been considerable interest in developing ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ channel Heterostructure Field Effect Transistors (HFETs) for high-temperature, high-voltage, and high-power applications. The motivation comes from the scaling of the UWBG $Al_xGa_{1-x}N$ breakdown field with alloy composition. This should in principle lead to a much higher Baliga Figure of Merit (BFOM) [12][23][24].

Some of the key reports of the earlier work aimed at developing AlGaN channel devices are listed in the Table 2.1. Nanjo/Tokuda et.al. started research with high-Al composition AlGaN-channel HEMTs and demonstrated its importance for power and RF devices. They realized that, the higher bandgap in AlN compared to GaN combined with its comparable saturation velocity would make AlN or high aluminum mole fraction AlGaN suitable materials to increase the breakdown voltage without decrease of the drain current density. However, they realized that high aluminum mole fraction AlGaN or AlN would have increased the contact resistance significantly, thus they fabricated AlGaN HEMT with $Al_{0.2}Ga_{0.8}N$ channel and $Al_{0.4}Ga_{0.6}N$ barrier [25]. Using Si implantation based ohmic contact formation technique, they demonstrated first AlGaN transistor operation with drain current (I_D) density of 0.13 A/mm at gate voltage (V_G) 2 V for a device with gate length (L_G) 1 µm, gate width (W_G) µm and distance between source and drain (L_{SD})

Table 2.1 Summary of key research results on AlGaN-channel transistors

Group	Al% (y/x or x or x→y)	Barrier Doping	Contact Resistance (Ω-cm^2)	Peak Currents (A/mm)	Breakdown Voltage (MV/cm)	Comments	Reference
Nanjo/Tokuda et.al.	40/20	Si-Implant Contact	1.2×10^{-3}	0.13	--	Mitsubishi Electric Adv. 2009	[25]
Nanjo/Tokuda et.al.	53/38	Si-Implant Contact	5.28×10^{-3}	0.11	1.6		[26]
Tokuda/Kuzahara et.al	86/51	Undoped	4.8×10^{-2}	0.025	1.2	Ohmic Contacts-Zr/Al/Mo/Au	[27]
Yafune/Kuzahara et.al	100/60	Undoped	1.9×10^{-2}	0.04	--	Ohmic Contacts-Zr/Al/Mo/Au	[28]
Baca et.al.	100/85	Undoped	--(non-linear)	0.002	0.81	n+ GaN regrown contact	[29]
Sakib/Khan et.al.	85/65	Doped	5.6×10^{-3}	0.25	0.9	Nonlinear Ohmic Contacts	[30]
Hu/Khan et.al.	65/45	Doped	1.4×10^{-5}	0.6	--	Linear Ohmic Contacts	[19]
Gaevski/Khan et.al.	65/40	Doped	1.35×10^{-5}	1.3	2.08	First AlGaN-Channel D-mode with $I_{Dmax} > 1$ A/mm	[31]
Klein et.al.	85/70	Undoped	8.4×10^{-2}	0.035	--	AlGaN-Channel E mode (recessed gate + fluorine treatment)	[32]
Douglas et. al.	45/30	Undoped	1.4×10^{-6}	0.1	--	AlGaN-Channel E mode (p-$Al_{0.3}Ga_{0.7}N$ gate)	[33]
Shahab/Khan et.al.		Doped	1.35×10^{-5}	0.48	1.7	AlGaN-Channel E-mode (recessed gate)	[34]

of 4 µm. Considering the first AlGaN device, this initial result was pretty good if compared with the first GaN HEMT I_D of 50 mA/mm with L_G= 4 µm, L_{SD} = 10 µm [35] while later GaN devices exceeded 1 A/mm.

Following the first demonstration of AlGaN channel HEMT the same group reported enhanced breakdown characteristics with increasing Al composition [26]. The breakdown voltage was evaluated for Al composition from x=0 (GaN) to x=0.38. The average breakdown field was about 1.6 MV/cm and exceeded the GaN HEMT breakdown by ~8×. In their devices, the enhanced breakdown voltage came with a sacrifice in the peak current density where they experience a decrease in I_D with the increase in Al mole fraction. These devices were without any field plate thus indicating potential improvement in breakdown field with the use of field plates.

Since then, Tokuda et. al., Yafune et.al., Baca et.al. and our group have also reported UWBG AlGaN channel HEMTs with Al-alloy compositions ranging from 50% to 85 % [27]-[30]. In 2010 Tokuda et. al., reported on breakdown and temperature dependent output characteristics of a $Al_{0.86}Ga_{0.14}N$/ $Al_{0.51}Ga_{0.49}N$HEMT. They introduced Zr based ohmic contact (Zr/Al/Mo/Au) as opposed to widely used Ti/Al based metals where they found the Zr based metal stacks work better in forming ohmic contact to high-Al composition AlGaN [27]. Their reported current density (I_D) was 25.2 mA/mm at V_G= + 4 V. This high forward gate bias was attributed to (i) the large conduction band discontinuity (ΔE_C= 0.75 eV) at channel/barrier interface and (ii) the high Schottky barrier height (φ_B = 2.67 eV) of $Al_{0.86}Ga_{0.14}N$ while the smaller drain current density was still attributed to the higher value of contact resistance of 4.8×10^{-2} Ωcm^2. When the HEMTs were compared against GaN-channel control devices over the 25 °C–300 °C temperature

range, the drain current density was found to decline less than in the GaN-channel control, as illustrated in Figure 2.1 (a) [27]. Later in 2014, the same group, demonstrated similar negligible temperature dependence of drain current density in their AlN/$Al_{0.6}Ga_{0.4}N$ HEMTs (see Figure 2.1(b)) [28]. The degradation ratio in the drain current between 300 and 573 K was only 4% for the AlN/$Al_{0.6}Ga_{0.4}N$ HEMT, whereas it was as large as 80% for the control GaN-channel HEMT. Temperature associated mobility degradation, larger for GaN than AlGaN, was given as the causal reason for the greater temperature I_D decline of the GaN-channel HEMT. Their result demonstrated that, AlGaN-channel HEMTs are suitable candidate for high-temperature electronics due to the temperature insensitive dependence.

In 2016, Baca et. Al., reported on higher Al-composition $Al_xGa_{1-x}N$ (x=0.85) with AlN barrier [36]. In these devices, they demonstrate AlN barrier etch and n+ GaN regrowth technique for source and drain ohmic contact formation. GaN:Si conformal growth was reported over the exposed AlGaN surfaces that depletes the AlGaN surface contributing substantial increase to parasitic resistance resulting nonlinear ohmic contact. Low I_D of 2 mA/mm was attributed to the rectifying behavior of the source and drain contacts. Without any gate insulator the devices showed extremely low gate leakage current ~ 10 pA. The device subthreshold slope (SS) and and ON/OFF ratio were reported to be 75 mV/decade and 10^7. Such low SS and high ON/OFF ratio were attributed to the excellent gate leakage characteristics. These results further show the potential of high-Al AlGaN for high-power electronics. The key problem they encountered was the excessively large contact resistance, in spite of the regrown n+-GaN contacts, that severely limited the peak drain current.

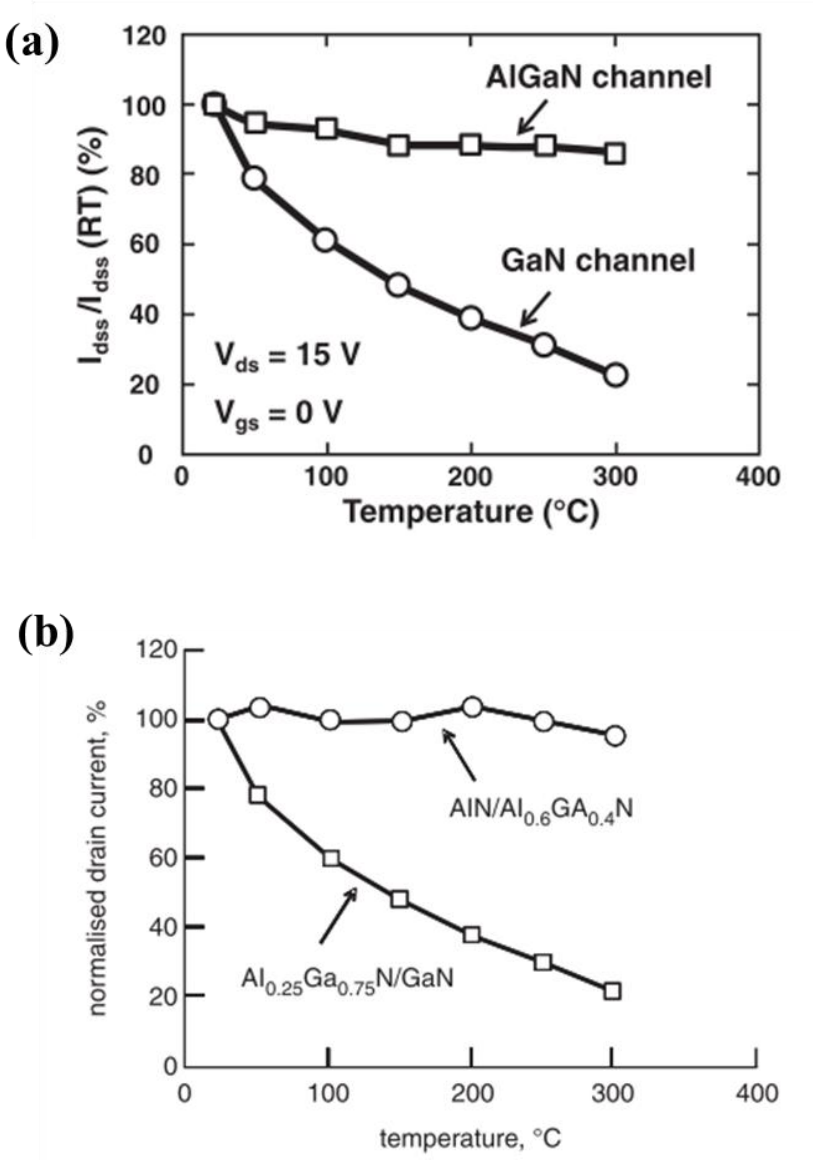


Figure 2.1 (a) Temperature dependent drain current in $Al_{0.51}Ga_{0.49}N$-channel HEMTs reported by Tokuda et. al (b) Similar temperature dependence on $Al_{0.6}Ga_{0.4}N$-channel reported by same group.

In 2017, our group reported on n-$Al_{0.65}Ga_{0.35}N$ channel Metal Semiconductor Field Effect Transistors (MESFETs) over high-quality AlN/sapphire templates from room-temperature up to 200 °C [37]. A selective area growth approach was used to fabricate graded composition n-$Al_xGa_{1-x}N$ source-drain contact layers. Si-doped graded composition n-$Al_xGa_{1-x}N$ layer (x=0.65 to x=0) was deposited in the source-drain openings. This highly doped graded composition contact layer approach allows the source-drain contacts to be made to a GaN layer as opposed to high-Al n-$Al_xGa_{1-x}N$, thereby helping with the ohmic-contact formation. Moreover, the high n-type doping compensates the free positively charged holes resulting from the fixed negative polarization charge due to the $Al_xGa_{1-x}N$ composition grading. A peak output current I_D=100 mA/mm was reported at V_G=+2V. For operation temperatures from room-temperature (RT) to 200 °C, the source-drain currents, the threshold voltages, and the dc-transconductance values were nearly unchanged with an estimated field-effect mobility of ~90 cm^2/V-s at 200 °C. Beside showing very good temperature dependent electrical characteristics, these devices also exhibited excellent performance as deep ultraviolet solar-blind optical sensor in the photoconductive mode with a peak responsivity of 1.22×10^6 A/W at 254 nm.

However, for these early reports the ohmic contact formation to the barrier $Al_xGa_{1-x}N$ layers was very challenging. Ohmic contacts were either nonlinear or contributed to a large series resistance of the order of the channel resistance thereby leading to very low peak currents ranging from 2 mA/mm to 100 mA/mm (see Table 2.1). To fully understand the role of the contact resistivity in high Al-content $Al_xGa_{1-x}N$ (x > 0.6) channel HEMTs Muhtadi et. al., did a comparative study of doped and un-doped barrier $Al_{0.85}Ga_{0.15}N/Al_{0.65}Ga_{0.35}N$ HEMTs on high-quality AlN buffer layers [30]. 2×10^{17} cm^{-3} Si

doping changed the sheet resistance by only 200 Ω/sq (from 2000 Ω/sq to 1800 Ω/sq). The peak drain-current in doped barrier structure was found to be 250 mA/mm which was state of the art value for an $Al_xGa_{1-x}N$ ($x > 0.6$) channel HEMT and ~5× higher compared to un-doped barrier structure. Even though barrier doping increased the output current significantly, was still high (~112 Ω-mm) and identical in both structures. The higher drain current in doped barrier structure was attributed to the less negative surface charge (compensated by the donor dopants) and pinch-off voltage due to higher total channel charge. In doped barrier design, gate leakage was found to be higher compared to un-doped barrier design, thus compromising the benefit that the doping was supposed to provide. To suppress gate leakage SiO_2 is a widely used material as gate insulator. More recently our group reported on an UWBG *n*-$Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ Metal Oxide Semiconductor heterostructure field effect transistor (MOSHFET) with a doped barrier design (see Figure 2.2 (a)) [19]. As shown in Figure 2.2(b), the doped barrier design enabled linear ohmic contact formation with a contact resistivity as low as 1.4×10^{-5} Ω-cm^2. The insulating gate enabled device operation up to gate-voltages as high +6V which pushed the peak drain currents to 600 mA/mm. Figure 2.2 (c, d) shows the transfer and gate leakage characteristics for the $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ MOSHFET with a gate width W=50 µm, gate length L_G=2 µm and the source-drain distance L_{SD}=6 µm. The gate-drain separation L_{GD} was 3 µm. The MOSHFET peak saturated current I_{DS} (at V_{GS}= +6V) is about 0.6 A/mm. However, for an identical geometry HFET device (no oxide under the gate), the peak current at V_{GS}=+2 V (maximum gate-voltage without excessive leakage) was only 0.4 A/mm. Figure 2.2 (d) shows in MOSHFET the gate leakage is suppressed by ~ 4 orders of magnitude compared to similar geometry HFET. Because of SiO_2 gate dielectric, the

current density in MOSHFET is increased by 1.5× compared to HFET due to the ability to apply more positive bias at the gate and the leakage current decreased by ~10^4 compared to HFET.

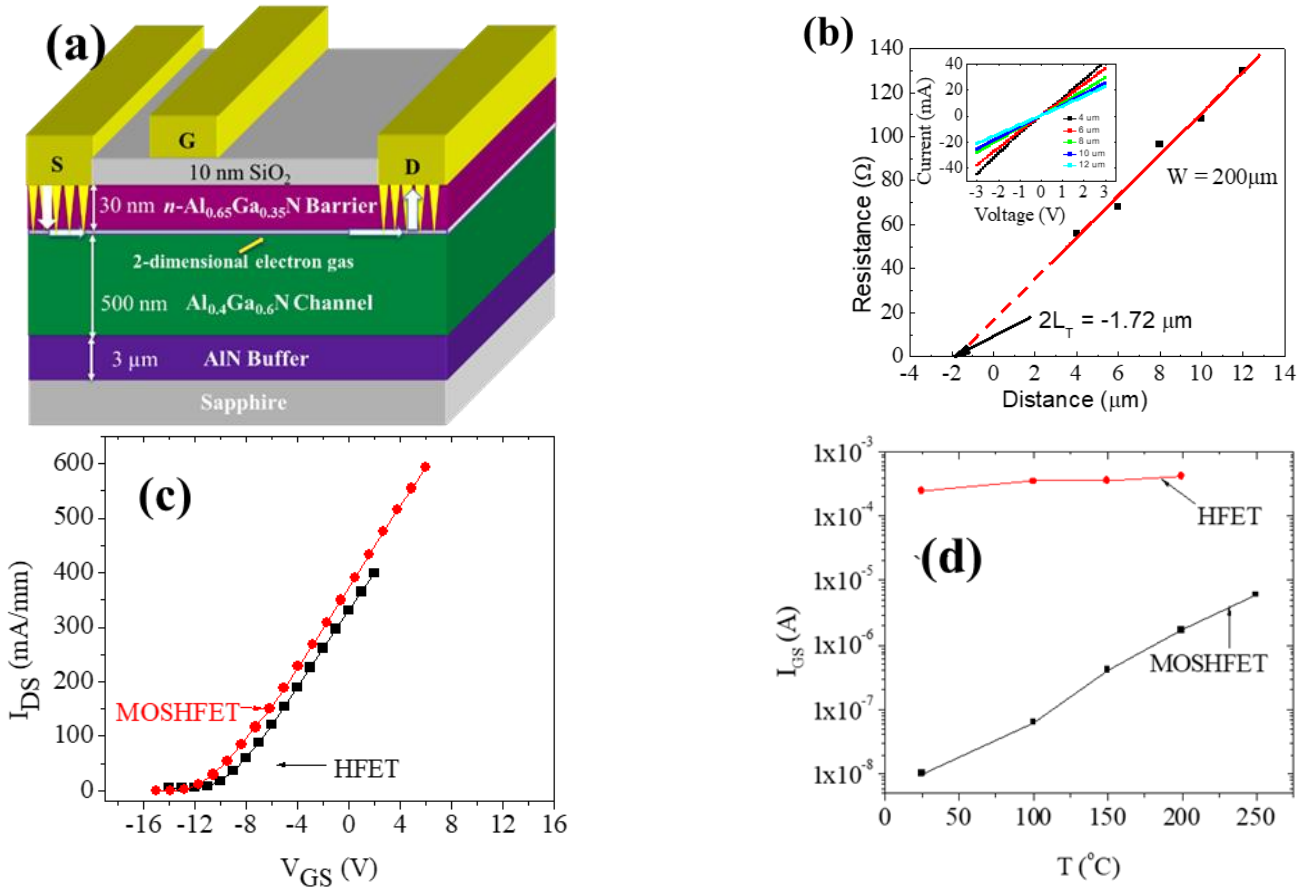


Figure 2.2 (a) Schematic of a *n*-$Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ Metal Oxide Semiconductor heterostructure field effect transistor (MOSHFET) with a doped barrier design (b) TLM plot for extracting contact and sheet resistances of $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ device. Inset shows the linear current-voltage plot (c) Transfer characteristics of the SiO_2 MOSHFET compared with that for the HFET (d) Temperature dependent gate leakage plot for the SiO_2 MOSHFET and the HFET.

CHAPTER 3: GATE LEAKAGE AND THRESHOLD VOLTAGE CONTROL IN UWBG ALGAN-CHANNEL MOSHFETS USING HIGH-K ALD DIELECTRICS

3.1 Background:

As discussed in the introductory chapter, good gate control and low gate leakage are two key requirements for power electronic devices which is typically not possible using classic Schottky gate structures thereby making MOSHFETs a more suitable device choice. Including a dielectric such as SiO_2 between the gate metal and barrier/channel region results in reduction of gate leakage in metal oxide semiconductor HFET's (MOSHFET) in both voltage directions [19]. However, this comes at the expense of higher negative threshold voltage (V_{TH}) as discussed before, which requires higher operating gate voltages that can lead to higher gate leakage, negating the very benefit the dielectric was supposed to provide. Usually this is solved using high-*k* dielectrics which are often deposited using atomic layer deposition (ALD) due to the ease of thickness control [20]. These ALD dielectrics can suppress gate leakage while maintaining a large gate capacitance in thick enough layers to increase the gate operating voltage with only a modest shift in V_{TH} [17][20]. However, in these ALD dielectrics, the V_{TH} shift is governed not by the geometrical capacitance, but instead by the fixed charges at the dielectric/AlGaN interface,

$n_{ox,intf}$, the distributed fixed charges through the bulk of the dielectric, $n_{ox,bulk}$, and the interfacial trapped charges as shown in Figure 3.1 [38]. These charges present additional variables that must be controlled to achieve the desired V_{TH} with low gate leakage.

To quantify the influence of $n_{ox,intf}$ and $n_{ox,bulk}$ on V_{TH}, in MOSHFETs we use [38][39]:

$$V_{th} = \Phi_b - \Phi_f - \Delta E_c - \frac{qt_{ox}^2}{2\varepsilon_{ox}} n_{ox,bulk} - \frac{qt_{ox}}{\varepsilon_{ox}} n_{ox,intf} - q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_b}\right) \qquad (3.1)$$

where Φ_b is the metal barrier height, ΔE_c is the conduction band discontinuity, Φ_f is the energy difference between conduction band and fermi energy, t is thickness, ε is permittivity and the subscripts b and ox refer to AlGaN barrier and oxide (ZrO_2). $n_{ox,bulk}$ represents the bulk oxide charge (per unit volume), and $n_{ox,intf}$ represents the oxide/barrier interface charge density. Equation (1) underscores the abovementioned fact that $n_{ox,bulk}$ and $n_{ox,intf}$ are two key V_{TH} control parameters in MOSHFETs especially in thicker oxides. To separate the contribution of $n_{ox,bulk}$ and $n_{ox,intf}$ to V_{TH} dispersion, we present an oxide thickness (t_{ox}) dependent study of V_{TH} values for MOSHFETs high-*k* ALD ZrO_2 gate-insulator, which is the key of this chapter.

In addition to a large dielectric constant, the high-*k* dielectric is required to have a large band gap (E_G) to suppress the charge injection from electrodes into dielectrics that cause the leakage current.[40]-[42] Therefore, the ideal high-*k* dielectrics should possess both large E_G and *k*. The E_G and *k* are related with the equation, $= 1 + {(\hbar\omega_p)^2}/{E_G^2}$., When E_g and *k* of well-known oxides are plotted (Figure 3.2), the trade-off relation is clearly noticeable. That is, materials are abundant with large E_G (4~8 eV) or high-*k* (4~20);

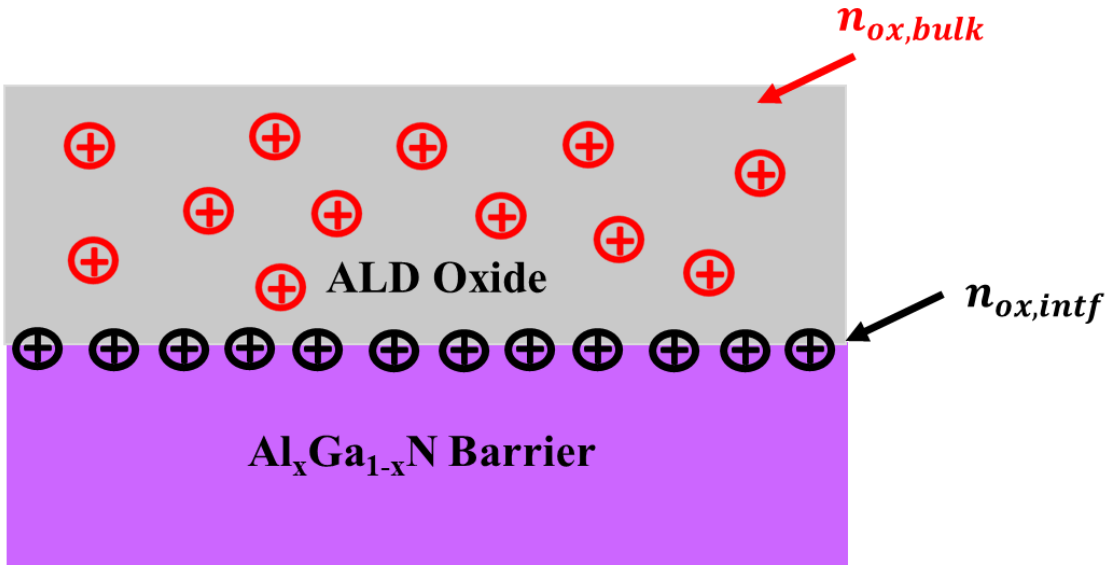


Figure 3.1 Schematic of bulk and interfacial charge distribution in ALD oxide on AxlGa1-xN barrier layer.

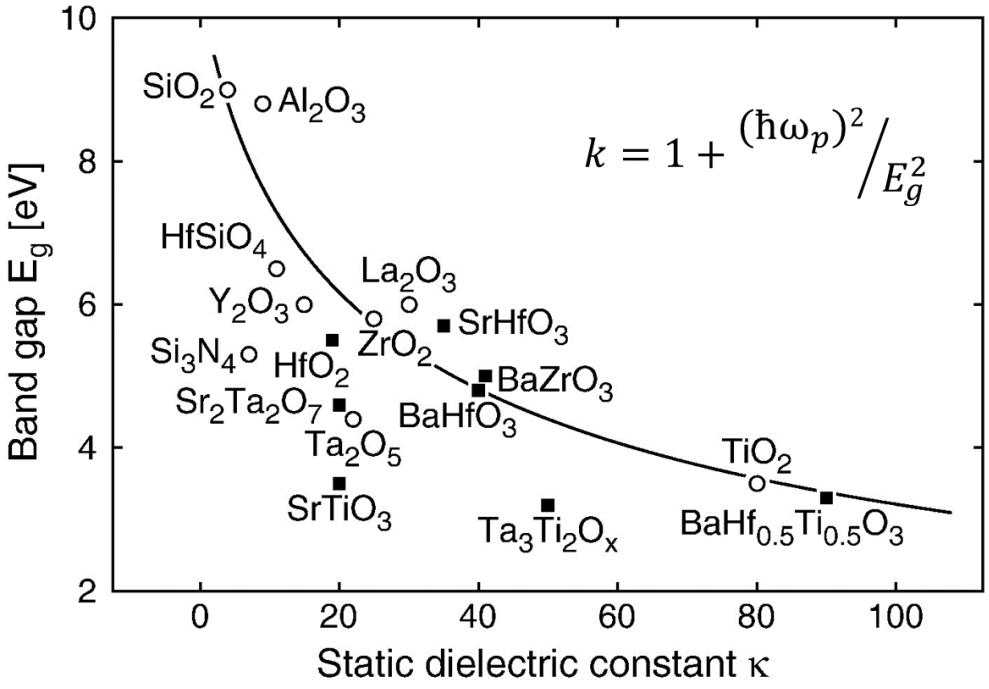


Figure 3.2 Bandgap and dielectric constant for well-known oxides.

however, no material satisfies both conditions simultaneously. In the later part of this chapter, we discuss performance of three different high-*k* dielectrics (ZrO_2, Al_2O_3 and TiO_2) and from experimental results we develop hybrid dielectric material that satisfies both high E_G and *k* conditions and enables fabrication of high-performance state of the art depletion and enhancement mode AlGaN-channel MOSHFETs.

3.2 Experimental Details:

3.2.1 Epilayer Growth:

The $Al_{0.6}Ga_{0.4}N$/ $Al_{0.4}Ga_{0.6}N$ structures in this study are grown on a high quality 3 μm thick AlN/Sapphire templates using metal organic chemical vapor deposition (MOCVD) system. All layers for this structure were grown at 1100 °C and 40 Torr. The off-axes (102) X-ray peak line width of the AlN template was 340 arc-sec which translates to a defect density of (1-3) $\times 10^8$ cm^{-2}. As seen from Figure 3.3 (a) it consists of a 85 nm reverse graded back barrier followed by 185 nm of $Al_{0.4}Ga_{0.6}N$-channel layer. There is a thin AlN spacer layer in between the channel and 15 nm $Al_{0.6}Ga_{0.4}N$ barrier layer. A 20 nm reverse graded $Al_xGa_{1-x}N$ (x=0.6-0.3) layer finishes the structure. The sheet resistance (R_{sh}) of the as grown 2" wafer was measured by the Lehighton contactless sheet resistance mapping system. The average R_{sh} value was found to be ~2300 Ω/sq (see Figure 3.3 (b)) for the sample that is used for ZrO_2 thickness dependent study. From mercury probe capacitance-voltage (C-V) measurement system the depletion voltage was estimated as ~ -11 V (Figure 3.3(c)). The structure is different from that used in the past to fabricate $Al_{0.4}Ga_{0.6}N$-channel MOSHFET by our group (Figure 3.4 (a)). More details about the epilayer structure can be found below.

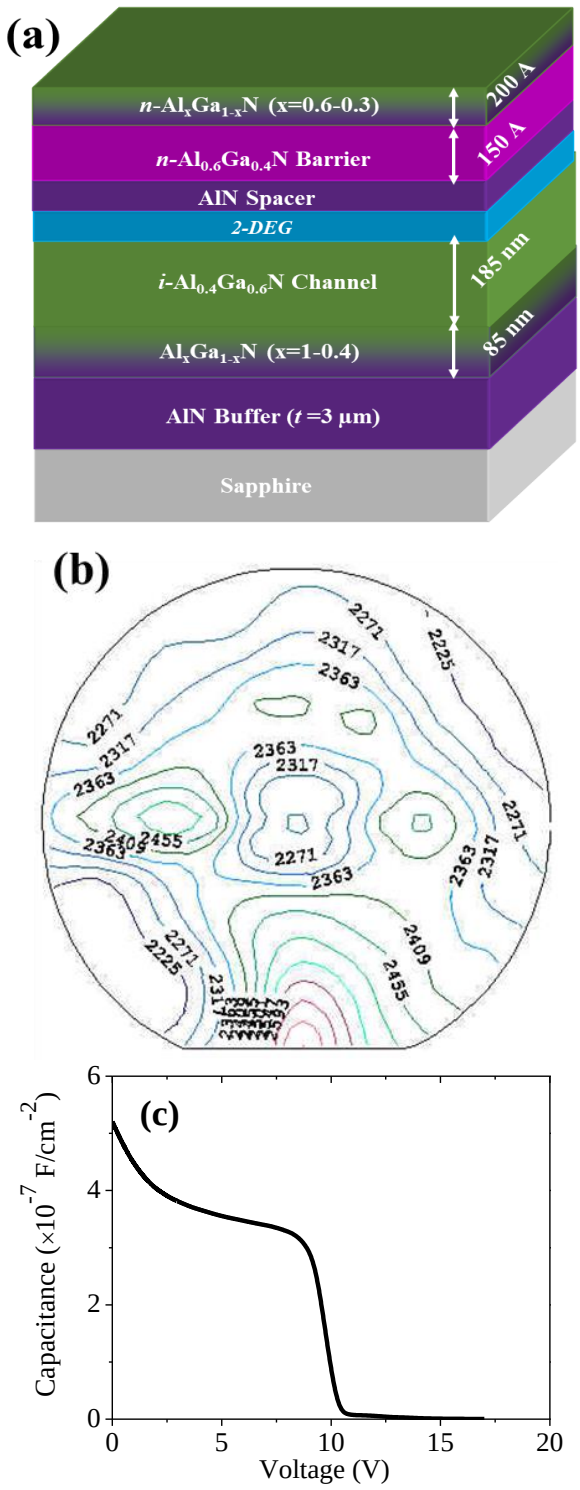


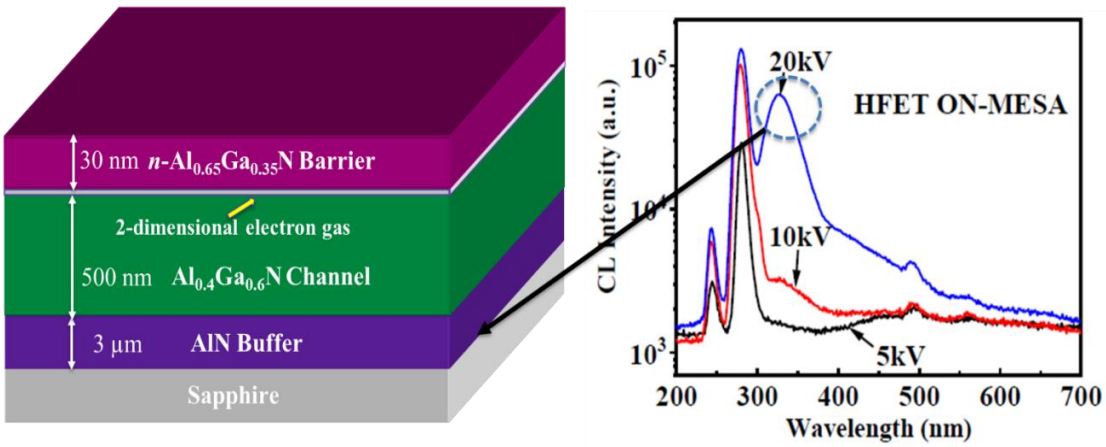
Figure 3.3 (a) Schematic of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ epilayer design for this study (b) Sheet resistance mapping using Lehighton contactless eddy current method (b) Mercury probe capacitance-voltage (C-V) characteristics of as grown $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET epilayer structure

3.2.1.a Graded back barrier:

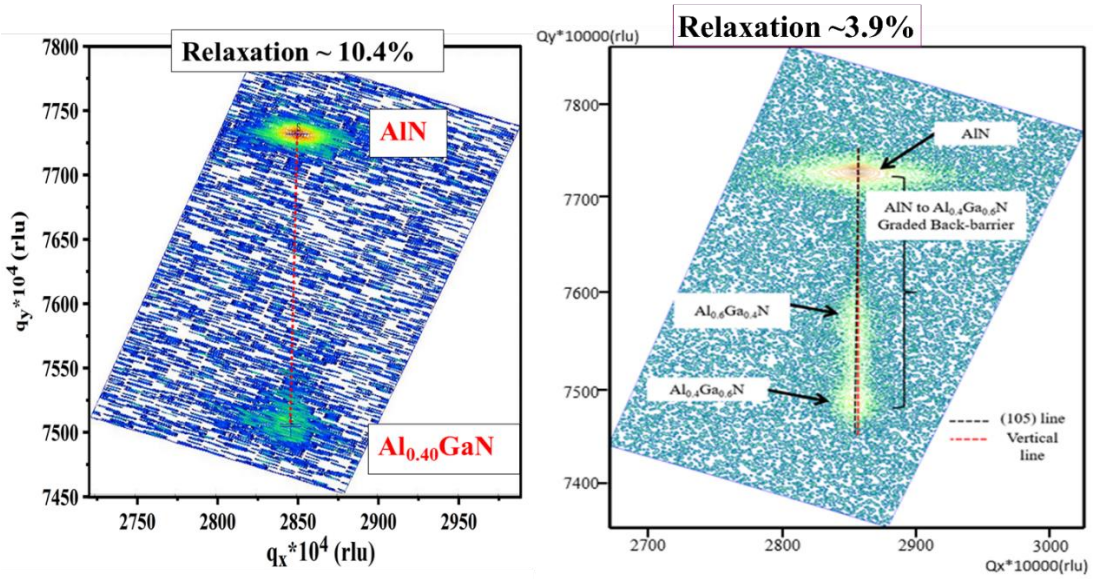
Due to the lattice mismatch between AlN and $Al_{0.4}Ga_{0.6}N$ layers, $Al_{0.4}Ga_{0.6}N$ layer relaxes after a critical thickness which creates defects at the interface. These defects scatter the channel electrons thereby reducing the device current. M. U. Jewel et. al., conducted acceleration voltage dependent Cathodoluminescence spectra to identify the location of the defects in the material. Figure 3.4 (a) shows that, as the voltage increases from 5 KV to 20 KV, the defect peak becomes more prominent indicating the presence of defect in the $Al_{0.4}Ga_{0.6}N$ layer and/or $Al_{0.4}Ga_{0.6}N$/AlN interface [43]. To mitigate the interfacial defects, one very effective method is lattice matching growth or reverse graded composition growth. The % relaxation of the graded and fixed $Al_{0.4}Ga_{0.6}N$ layers are presented in Figure 3.4 (b) using the reciprocal space lattice mapping data. It shows that epilayer structure with graded composition back barrier offers less relaxation epilayer with $Al_{0.4}Ga_{0.6}N$ layer.
The back-barrier design enables a reduction in leakage currents by screening the substrate-epilayer growth interface, which improves the ON-OFF ratios, drain-currents, and the sub-threshold swing (SS) [44][45].

3.2.1.b AlN Spacer:

One of the key material properties is electron mobility. For the AlGaN alloys, the low-field mobility is a strong function of alloy composition. Figure 3.6 shows the typical electron mobility plot as a function of alloy composition. The dominant scattering mechanism over nearly the entire composition range except the two endpoints is alloy scattering which tells that the electron mobility is degraded due to alloy scattering in AlGaN alloys, relative to the binary endpoints GaN and AlN. In III-Nitride heterostructure,



(a)



(b)

Figure 3.4 (a) (b) Schematic presentation of a $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ HEMT structure without back barrier and reverse graded contact layer (c) Cathodoluminescence of $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ structure (d,e) reciprocal space lattice mapping of HEMT structures without and with graded back barrier respectively.

the 2DEG generates at the heterostructure interface. In GaN/AlGaN HEMT, the use of AlN spacer layer has been found beneficial. It has been seen that, the 2DEG transport properties and the DC characteristics are strongly affected by the AlN spacer layer. The electron concentration so as the carrier mobility increases with the insertion of such spacer layer as the level of 2DEG concentration is virtually moved away from the interface. Similar benefits of using AlN spacer layer are expected in case of AlGaN-channel devices.

3.2.1.c Reverse Al-Composition graded contact layer:

AlGaN composition is graded from the barrier $Al_xGa_{1-x}N$ composition (x=0.6) to 30% Al AlGaN. $Al_{0.3}Ga_{0.7}N$ is typical barrier layer for GaN-channel HEMTs and making low resistance ohmic contact is already established on these layers. It is very important to heavily dope the reverse graded contact layer with n-type dopant such as [Si^+] in order to serve two purposes: 1) keep the contact region highly conductive to minimize any additional resistance being added by the contact layer 2) compensate for any negative polarization charge introduced because of Al-composition grading of the AlGaN. The reverse composition graded Si-doped $Al_xGa_{1-x}N$ (x from 0.6 to 0.3) layer assist with ohmic contact formation, by presenting an effective Schottky barrier height lower compared to that for a flat barrier. Figure 3.6 shows the simulated energy band diagram of a $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ heterostructure, where it is evident that the addition of reverse graded contact layer lowers the Schottky barrier height to 0.7 eV from 2.7 eV [46] for flat $Al_{0.6}Ga_{0.4}N$ barrier layer.

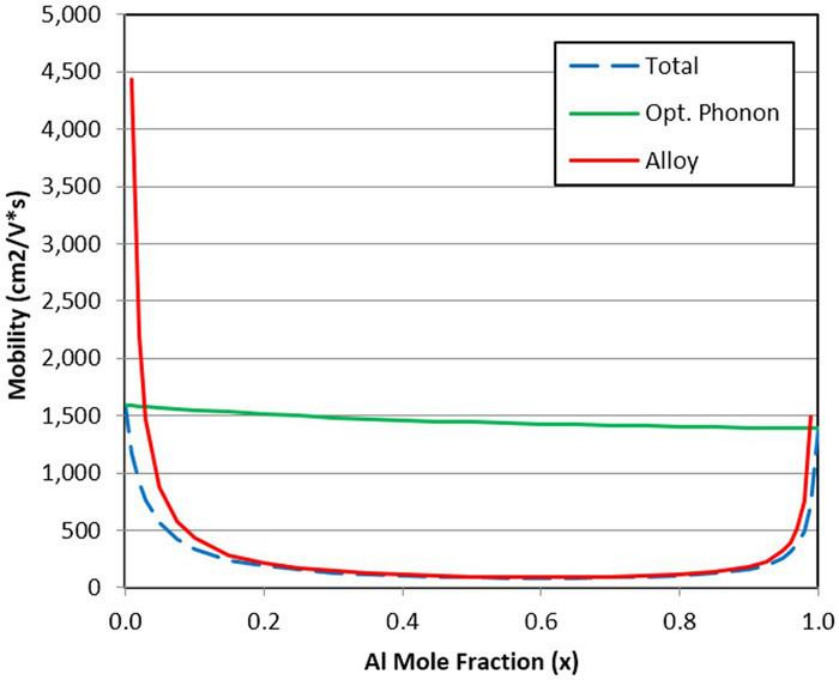


Figure 3.5 Mobility as a function of Al mole fraction (x) in $Al_xGa_{1-x}N$ s[10]

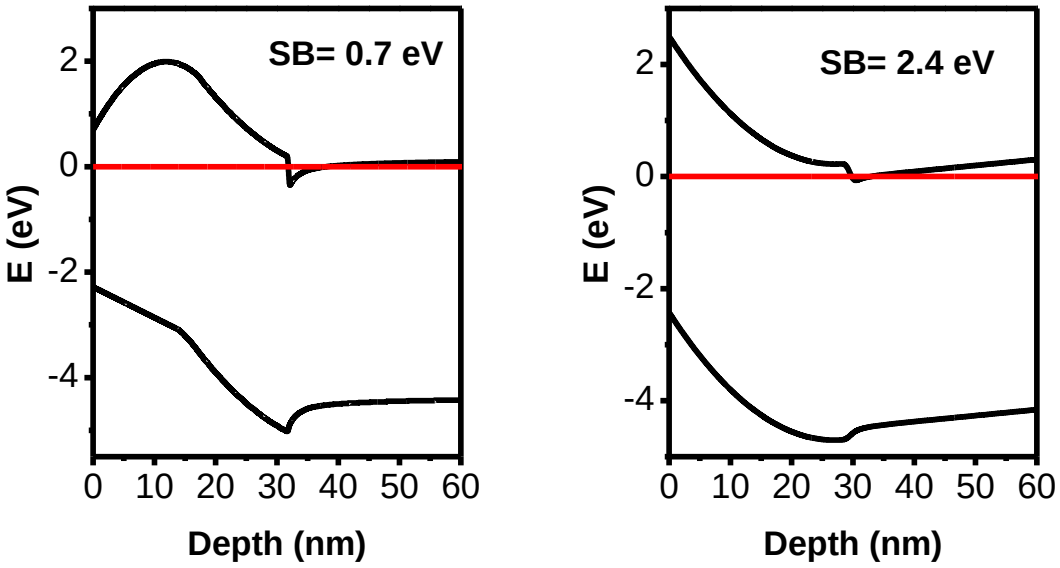


Figure 3.6 Simulated energy band diagram of a $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ structure with (left) and without (right) the reverse graded contact layer.

3.2.2 Device Processing:

The process flow for the fabrication of baseline $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ MOSHFET devices used in this study is shown below in Figure 3.7. The fabrication process starts with the mesa isolation which defines independent devices on the wafer. This is then followed by source-drain ohmic contact formation and by the atomic layer deposition of ZrO_2 and removal of oxide layer from the source and drain contact area. The Schottky gates are then formed on the ZrO_2 in between source and drain contacts. This is then followed by large probe pad deposition for measuring these devices.

The contact and etching patterns are defined using standard photo lithography system. All the contact deposition involved in this process flow are done using temescal BJD 1800 E-beam evaporation system with a lift-off process to define the contacts.

3.2.2.a Mesa Etching

GaN and related compounds are high temperature materials with strong bond strengths and excellent chemical stability. Inductively coupled plasma (ICP) sources has proven to be more efficient than reactive ion etching (RIE) for the nitrides due to its high-density of plasma [47]. Plasma density in ICP (10^{11}-10^{12} cm^{-3}) is typically 2 orders of magnitude higher than RIE (10^{9}-10^{10} cm^{-3}) thus improving the bond breaking efficiency in these strongly bonded semiconductors and the sputter desorption of etch products formed on the surface. The plasma in contained inside the dielectric shield, which is surrounded by an inductive coil powered with a 2 MHz RF source [48]. An alternating magnetic field is induced inside the chamber by the oscillating electric field, and this helps to produce high-density plasma due to confinement of electrons. The plasma etching can be broken down into as many as six primary steps as shown in Figure 3.8 [49].

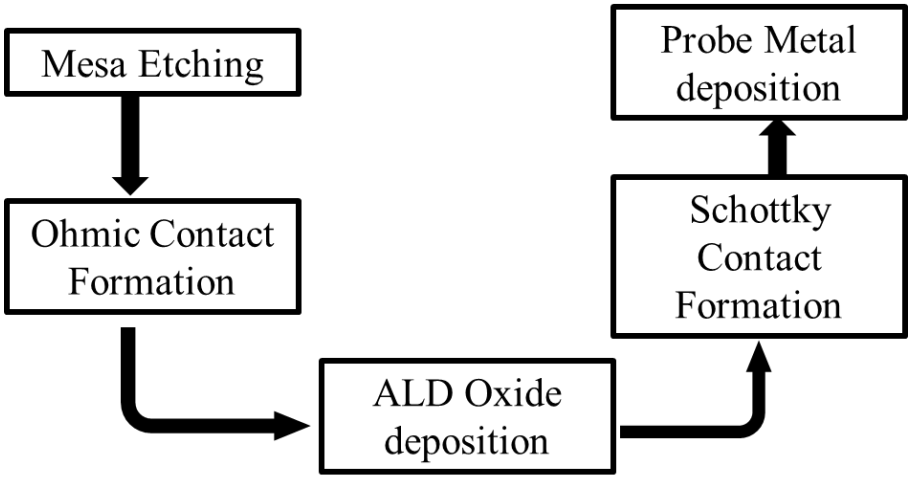


Figure 3.7 Process flow for the baseline $Al_{0.4}Ga_{0.6}N$-channel MOSHFET fabrication

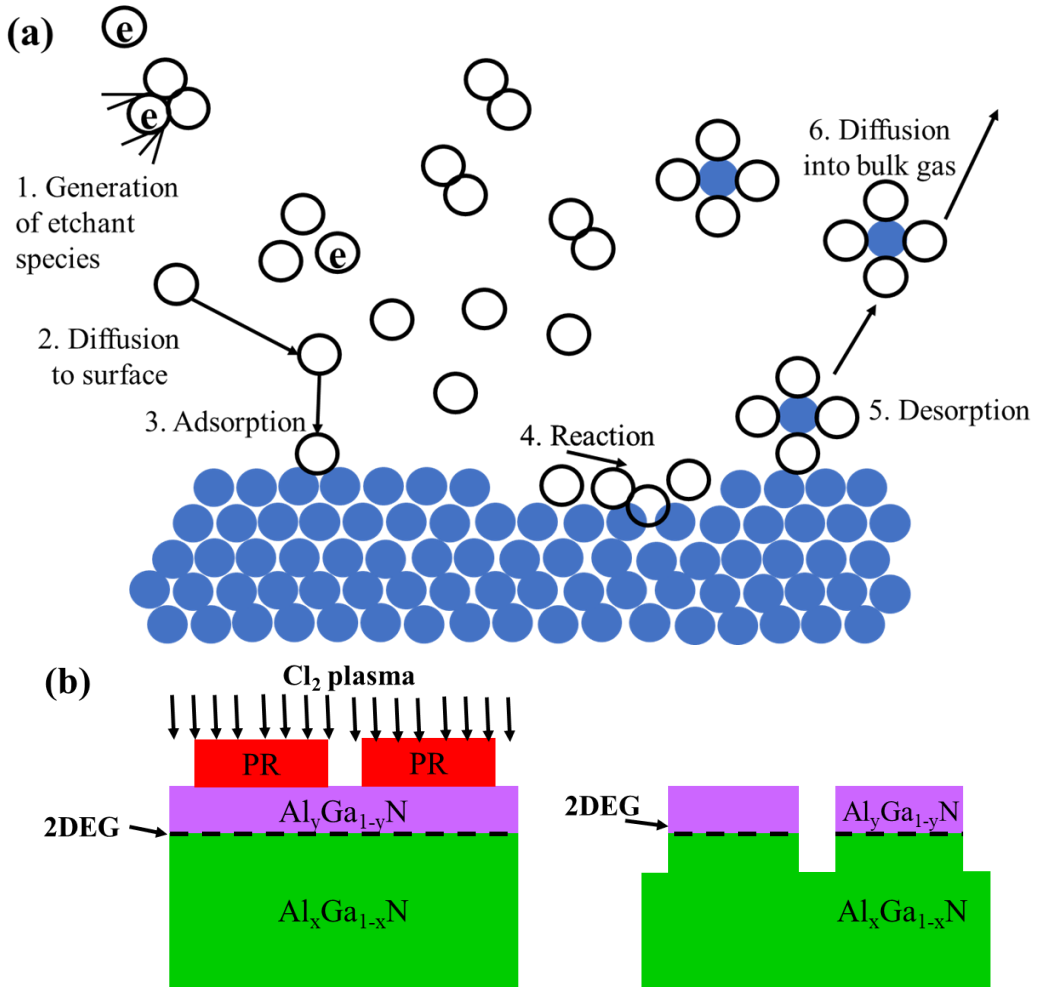


Figure 3.8 (a) Plasma etch process (b) Schematic of mesa formation

The first step is the production of the reactive species in the gas phase (1). In the second step, the reactive species diffuse into the solid (2) where they become adsorbed (3), diffuse over the surface and react with the surface (4). Finally, the reaction products leave the surface by desorption (5) and diffusion (6).

For III-Nitrides, the etch mechanism is dominated by the high ion bombardment and the etch rates are limited by the volatility of the III-halogen etch product. Cl_2, Br and I based chemistries are preferred to F due to the volatility of the etch product. Cl_2 chemistries are widely used for the etching of III-Nitride etching due to their less corrosiveness compared to Br and I.

The etch products for AlGaN are typically $AlCl_3$ and $GaCl_3$, meaning that the chlorine radical density and the ion density are the key factors [50]. For the fabrication of HFET and MOSHFET devices used for this dissertation study are done in ICP with a combination of Cl_2/Ar and BCl_3/Ar chemistries for higher etch rates and a better anisotropic etching. Previous investigations have shown that Cl_2/Ar plasmas can yield lower surface roughness and damage compared to plasmas with BCl_3 additives, although the latter is commonly added because of its ability to remove oxides that inhibit the initiation of etching [51].

The procedure of mesa formation starts with coating the wafer with photoresist (PR). This is followed by the pattern creation in the photoresist using the standard lithography process. The pattern in the photoresist is used as a mask for etching in the Cl_2 plasma. Figure 3.8 (b) shows how the photoresist pattern replicates the required mesa edges on the epilayer. After the etching is done, the photoresist is removed using organic solvents and the sample is then cleaned in H_2SO_4: H_2O_2 (3:1) solution to remove the residue left on

the surface. Mesa depth is measured using DEKTAK 6M Stylus Profiler. The typical etch depth for all samples used in this study is 300-400 nm.

3.2.2.b Ohmic Contact formation:

As outlined in the previous chapters, ohmic contacts of FETs are crucial quality factor in determining device performance. Good Ohmic contacts are required to obtain high drain saturation current, to reduce on- resistance, to minimize the power dissipation in the contacts. By definition, the type of metal semiconductor contact in which the current-voltage relationship maintain ohm's law i.e., linear and symmetrical under both forward and reverse bias voltage is called ohmic contact. The contact resistivity (ρ_c) for a high quality metal-semiconductor ohmic contact should be as low as possible. The contact resistivity is expressed by [6]:

$$\rho_c = \rho_{c0} \exp\left(\frac{2\Phi_B}{\hbar}\sqrt{\frac{\varepsilon_s m^*}{N}}\right) \qquad (3.2)$$

Here, Φ_B is the Schottky barrier height, m^* is the effective mass of majority carrier, N is the doping density and ρ_{c0} is the constant depends on metal and semiconductor. From above equation it is evident that, contact resistivity strongly depends on the metal-semiconductor Schottky barrier height and doping density. Since the depeltion width $W_d = {}^{1}/_{\sqrt{N}}$, if N increase W_d will decrease. The Schottky barrier height is the difference between metal work function and the semiconductor electron affinity ($q\Phi_m - q\chi_s$). In $Al_xGa_{1-x}N$, as the x value keeps increasing the electron affinity keeps decreasing, resulting higher schottky barrier height for high-Al composition AlGaN. Moreover, it is difficult to dope ultrawide bandgap $Al_xGa_{1-x}N$ materials because of its wider bandgap nature that

results poor metal-semiconductor contact. The combined effect of high barrier and low interfacial doping density results in high contact resistivity.

Making ohmic contact to wide bandgap materials like GaN and low-Al mole fraction ($x<0.3$) AlGaN is well matured. The standard metallization schemes for these materials are X/Al/Y/Au, where X is typically Ti/Zr/V/Nb and Y is Ni, Ti, Mo, Pt or Nb [52]. The work function of different metals are shown in Table 3.1. In GaN-channel HEMTs Ti is standard metal while in UWBG AlGaN-channel HEMTs, Zr based ohmic contacts have shown better performance over Ti based contacts.There are two main mechanisms for low resistance ohmic contact formation on AlGaN/GaN structure with these quaternary metallization stacks: during high temperature annealing the exchange reaction between metal and semiconductor creates spikes or protrusions that penetrates through the barrier and directly connects to the 2DEG as shown in Figure 3.9 (a). The other mechanism suggests that during high temperature annealing of Ti based metal stacks reacts with the AlGaN and form TiN, thus creating N vacancies (V_N), which act as donors and causes the Fermi level pinning that results in a tunnel junction (see Figure 3.9 (b)) [53].

X(Ti, Zr, V, Nb): These metals can easily react with AlGaN surface at high temperature and form XN (TiN, ZrN), these are believed to have lower work function than the Ti or Zr metal itself [54][55]. Moreover, it creates N vacancies that act as n-type dopant [56]. This in turn reduce the tunneling width and favors electron tunneling. However, mostly accepted explanation is the penetration of XN throught he barrier and directly connecting the 2DEG. For UWBG AlGaN materials it is observed that, Zr based metal cofntact penetrates more effectively through the barrier in contrast to the Ti based metal contact [56].

Table 3.1 Metal work function

Metal	Work function (eV)
Ti	4.33
Al	4.25
Ni	4.8
Au	4.5
Pd	5.1
Pt	5.3
Zr	4.05
V	4.3
Nb	3.95-4.87

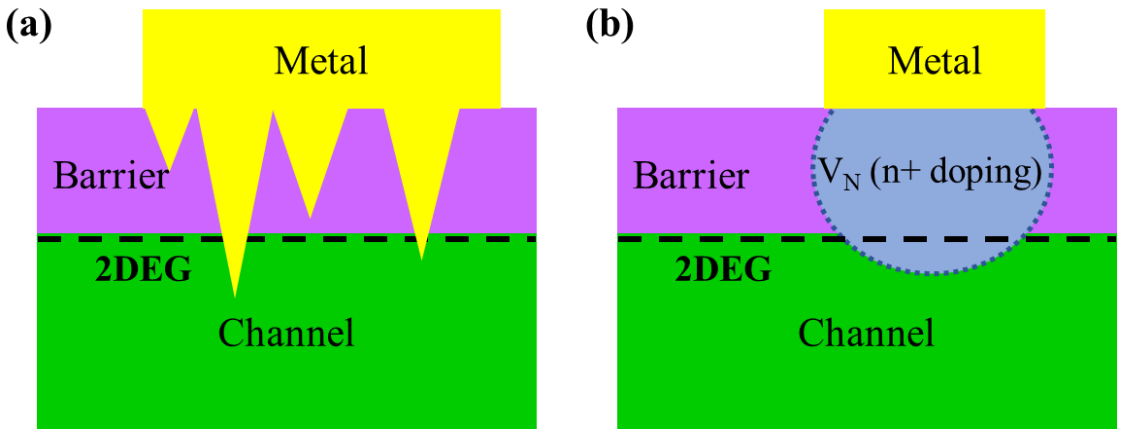


Figure 3.9 (a) Ohmic contact formation by lowering Schottky barrier contacts via interfacial reaction between metal and semiconductor, resulting metal spike (b) reaction of metal with semiconductor resulting nitrogen vacancies and subsequent n-type doping.

Aluminum (Al): At high annealing temperature Al reacts with the underlaying layer and forms Al_3X which prevents oxidation of the underlaying layer. Al also reacts with N and causes N vacancies, thus increasing the n-type doping.

Y (Ni, Ti, Mo, Pt or Nb): The role of this layer is to act as a diffusion barrier between the Au and Al to prevent the formation of a highly resistive alloy called ‘purple plague‘. This layer has an important role to maintain good surface morphology and contact edge-acuity. Molybdenum is one of the metals which maintains very good edge-acuity at very high temperature annealing due to its high melting point and robustness [57][58].

Gold (Au): The top Au layer prevents oxidation of the bottom X and Al layers during high temperature annealing. Gold is used on contacts and connectors because it has excellent corrosion resistance and high electrical conductivity.

The ohmic contact processing starts with photoresist coating of the sample and define ohmic pattern using photolithography. Before ohmic metal deposition the sample is cleaned in $NH_4OH:H_2O$ (1:4), $HCl:H_2O$ (1:1) and $HF:H_2O$ (1:4) respectively to remove residual resist particles and surface oxide from the defined ohmic window. It was found that HCl-based solution is more effective in removing oxides and leaves less residue but HF is more effective in removing carbon and hydrocarbon contamination [59]. The metal stack is deposited using E-beam metal deposition system followed by lift-off process to remove metal from outside of the ohmic area. This is then followed by high temperature annealing to create ohmic contct.

The ohmic metallization scheme for the devices used in this study is Zr/Al/Mo/Au (150/1000/400/300 Å). Annealing of these contacts is done at 950 °C under N_2 ambient

using rapid thermal annealing (RTA) [19]. The contact resistance is measured by transmission line method (TLM). Figure 3.10 (a) shows a typical TLM pattern where the spacing between the contacts increases. The total resistance measured between ohmic contacts is:

$$R_T = 2R_C + R_{sh}\frac{L_{n,n+1}}{W} \qquad (3.3)$$

where L is the distance between contacts and W is the width of the ohmic pads. R_C is the specific contact resistivity and R_{sh} is the sheet resistance. Figure shows total resistance measured from the TLM pattern as a function of distance between contacts.The estimated R_c and R_{sh} are 2.27 Ω-mm and 2280 Ω /□ respectively. R_{sh} value is consistent with that measured on as grown sample using eddy current method.

3.2.2.c ALD Oxide Deposition:

The deposition of ZrO_2 for the gate isolation in MOSHFET is typically done using the ALD technique[60]-[65]. The ALD process requires two chemicals called precursors. These prcursors react with the surface of a material one at a time in a sequential , self limiting manner. In this process, a gas is introduced in the chamber that reacts with the surface of the wafer, leaving the whole substrate coated in a single layer of atoms. Then, because there is no more surface to react with, the deposition stops. The gas is evacuated from the chamber and replaced with a second gas, one that chemically reacts with the layer of atoms just deposited [21]. Figure 3.11 demonstrates the formation mechanism of ZrO_2 coating using TDMAZ and water as precursors. This process includes two half-reactions, indicated as follows:

$$2^{\#}OH + Zr[N(CH_3)_2]_4 \rightarrow {}^{\#}O\text{-}Zr[N(CH_3)_2]_2 + 2(CH_3)_2NH\ \#O \qquad (R1)$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\quad |$$

$$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\quad {}^{\#}O$$

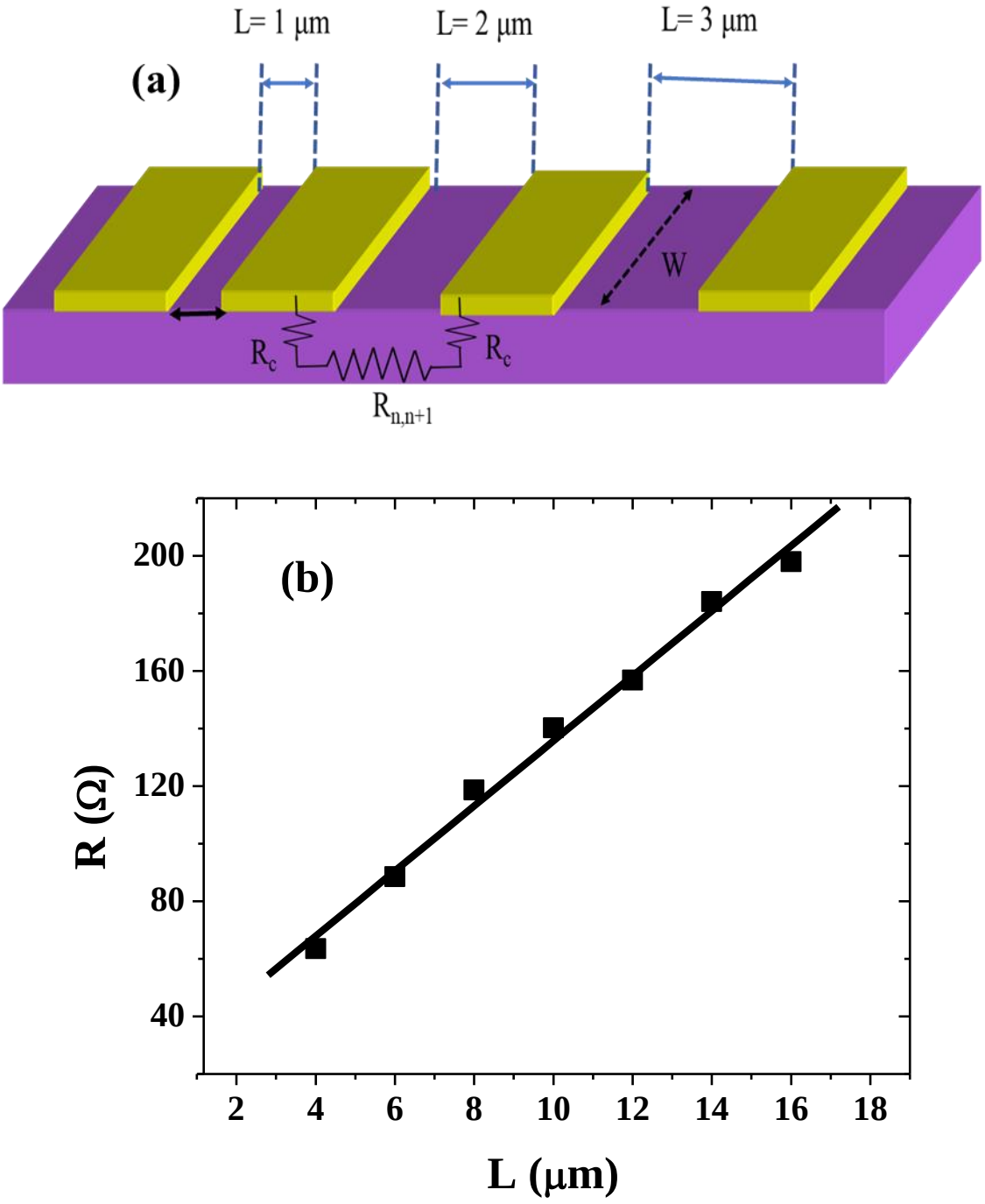


Figure 3.10 (a) Schematic diagram of TLM pattern (b) Resistance as a function of distance plot to extract contact and sheet resistances

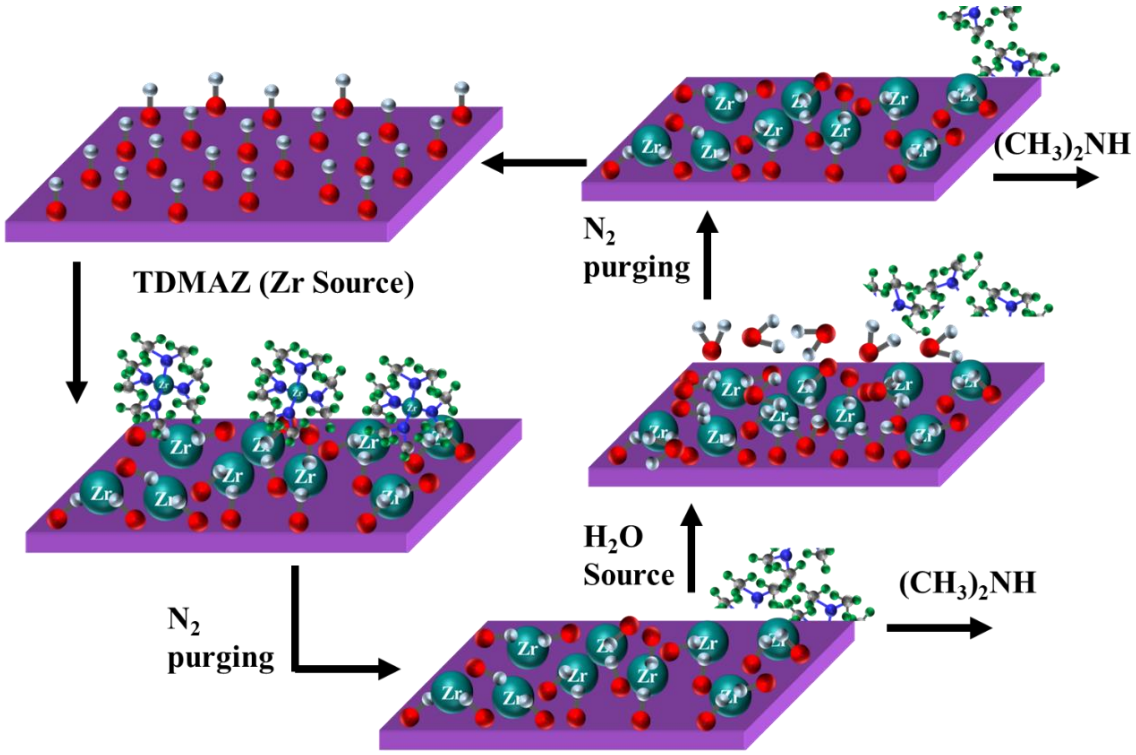


Figure 3.11 Schematic of surface reaction during ALD deposition process

$$^{\#}O\text{-}Zr[N(CH_3)_2]_2 + 2(CH_3)_2NH\ \#O + 2H_2O \rightarrow {}^{\#}O\text{-}Zr(OH)_2 + 2(CH_3)_2NH \quad (R2)$$

where, the hydroxy (OH) group is originated from the natural oxidation of AlGaN, and the octothorpe (#) indicates the connection of these groups with the substrate. The overall reaction is as follows:

$$Zr[N(CH_3)_2]_4 + 2H_2O \rightarrow ZrO2 + 4(CH_3)_2\,NH$$

As seen from the Figure 3.11, the ALD process contains two repeatitive steps. In step 1, certain amount of Zr source precursor (TDMAZ) is introduced in the chamber to induce a surface reaction with the active sites like -OH which forms an intermediate layer $Zr[N(CH_3)_2]_2$ and during this course the by-product $(CH_3)_2$ NH is released which is removed with the residual TDMAZ by the N_2 purge. During the step 2, a certain amount of oxygen (O) source precursor H_2O gas is introduced for another surface reaction with the active sites of intermediate layer i.e., $Zr[N(CH_3)_2]_2$ to form thye target product ZrO_2 as well as new active sites. The residual H_2O gas and the by-product $(CH_3)_2$ NH are removed by the N_2 purge. This process is recyclable, so that the thickness of the film can be easily controlled by the number of cycles.

For the current study, GEMSTAR6 series ALD system is used to deposit the high-*k* oxides. For threshold control study, the 2" $Al_{0.6}Ga_{0.4}N$/ $Al_{0.4}Ga_{0.6}N$ HEMT wafer was diced into four quarters and three quarters were used to deposit 10, 20 and 30 nm ZrO_2 respectively while the fourth quarter was used to fabricate control HFET device. For study with three different dielectrics, three quarters from another 2" wafer with contact resistance 1.64 Ω-mm and sheet resistance ~1900 Ω /□ were processed with 10 nm ZrO_2, TiO_2 and Al_2O_3 and fourth quarter was used for HFET fabrication.

The precursors used for ZrO_2, Al_2O_3 and TiO_2 are tetrakis (dimethylamido) zirconium (IV), trimethylaluminum (TMA) and tetrakis(dimethylamino) titanium (TDMAT), respectively. The TDMAT precursor was heated to 75°C to ensure sufficient vapor pressure to attain a saturated linear growth rate of 0.6 Å $cycle^{-1}$. Deposition of the TiO_2 film was initiated by 15 *in situ* plasma pulses prior to alternating precursor pulses for film growth.[66][67][68]. For the ZrO_2 and Al_2O_3 gate-oxide films thermal ALD processes at 200°C and 250°C respectively were used. The TDMAZ precursor was also heated to 75°C in order to achieve a linear growth rate of 0.7 Å $cycle^{-1}$. For both the Al_2O_3 and the ZrO_2 films, the deposition was initiated with 15 water pulse prior to the typical AB pulsing sequence to deposit the gate dielectric to ensure saturation of hydroxyl groups at the AlGaN surface required for conformal ALD nucleation.[69][70][71]

3.2.2.d ZrO_2 characterization:

The thickness of the ZrO_2 films was obtained using witness samples grown on Si substrates in the same run, giving thickness 10nm, with an index of refraction 2.13 from ellipsometry, very close to the ideal value of 2.15 expected for ZrO_2 [72][73]. The stoichiometry of the films was confirmed by XPS (Figure 3.12 (a) and (b)). Neither carbon, nor nitrogen were observed, indicating complete ligand exchange during ALD, underscoring the high purity of the films. This is consistent with the close to ideal index of 2.13 measured by ellipsometry. The relative intensities of the Zr3d and O1s core levels (Figure 3.12 (a) and (b)) are also consistent with stoichiometric ZrO_2 [74]. XRD showed no sharp peaks, indicative of highly amorphous films.

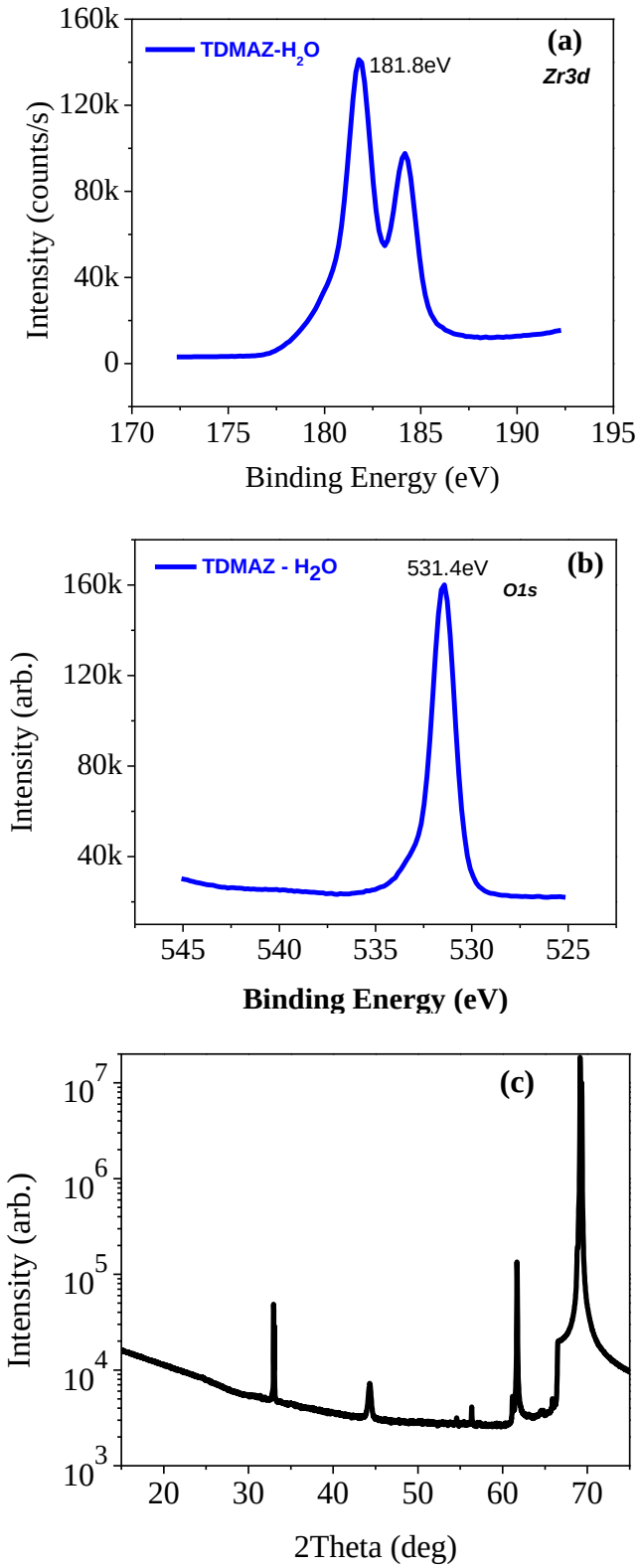


Figure 3.12 (a) The 3d core level XPS spectra (b) O 1 s photoelectron spectra of ZrO_2 dielectric (c) XRD of ZrO_2 dielectric film.

3.2.2.e Gate Electrode Fabrication:

The gates are defined using the maskless aligner- Heidelberg MLA100 instrument. The lithography procedure used in this current study for 1.8 μm gate definition includes:

1. Coating the sample with S5218 photoresist and post baking at 85°C
2. Aligning the gates with respect to the ohmic contacts and exposing it with a dose 220 mJ/cm^2.
3. Thermal image reversal at 110°C for lmin followed by a flat exposure for 30sec
4. Developing in Microposit MF 26A for l min.

Once the gates are defined, the sample is baked at 85 °C for 5 minutes before loading it in the E-beam metal deposition system to remove any moisture from the sample. After the gate metal deposition, lift-off process is used to remove the metal except from the gate region. Figure 3.13 shows the microscopic image of a 100×6 μm^2 device after gate lift-off. Gated transmission lined model (GTLM) test structures with gate-lengths ranging from 10 to 100 μm were also fabricated for extracting sheet charge density (n_s) and mobility (μ). For the current study, Ni/Au schottky contacts are used as gate metal, due to its superior sticking property and metal work function.

3.2.2.f Contact probe deposition:

To measure these MOSHFET devices, thick contact pads are required. These contact pads are the extensions of the gate and ohmic contacts of the device outside the mesa region. Figure 3.14 shows the microscopic image of the device with the contact pads.

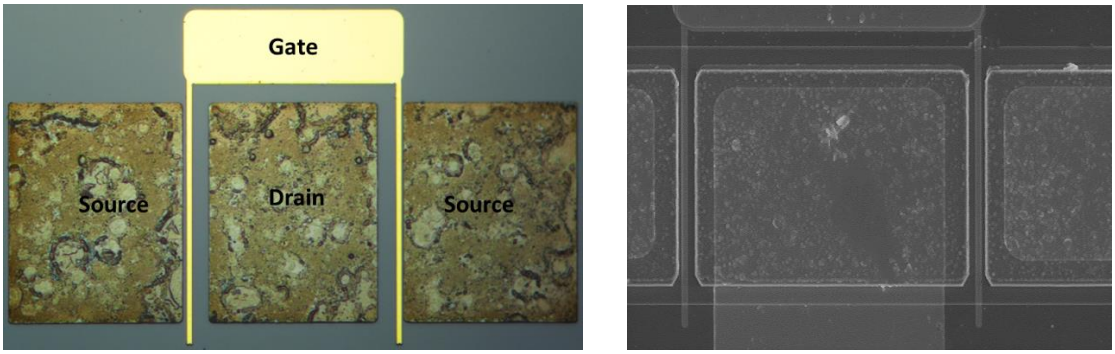


Figure 3.13 Microscopic (left) and SEM (right) image after gate lift-off

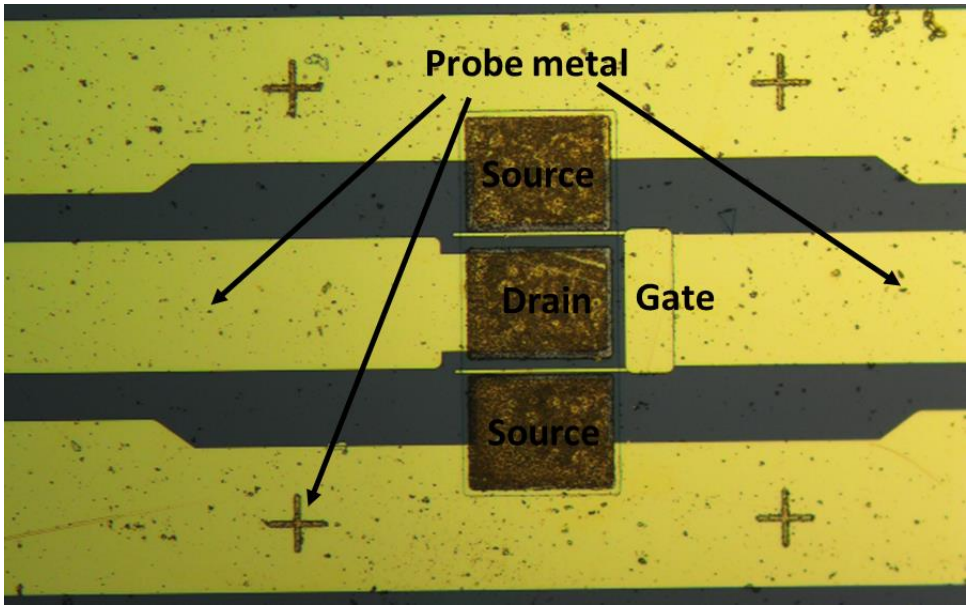


Figure 3.14 Microscopic image of the device after probe metal deposition

The contact pad lithography is done using the standard lithography technique as used for the ohmic contact formation. Ti/Au (20/300 nm) metal contacts are used as the contact pads for our devices.

3.2.2.g Post Deposition Annealing:

Post deposition annealing of ALD dielectrics can influence the crystal quality and reduce fixed charges and the trap density at the oxide/semiconductor interface [75][76]. However, selecting the optimal annealing temperature is a very crucial issue. If the temperature is too low, there is no significant influence on $n_{ox,intf}$ and $n_{ox,bulk}$. If the temperature is too high, recrystallization of the ideally amorphous dielectric, can lead to higher leakage currents through the grain boundaries [77]. J. Liu et al. reported that, the onset of crystallization starts around 210 °C and above 350 °C it completely changes to a crystal structure [75]. The anneal temperature for the ideal optical density was found to be around ~300 °C. Thus, for our study reported here, we selected a 300°C post-deposition anneal of the gate-dielectrics to maximize its influence on the bulk/interface charges and the interface trap density without changing the crystalline structure. The MOSHFET devices were taken through a two-step post deposition annealing procedure on a hotplate in ambient atmosphere at 250 °C and 300 °C for 30 minutes at each temperature. The devices were characterized both before and after the annealing step. No noticeable differences in device characteristics were seen after the 250 °C annealing while significant differences were observed after the 300 °C anneal. Thus, the reported results all correspond to the 300 ^{0}C anneal.

3.3 MOSHFET Characterization:

3.3.1 Characterization of ZrO_2 MOSHFETs with different thickness:

3.3.1.a MOSHFET characteristics:

The DC output and transfer characteristics were measured using a parameter analyzer Agilent 4155C and the capacitance-voltage (C-V) measurements were done using HP 4284A LCR meter. Figure 3.15 shows the C-V characteristics of MOSHFETs with different gate dielectric thickness before and after annealing that was measured on gated TLM structures. The 2DEG charge density shown in Figure 3.16 was extracted using capacitance-voltage (C-V) measurement giving an on-state sheet electron density n_s ~1-4×10^{13} cm^{-2} (Table 3.2) for the various devices of this study. Figure 3.17 shows output characteristics for all the MOSHFETs before and after annealing, where good saturation behavior is seen with current densities ~0.5A/mm in the 1.8 µm gate length devices. The output current for the Schottky gated device is ~ 0.24 A/mm at gate voltage VG=+2 V, while all the oxides seem to provide large forward gate swing, thus increasing the current ~2×.

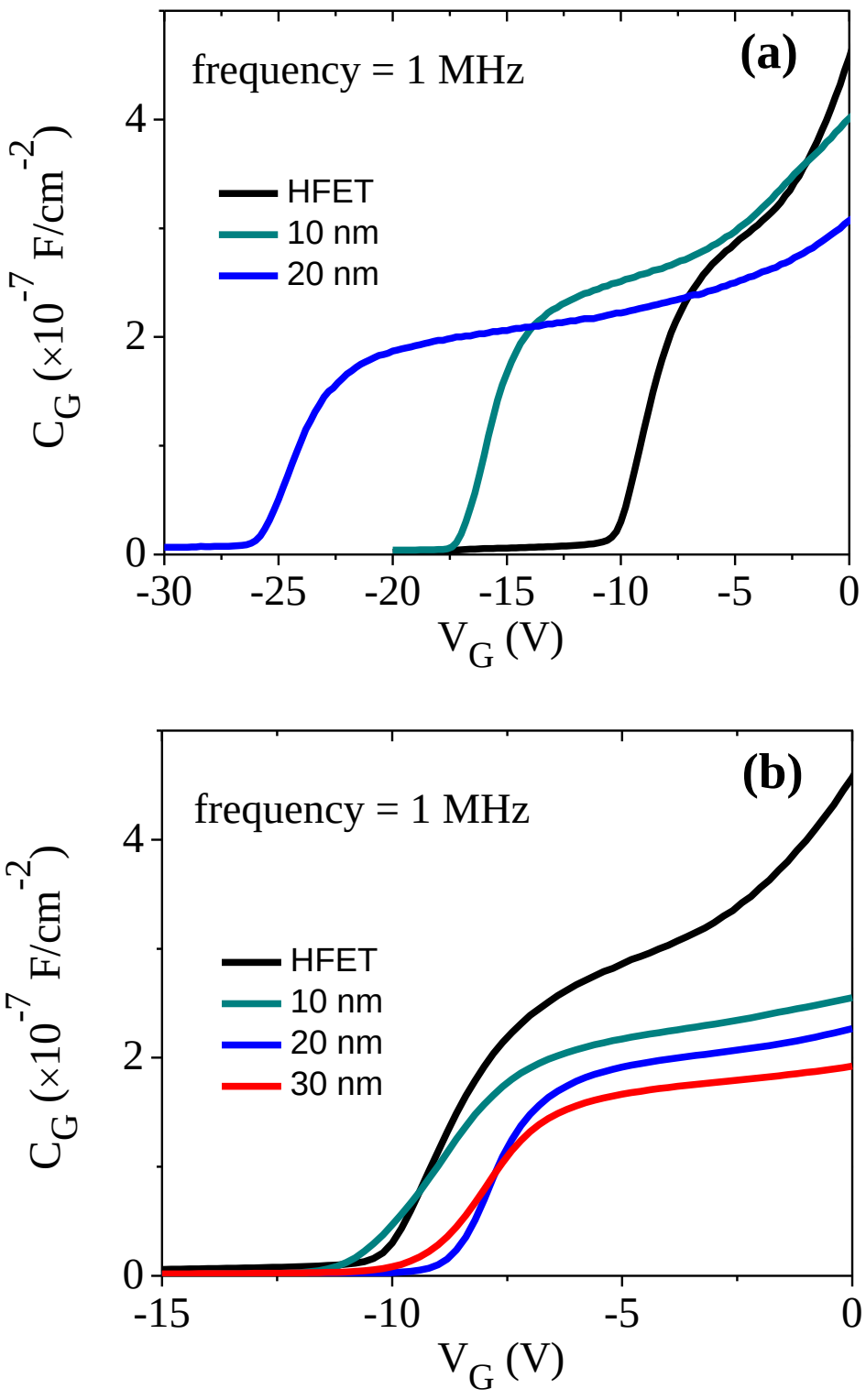


Figure 3.15 Capacitance-voltage (C-V) characteristics of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs before (a) and after (b) annealing.

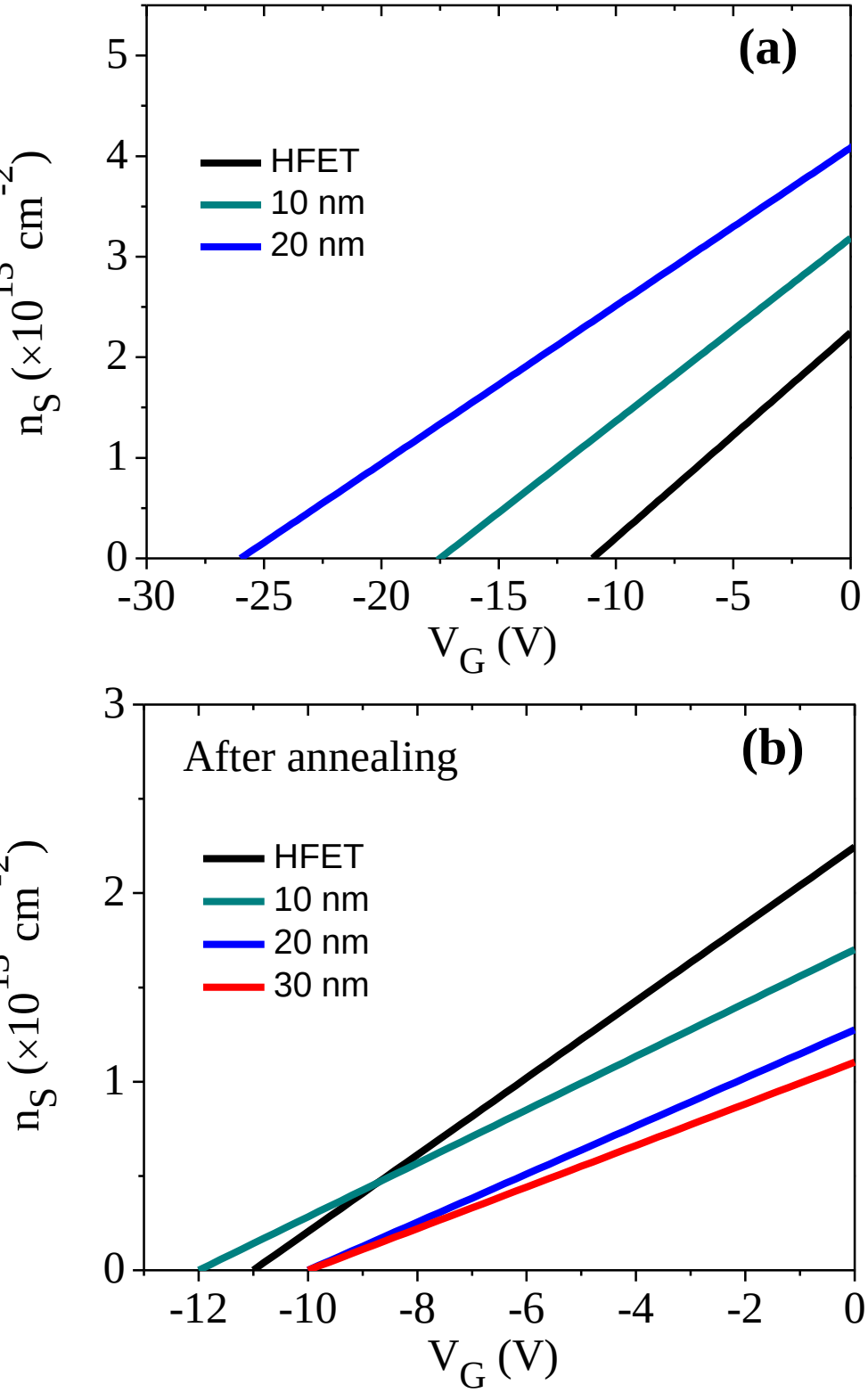
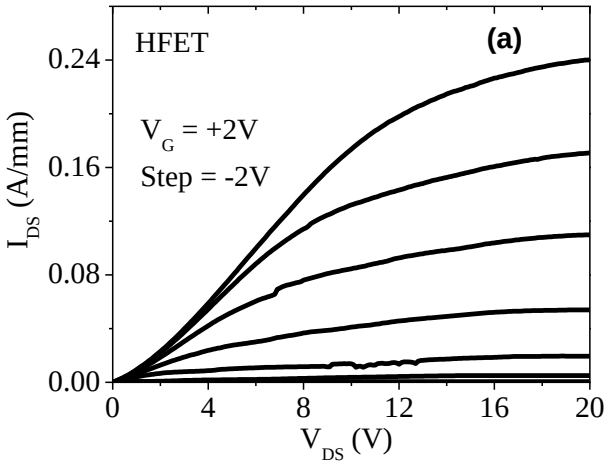
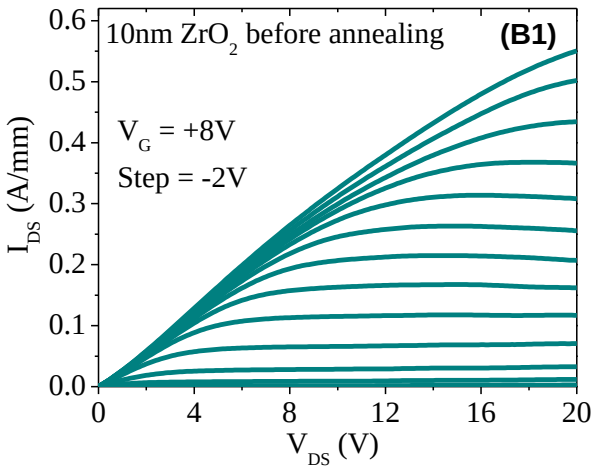


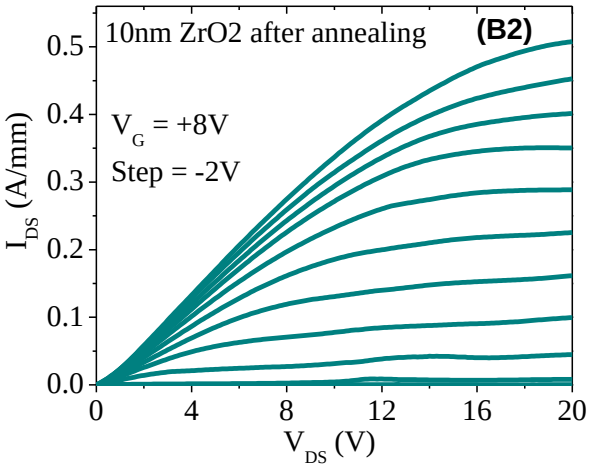
Figure 3.16 2DEG carrier density as a functsion of gate voltage of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs before (a) and after (b) annealing.

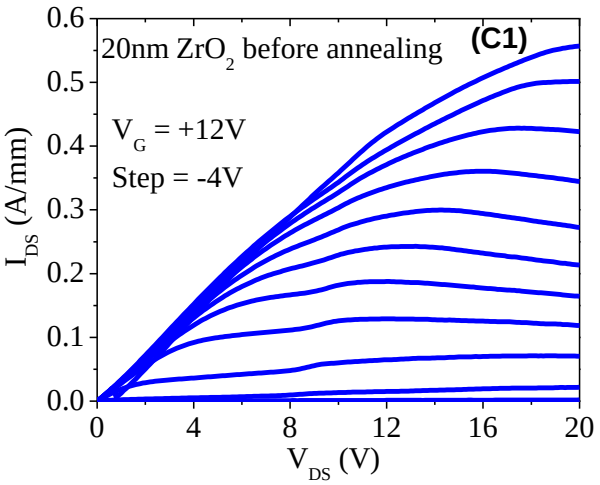
Table 3.2 Summary of MOSHFET device characteristics with different ZrO_2 thickness before and after the 300 ^{0}C anneal.

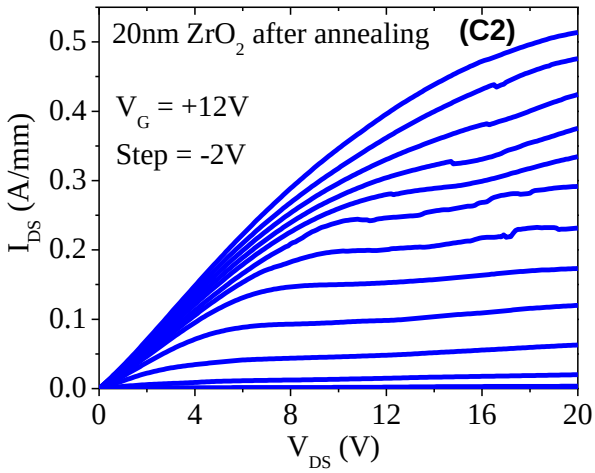
	HFET	10nm		20nm		30nm	
		Before	**After**	**Before**	**After**	**Before**	**After**
I_D(A/mm)	0.24 at V_G=+2V	0.55 at V_G=+8V	0.509 at V_G=+8V	0.558 at V_G=+12V	0.515 at V_G= +12V	0.595 at V_G=+15V	0.504 at V_G=+18V
I_G(A)	5×10^{-6} at V_G=-20V	6×10^{-11}at V_G=-20V	8×10^{-9}at V_G=-20V	1.1×10^{-9}at V_G=-20V	4×10^{-11}at V_G=-20V	1.7×10^{-9}at V_G=-40V	1.5×10^{-9}at V_G=-40V
off state current (A) from Transfer curve	2×10^{-6}	4×10^{-9}	6×10^{-9}	5×10^{-7}	2×10^{-11}	2×10^{-7}	6×10^{-10}
V_T(V)	-10.8	-20.8	-13.1	-25.5	-12.1	-33.7	-12.2
SS (mv/decade)	378	252	210	575	105	255	116
N_s(cm^{-2})	2.5×10^{13}	3.2×10^{13}	1.5×10^{13}	3.8×10^{13}	1.2×10^{13}	4×10^{13}	1.06×10^{13}


HFET
(a)
V_G = +2V
Step = -2V
I_{DS} (A/mm)
V_{DS} (V)
0.00
0.08
0.16
0.24
0
4
8
12
16
20


10nm ZrO_2 before annealing
(B1)
V_G = +8V
Step = -2V
I_{DS} (A/mm)
V_{DS} (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0
4
8
12
16
20


10nm ZrO2 after annealing
(B2)
V_G = +8V
Step = -2V
I_{DS} (A/mm)
V_{DS} (V)
0.0
0.1
0.2
0.3
0.4
0.5
0
4
8
12
16
20


20nm ZrO_2 before annealing
(C1)
V_G = +12V
Step = -4V
I_{DS} (A/mm)
V_{DS} (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0
4
8
12
16
20


20nm ZrO_2 after annealing
(C2)
V_G = +12V
Step = -2V
I_{DS} (A/mm)
V_{DS} (V)
0.0
0.1
0.2
0.3
0.4
0.5
0
4
8
12
16
20

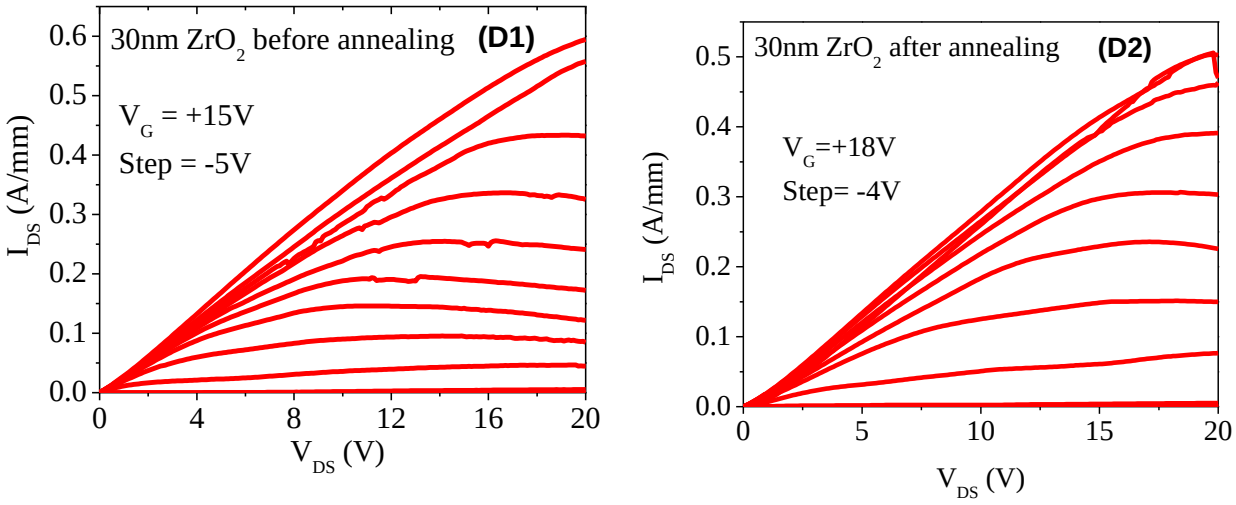
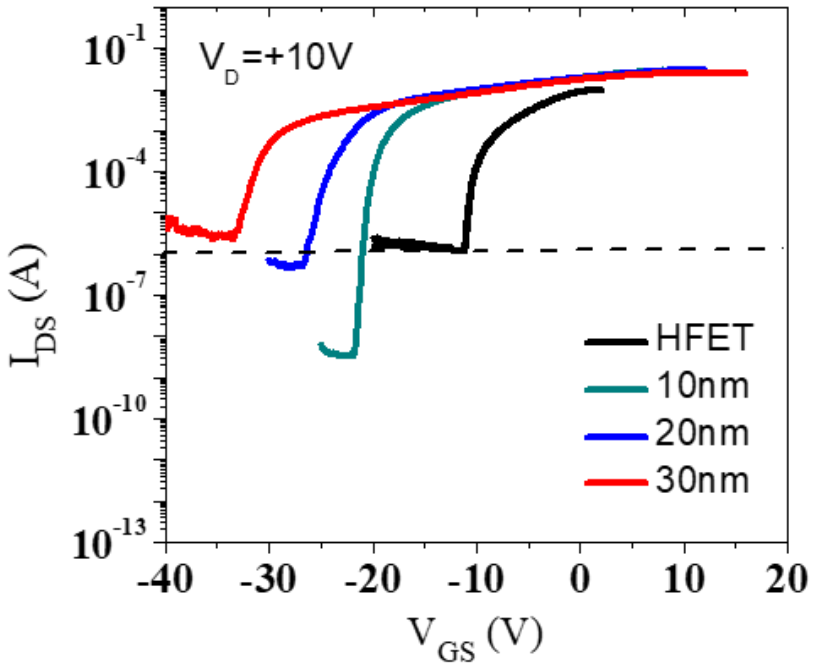


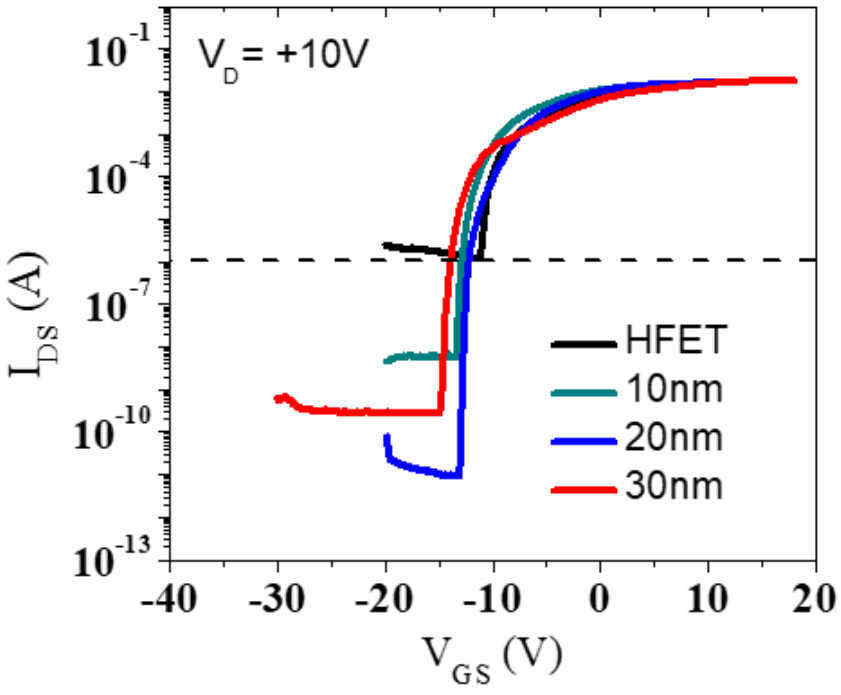
Figure 3.17 Output characteristics of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ (a) HFET and MOSHFETs with 10 nm(B), 20 nm (C) and 30 nm (D) ZrO_2. Numbers 1 and 2 represents the un-annealed and annealed condition respectively.

Figure 3.18 shows the transfer characteristics of the 1.8 μm gate length devices with at a drain bias V_{DS} = +10 V. Due to their extremely low gate leakage, MOSHFET devices can operate at much higher positive gate voltages as compared to HFETs, which lose the gate control at $V_G \geq 2V$ due to high gate conduction. For the 30nm-thick dielectric MOSHFET, at V_G =+14 V the channel current 0.5A/mm was achieved, which is twice as high as that of HFET (Table 3.2). Further increase in the gate forward bias does not lead to current increase due to limited 2DEG channel capacity and real-space charge transfer from 2DEG to dielectric-barrier interface [78]. As seen from Figure 3.18 (a), the un-annealed MOSHFET devices show very large threshold shift compared to an HFET. V_{TH}, which was defined as the gate voltage V_{GS} at which channel current I_{DS}=1μA, or 20μA/mm had a large negative shift immediately after deposition (Figure 3.18), increasing monotonically with t_{ox}. V_{TH} reaches as high as -33.7V for 30nm thick ZrO_2 making devices unusable in practical applications. The leakage current in the off-state for MOSHFETs (for all t_{ox}) is reduced by more than two orders as compared to the control HFET.

Post-deposition annealing showed drastic improvement in the V_{TH} in all MOSHFETs where the biggest V_{TH} shift occurs in 30 nm ZrO_2 from -33.7 V to -12.2 V. Interestingly, after the anneal, V_{TH} only showed a weak t_{ox} dependence, suggesting that the interfacial charge $n_{ox,intf}$ has been significantly changed. The significantly lower negative V_{TH} translated to a reduction in the on-state 2DEG n_s from ~2-3×10^{13} to ~1×$10^{13}$$cm^{-2}$, in rough proportion to the V_{TH} shift. The off-state current, determined primarily by gate leakage, decreased further for the thicker oxides to <<1nA, ~10^3 reduction from that for the HFET. The off-state current for the thinnest 10nm oxide increased slightly, although it remained in the nA range. We ascribe this unusual outlier to a dramatic change in the



(a)



(b)

Figure 3.18 Transfer (I_{DS}-V_{GS}) characteristics of HFET and high-*k* ZrO_2 MOSHFETs before (a) and after (b) 300 °C annealing.

ZrO_2/AlGaN interface, $n_{ox,intf}$, which we will discuss further when quantifying the various charges responsible for the V_{TH} shifts. As expected, the 2-terminal gate-source leakage characteristics showed a behavior similar to that of the off-state leakage current as shown in Figure 3.19.

The sub-threshold swing (SS) for MOSHFETs (all t_{ox}) improved significantly after annealing to a value as low as 105mV/decade for the device with 20nm thick ZrO_2. The improvement in SS is primarily due to the reduction in gate leakage described above, with high gate leakage masking the channel current at the lowest levels. We believe, the ALD oxide annealing lowers the interface trap density leading to reduced hysteresis and improved SS values [79].

3.3.1.b Threshold control mechanism:

To separate the influence of $n_{ox,bulk}$ and $n_{ox,intf}$,V_{TH} of un-annealed and annealed MOSHFETs are plotted as a function of t_{ox} in Figure 3.20 (a). In equation (1) V_{TH} is described by a quadratic polynomial of t_{ox} where the linear term gives $n_{ox,intf}$ while the quadratic term gives $n_{ox,bulk}$. A second order polynomial fit to the experimental V_{TH} vs t_{ox} gave excellent agreement with the equation. The $n_{ox,bulk}$=+2.5×10^{19} cm^{-3} in un-annealed MOSHFETs decreases only slightly to +1.7×10^{19} cm^{-3} after annealing. In contrast, annealing flipped the polarity of the large $n_{ox,intf}$ =+5.5×10^{13} cm^{-2} to $n_{ox,intf} = -4.2\times10^{13}$ cm^{-2}, a very large change of ~ (-10^{14} cm^{-2}). Figure 3.20 (b) shows the band diagram with the locations of these charges in the structure. This large negative $n_{ox,intf}$ induced by post-deposition annealing at 300°C is responsible for partially depleting the channel 2DEG, reducing n_s, and making V_{TH} less negative. This reduced $n_{s,}$ we believe is also responsible for the ~20% decrease in the peak drain current that

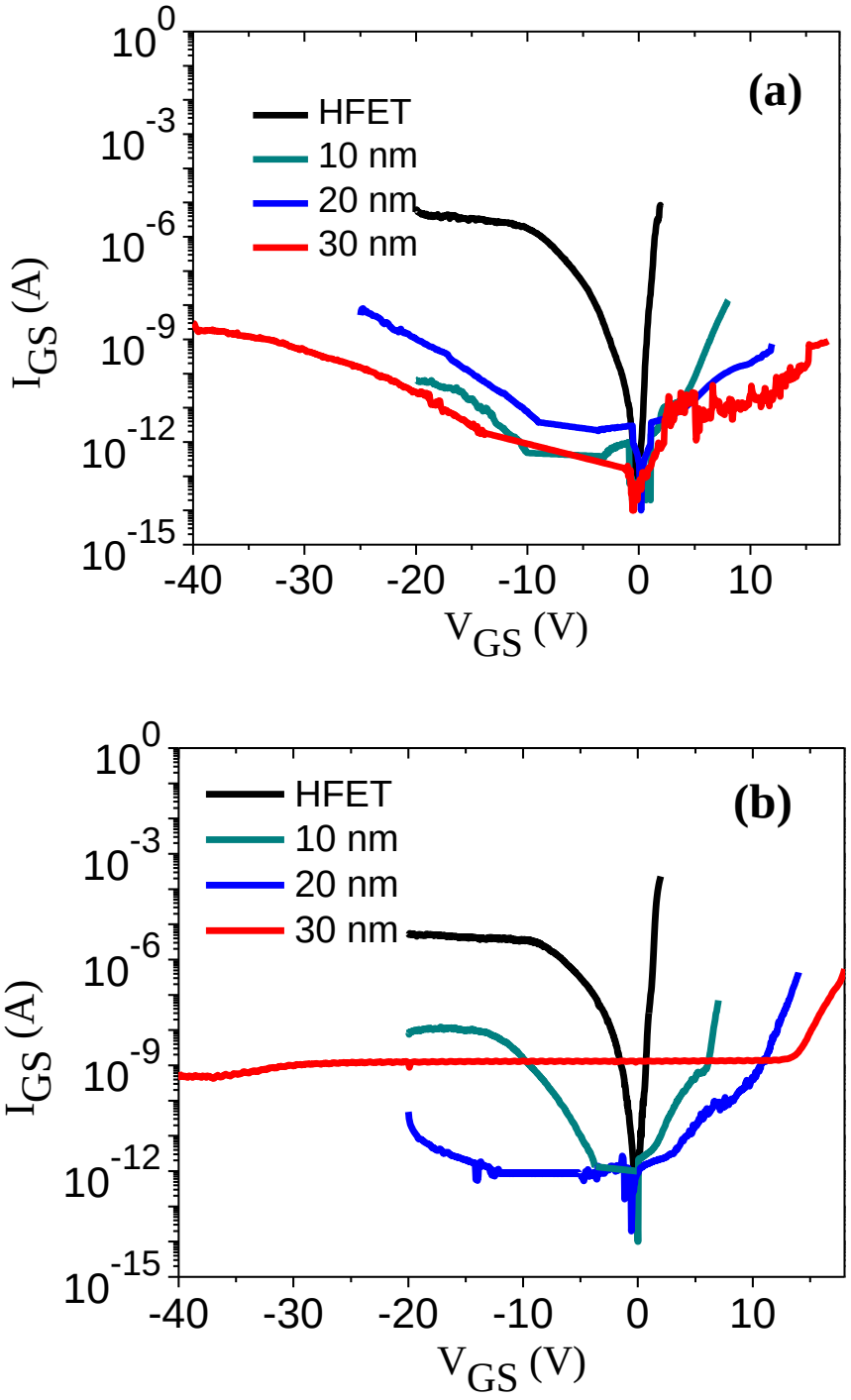


Figure 3.19 Gate leakage characteristics of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs before (a) and after (b) annealing.

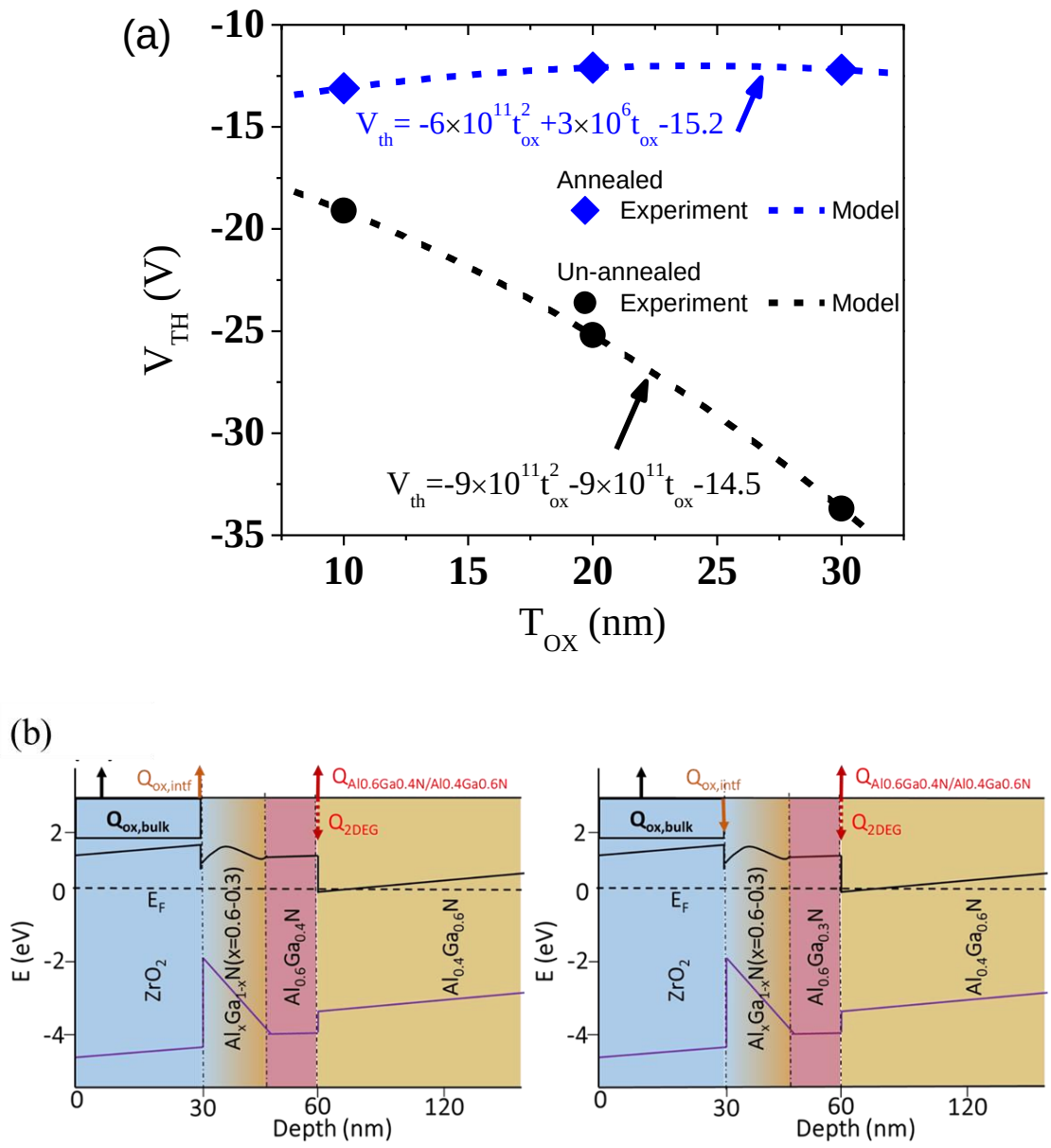


Figure 3.20 (a) V_{TH} of un-annealed and annealed MOSHFETs with ZrO_2 thickness of 10, 20 and 30 nm. The dots show experimental value and dashed lines show fitting to analytical model. (b) Band diagram of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ MOSHFET showing the location and polarity of bulk and interface charges before (left) and after (right) annealing.

was observed after the 300 ^{0}C annealing. However, this is much lower than the 2-3x decrease in n_s, indicating that because of the annealing, the channel mobility may have increased ~2x.

3.3.2 Characterization of MOSHFETs with different high-*k* dielectrics:

Due to their superior breakdown fields compared to GaN and SiC and high thermal conductivity, $Al_xGa_{1-x}N$ (x>0.4) channel Transistors (HEMTs) will find applications in extreme environments such as power electronics. In this part of the chapter, we characterize the MOSHFET devices at room temperature as well as high temperature to compare their performance at extreme environments, hence decide their usage in next generation devices.

3.3.2.a MOSHFET characteristics:

3.3.2.a(i) DC output characteristics:

Figure 3.21 **(a)** shows the drain I-V characteristics of the fabricated AlGaN channel ZrO_2 MOSHFET, with a 1.8 μm long gate (L_G), in a 6 μm source-drain spacing. Clear saturation and pinch off are observed. Figure 3.21 (b) and (c) show the peak currents of same geometry ALD MOSHFETs with different dielectrics compared to that of the HFET at room temperature and 250°C respectively. The I-V characteristics of Al_2O_3, ZrO_2 and TiO_2 MOSHFETs are similar with peak currents ~0.44 A mm^{-1} at V_G= +2V, ~0.5 A mm^{-1} at V_G=+6V and ~0.54 A mm^{-1} at V_G=+6V correspondingly at room temperature. These currents are higher than the control HFET (i.e. no oxide under gate) peak currents of ~0.4 A mm^{-1}, at V_G=+2 V, which is maximum gate voltage that can be applied without triggering high gate leakage current. Higher peak currents in MOSHFETs are due to the higher positive voltage that can be applied to the gate. At 250°C the peak drain current of Al_2O_3, ZrO_2 and TiO_2 MOSHFETs are 0.3 A mm^{-1}, 0.31 A mm^{-1} and 0.35 A mm^{-1} respectively

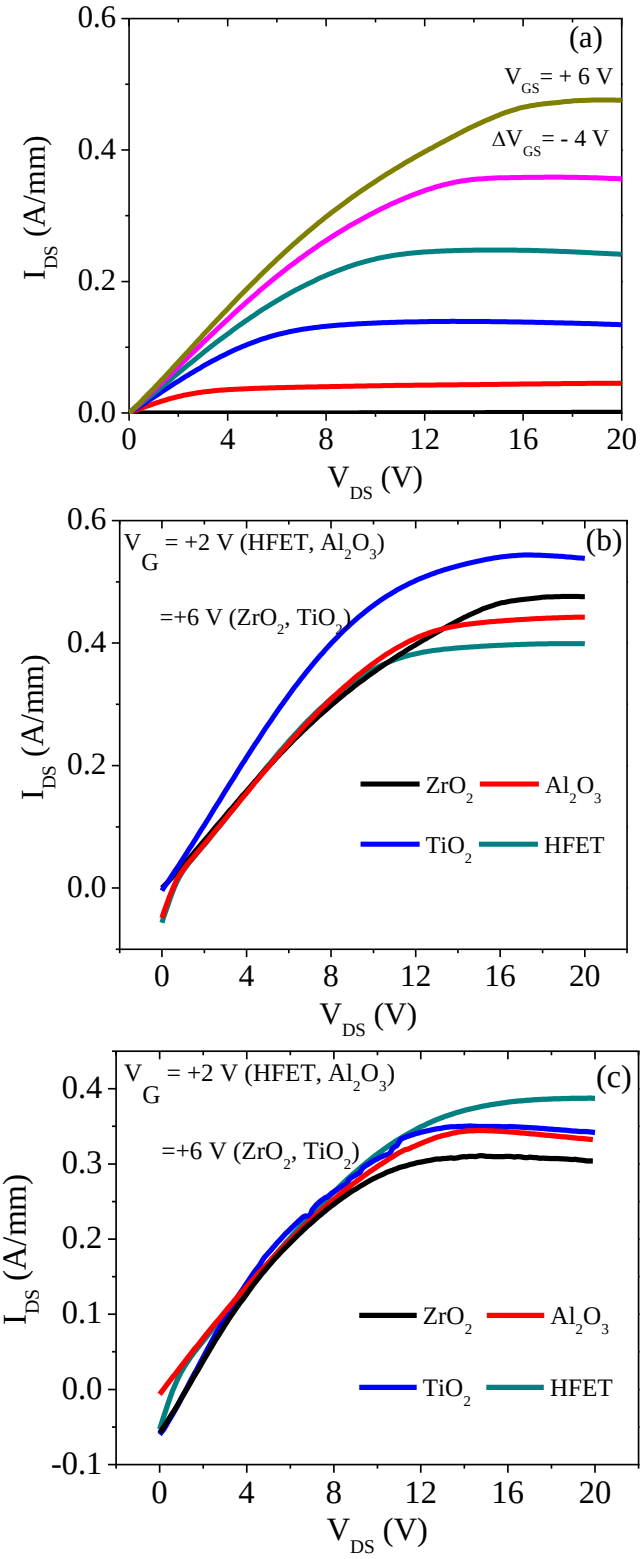


Figure 3.21 (a) Output characteristics of ZrO_2 MOSHFET. (b)The peak current comparison of different MOSHFETs and HFET at RT. (c)The peak current comparison of different MOSHFETs and HFET at 250°C.

where for HFET it is 0.38 A/mm under same gate voltage condition of room temperature. Thus, at 250 °C the peak current decrease by 35%, 38%, 32% and 5% from room temperature peak current for TiO_2, ZrO_2, Al_2O_3 and HFET respectively.

3.3.2.a(ii) Transfer and gate leakage characteristics:

The room temperature transfer characteristics of Figure 3.22 (a) were measured using 10 µm long gate MOSHFETs. This was done to ensure that in the subthreshold regime the gate leakage current is dominated by bulk rather than the surface leakage. This allows a direct comparison of the gate isolation by the different dielectrics. The transfer curves show that the ON/OFF ratio of ~10^3 for the HFET increases to ~6×10^6 for devices with ZrO_2 and Al_2O_3 gate-dielectrics. This improvement is primarily from the reduction in the gate leakage current (see Figure 3.22 (a) inset). The I_G-V_G curves in the inset of Figure 3.22 (a) show a reduction of the gate-leakage current by 5 orders of magnitude for Al_2O_3 and ZrO_2 and by ~2 orders of magnitude for TiO_2 gate devices. We attribute the poorer reduction of the gate leakage current in TiO_2 devices to a smaller bandgap of this material compared to the other two dielectrics used in our study (see Table 3.3). Using data of Figure 3.22 (a), the values of threshold voltage V_{th} were obtained as V_G voltages at which the drain current decreases to 30 µA. Figure 3.22 (b) shows transfer characteristics of these devices at 250°C. From RT to 250°C the threshold voltage changes from -9.8 V to -10 V, -12.7 V to -12.8 V, -10 V to -10. 5 V and -13.5 V to -14 V for ZrO_2, Al_2O_3, TiO_2 and HFET respectively.

Figure 3.23 (a-c) shows the gate leakage characteristics of the MOSHFETs from RT up to 250 °C. The gate leakage is seen to be weakly dependent on temperature. Like the transfer characteristics discussed in the previous section, the transfer characteristics of

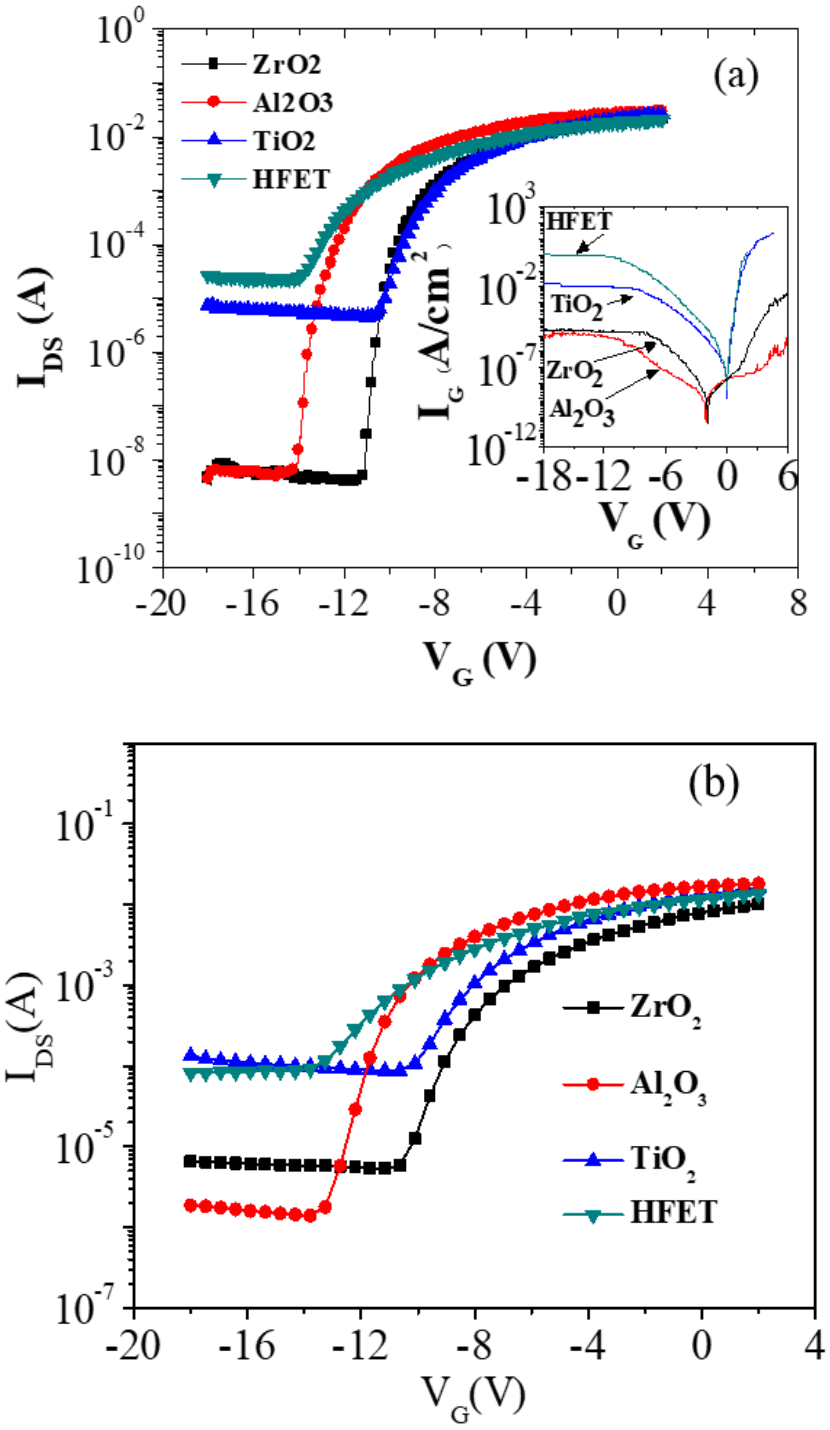


Figure 3.22 (a) The transfer characteristics of HFET and MOSHFETs at RT. Inset shows the gate leakage current of HFET and MOSHFETs. (b) The transfer characteristics of HFET and MOSHFETs at 250 °C.

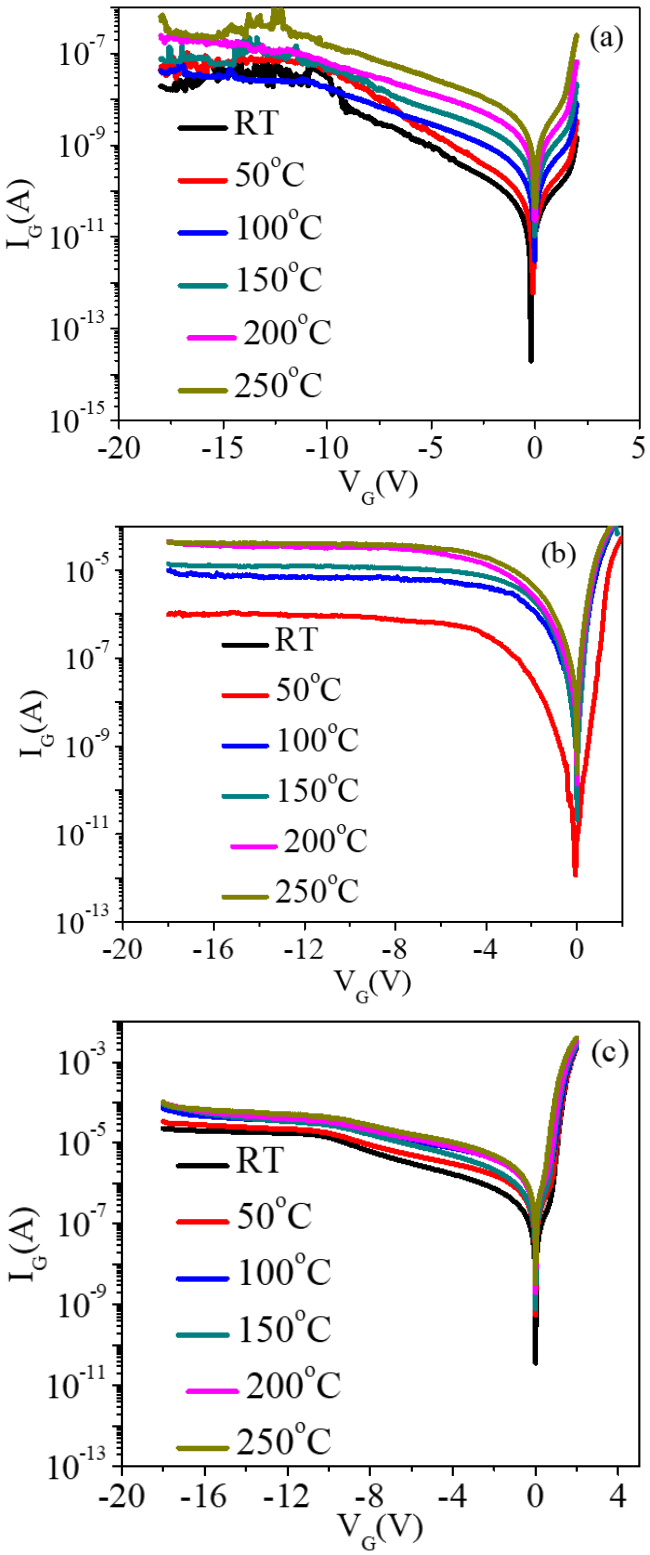


Figure 3.23 Temperature dependent gate leakage of (a) Al_2O_3 (b) ZrO_2 and (c) TiO_2 MOSHFETs.

Table 3.3 Summary of key transistor parameters. Here *k* is the dielectric constant, E_G is the bandgap of the gate dielectric, q is the elementary charge.

	k/E_G(eV)	V_{th} (I-V)	V_{bi} (C-V)	On/Off	SS (mV/dec)	$N_{d,b}$ (cm^{-3})	Q_{2D} (C-cm^{-2})	Q_{ox} (C-cm^{-2})
HFET	None	-13.7	3.0	10^3	1290	6.8×10^{18}	1.9×10^{13}q	None
Al_2O_3	8/6eV	-12.9	5.5	6×10^6	105	5.0×10^{18}	1.9×10^{13}q	$+0.8\times10^{12}$ q
ZrO_2	25/6eV	-10.3	2.6	6×10^6	190	4.2×10^{18}	1.5×10^{13}q	-3.1×10^{13}q
TiO_2	80/3.2eV	-10.0	2.0	2×10^4	740	4.4×10^{18}	1.4×10^{13}q	-1.4×10^{13}q

Figure 3.22 (a) show a positive shift in V_{th} for all the ALD MOSHFETs as compared to that of HFET.

The threshold voltage, V_{th} showed *positive shift* by ~4V for the ZrO_2 and TiO_2 dielectrics and by ~1V for the Al_2O_3 gate-devices. Positive threshold voltage shift is an important effect that may help creating normally-off (enhancement mode) MOSHFETs which are very important for use in power electronics applications. In the previous section we already identified the mechanism of this threshold shift which is mainly because of the fixed negative charges (Q_{ox}). Oxide (Q_{ox}) and interfacial charges (D_{it}) also play an important role in switching and high-frequency performance of wide bandgap MOSHFETs [80]. To determine these charges detailed frequency dependent C-V analysis was conducted that will be discussed in the next section.

3.3.2.a(iii) Q_{ox} and D_{it} Estimation:

For the study, large area FETs with gate-length L_G=100 μm, and gate-width W=200 μm were used to test the C-V characteristics. Frequency dependent C-V characteristics for the MOSHFETs are shown in Figure 3.24 (a-c). The carrier depletion at V_G=0 V, only extends partially into the barrier layer, and does not reach the 2DEG, which is true for all the MOSHFETs. This phenomena simplifies the analysis. Because of the high doping in the barrier layer, it is possible to clearly distinguish three regimes seen in all devices:

i) Depletion through barrier layer -2 V<V_G<0 V with $1/C^2$ dependence showing constant doping

ii) 2D electron gas at barrier/channel interface ≈-8 V<V_G<-2 V

iii) pinch-off, with depletion extending into channel epitaxial layer V_G<<-8 V

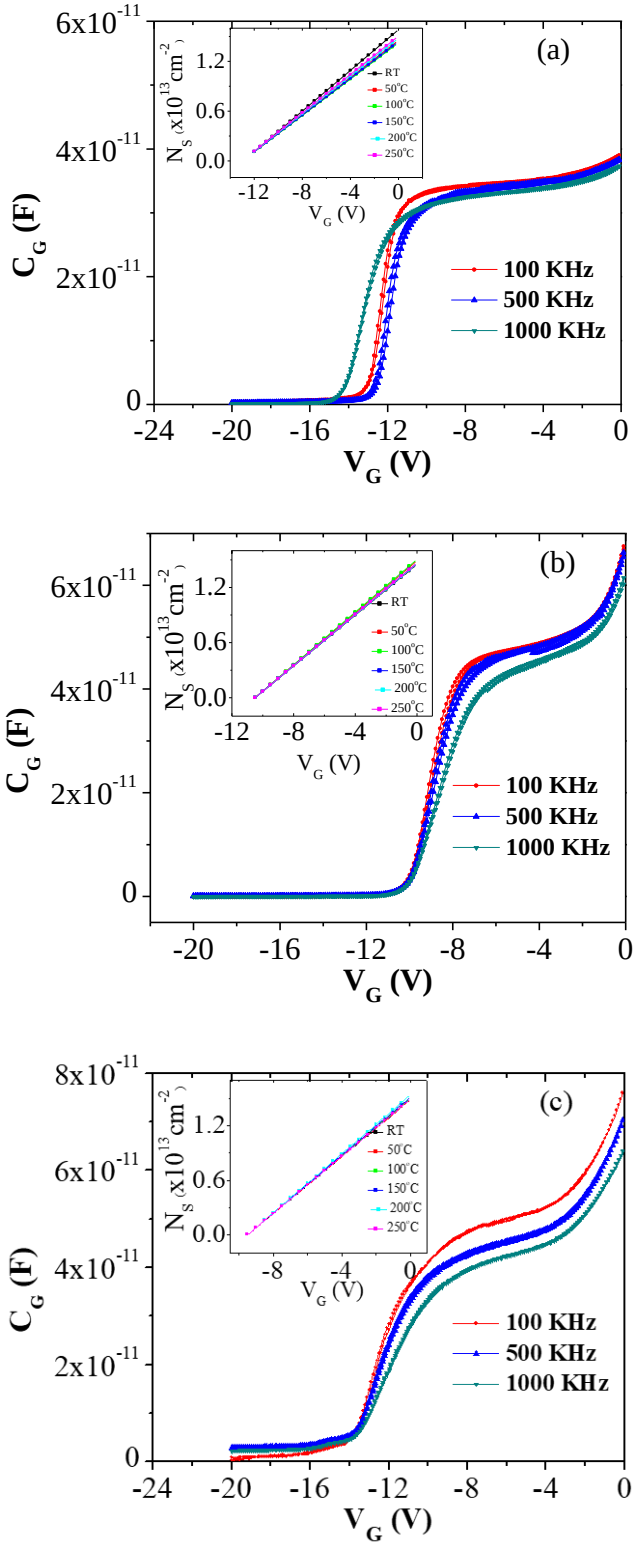


Figure 3.24 Frequency dependent C-V characteristics of (a) Al_2O_3 (b) ZrO_2 and (c) TiO_2 MOSHFET. Inset figures show the temperature dependent carrier concentration of corresponding MOSHFETs.

For all the devices, the boundary between regimes (i) and (ii) represents the voltage at which the 2DEG is being depleted, from which the capacitance of the gate at the 2DEG is measured, C_{2D}, which is true regardless of whether an oxide is present.

The donor concentration in the barrier layer, N_d is extracted from the linear $1/C^2$ characteristics in regime (i). For all the ALD oxide devices, this was ~4-5×10^{18} cm^{-3}, whereas for the HFET, this was significantly higher at 6.8×10^{18} cm^{-3}. This change from HFET to MOSHFET N_d value is due to the *in situ* pre-ALD surface preparation. From the boundary between regimes (i) and (ii) for the HFET, where the 2DEG is located at the barrier/channel interface, The barrier thickness is extracted using the formula, $t_b = \varepsilon_s/C_{2D,}$ where C_{2D} is the capacitance of the boundary between regime (i) and (ii) for the HFET. The extracted barrier thickness is 30 nm. We use this value of t_b for all the other MOSHFET's, which is justified given that all these transistors were fabricated on quarters from the same wafer.

The built-in voltage V_{bi}, measured from the $1/C^2$ x-intercept in Figure can be expressed in terms of x_d as follows [81]:

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + E_{ox} t_{ox} \qquad (3.4)$$

For the HFET, t_{ox}=0, so that from the measured N_d and V_{bi}, x_d is extracted to be 20 nm, in agreement with that extracted from the gate capacitance at V_G=0 V i.e. C (0), which is $x_d = \varepsilon_s/C(0)$=24 nm, showing that our formalism here is self-consistent. The Q_{ox} extracted is shown in Table 3.3. The extraction procedure is outlined in our recent report [46] . Here, the negative Q_{ox} is responsible for depleting the 2DEG, and making V_{th} more positive. Al_2O_3, being native to the AlGaN system shows very low Q_{ox}. The small positive shift from

the HFET to the Al_2O_3 MOSHFET is apparently due to the lower N_d in the barrier as discussed above.

From the difference in the high and low frequency C-V characteristics, the density of interface states, D_{it} is obtained in cm^{-2}. It is a reasonable assumption that since the barrier here is doped, and relatively thick ~30 nm, the surface oxide charges, Q_{ox} do not significantly impact trapping at the barrier/channel interface. At low frequencies, slow traps respond capacitively, whereas at high frequency, they do not, leading to a decrease in measured capacitance at higher frequencies. Figure 3.24 (a-c) shows this dispersion for the MOSHFETs. The total integrated trap density is ~2-3×10^{12} cm^{-2}. We also note that there is mild hysteresis near V_{th}, although the charge in the area bounded by this hysteresis is ~0.5×10^{12} cm^{-2}, small compared to that by the hi-lo method.

Considering the high ON/OFF ratio of these devices, we were also interested to calculate the subthreshold swing (SS) which characterizes how steep is the device transition from the ON to the OFF state as a function of gate voltage. Because the SS depends intrinsically on the barrier/channel interfacial trap density, and extrinsically on gate leakage, below we provide our comparison of the SS values in HFETs and ALD MOSHFETs. The results are summarized in Table 3.3. The intrinsic SS is given by [82]:

$$SS = \frac{60mV}{decade}\left[1 + \frac{qD_{it}(cm^{-2})}{C_G(V_{th})}\right] \qquad (3.5)$$

where D_{it} (cm^{-2}) is the total interface charge density implying ~2-3×10^{12} cm^{-2} which is obtained by integrating the area under the low frequency and high frequency C_G dispersion curve. We note that the HFET and higher leakage dielectric TiO_2 both display poor SS, which is artificially masked by the large gate leakage (Figure 3.22 (a) inset) below V_{th} (see Table 3.3) which also limits the ON/OFF ratio. By reducing the gate leakage with

ZrO_2 and Al_2O_3, the intrinsic SS of the barrier/channel interface was recovered as given by equation (3.5), which are comparable to the SS values of previously reported AlGaN channel HEMTs [83].

3.3.2.a(iv) MOSHFETs' Dynamic Characteristics (Current Collapse):

One of the most critical unavoidable issues in III-nitride based HEMT technology is degradation of drain under high frequency application which is typically known as current slump or current collapse. The leakage current from the gate and carrier trapping in the surface states in general, into the surface and buffer traps is the physical cause behind the current collapse class of the phenomena. In addition to the intrinsic trap states, the presence of Q_{ox} and D_{it} in our MOSHFET devices makes the current collapse study very important. Si_3N_4 is widely used to passivate the surface and reduce current collapse. In this study, we for the first time present current collapse study in UWBG AlGaN-channel MOSHFETs and efficient suppression of current collapse using Si_3N_4 passivation layer. 300 nm thick passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD) system.

The static and pulsed output I-V characteristics (I_{DS} vs V_{DS}) were measured using the DIVA D265 dynamic IV analyzer. Positive gate and negative drain pulses with the quiescent points $V_{GS,Q}$ = -15 V (below the threshold voltage) and $V_{DS,Q}$ = 20 V correspondingly. Pulse widths for our study varied from 500 ns to 1 ms with duty cycle of 0.1%. Figure 3.25 shows the Si_3N_4 passivate MOSHFET device and the time diagram of the gate and drain pulse.

Figure 3.26 (a-d) shows the static and pulsed I-Vs of un-passivated $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs, with a 1.8μm long gate (L_G), in a 6 μm

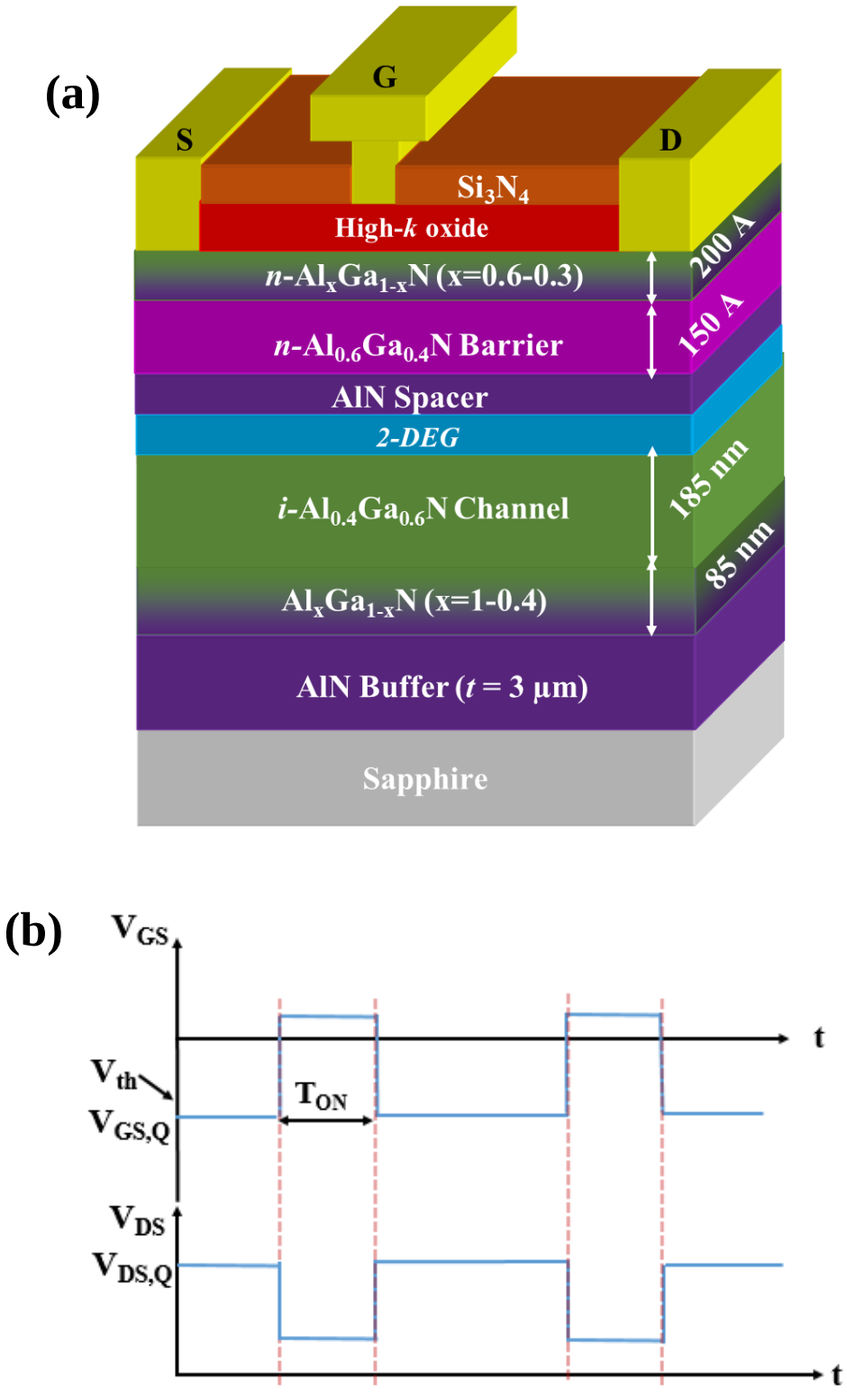


Figure 3.25 (a) High-*k* ALD MOSHFET with Si_3N_4 surface passivation. (b) Time diagram of Gate and Drain pulses.

source-drain spacing. Under gate and drain pulsing with above mentioned quiescent bias points, both HFET and MOSHFETs show significant reduction in the drain current (current collapse). These observations are similar to those on unpassivated AlGaN/GaN transistors[84][85][86][87][88]. All fabricated MOSHFETs showed higher degree of current collapse than the HFET. This implies that although high-*k* ALD oxides can be used as excellent gate dielectric, they are not suitable for current collapse removal However, the degree of current collapse is different. Al_2O_3-MOSHFETs show the minimal current collapse, whereas ZrO_2 and TiO_2 MOSHFETs exhibit stronger collapse. Figure 3.27 includes the same data for HFET and MOSHFET devices where Si_3N_4 passivation layer was deposited on top of the ALD oxides. These data show that the Si_3N_4 passivation layer removes the current collapse in our high- Al AlGaN channel MOSHFETs. This observation is similar to high-Al AlGaN channel HFETs[89]. However, the degree of removal of current collapse is different in different high-*k* MOSHFETs. We find a correlation here between the degree of current collapse and the value of dielectric constant (*k*). The degree of current collapse increases as the *k* value increases. On the other hand, the degree of current collapse removal increases when the dielectric allows for some discharge currents, i.e. is more conducting.

Figure 3.28 shows that, as pulse width increases from 100 ns to 1000 µs, the degree of collapse reduces due to sufficient time the device spends in the on- state for electron de-trapping. As seen from Figure 3.28, the characteristic time for electron emission from traps range from approximately 1 µs to 1 ms. At a pulse width of 1 ms, the degree of collapse is significantly lower and the dynamic drain current returns to ~90% of the static current value.

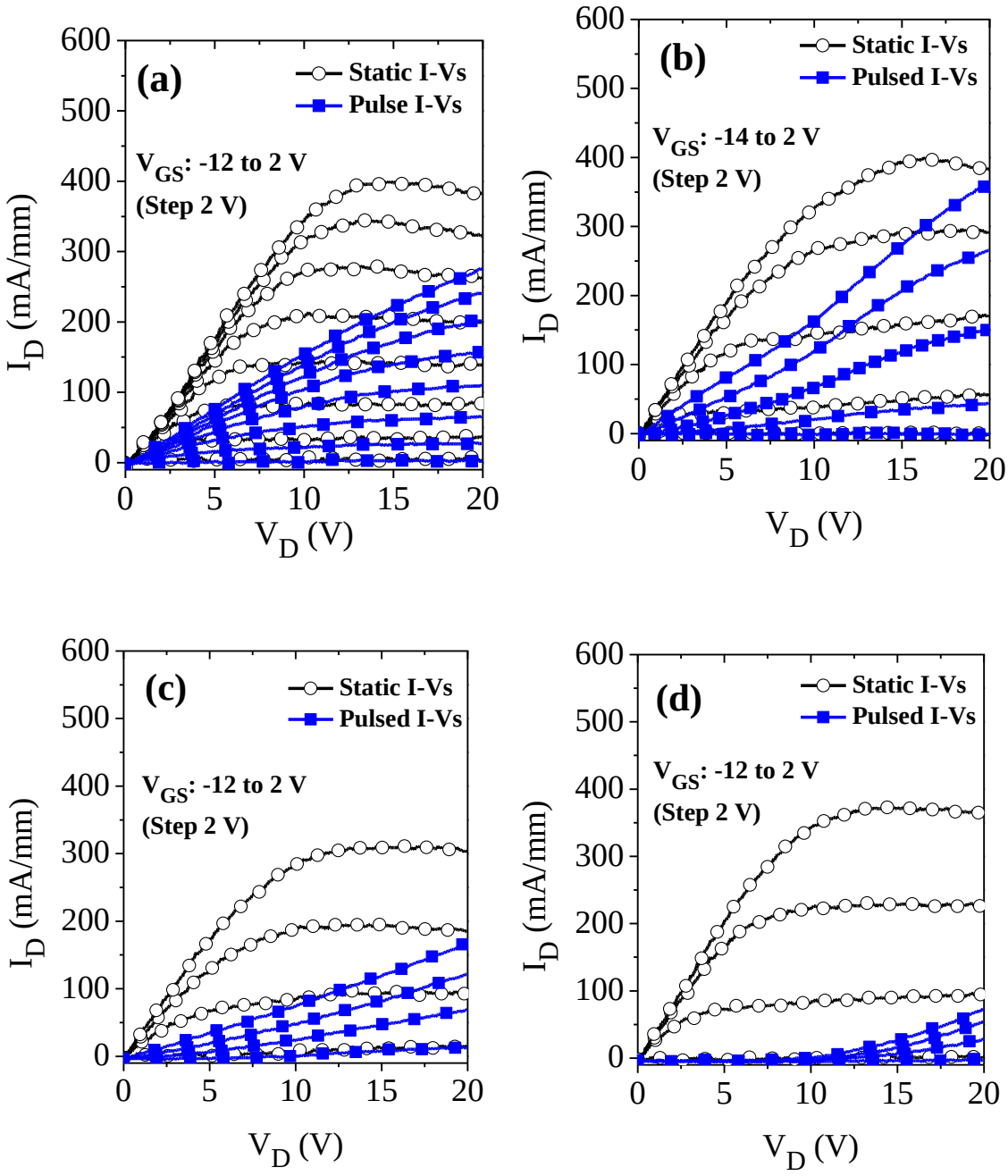


Figure 3.26 Static and Pulse I-V characteristics measured on un-passivated (a) HFET, (b) Al_2O_3, (c) ZrO_2 (d) TiO_2 MOSHFETs. Pulse duration T_{ON}= 500 ns, pulse period T= 500 µs, Quiescent bias point V_{GSQ}, V_{DSQ}= (-12 V, 20 V)

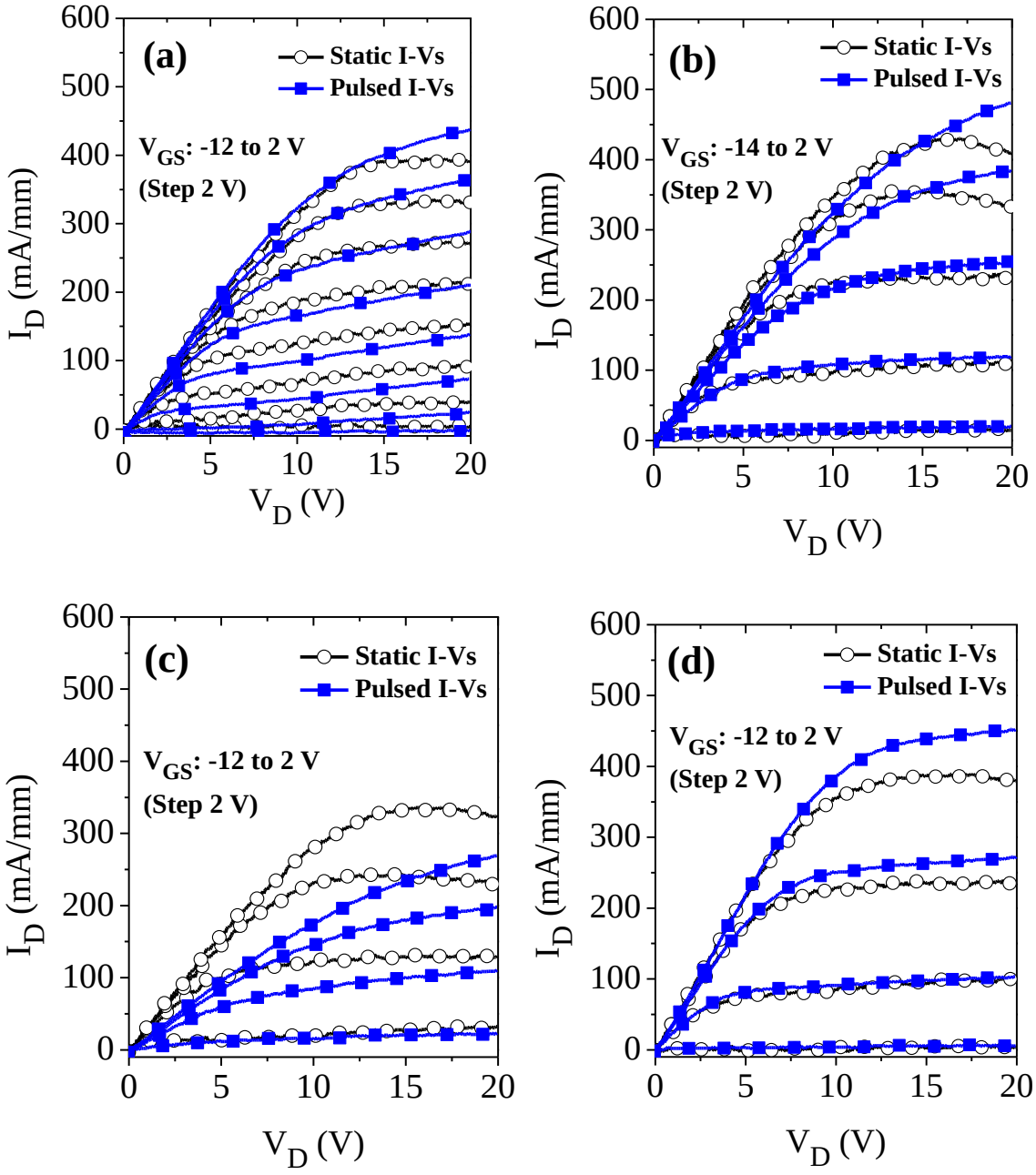


Figure 3.27 Static and Pulse I-V characteristics measured on Si_3N_4 passivated (a) HFET, (b) Al_2O_3, (c) ZrO_2 (d) TiO_2 MOSHFETs. Pulse duration T_{ON}= 500 ns, pulse period T= 500 µs, Quiescent bias point V_{GSQ}, V_{DSQ}= (-12 V, 20 V)

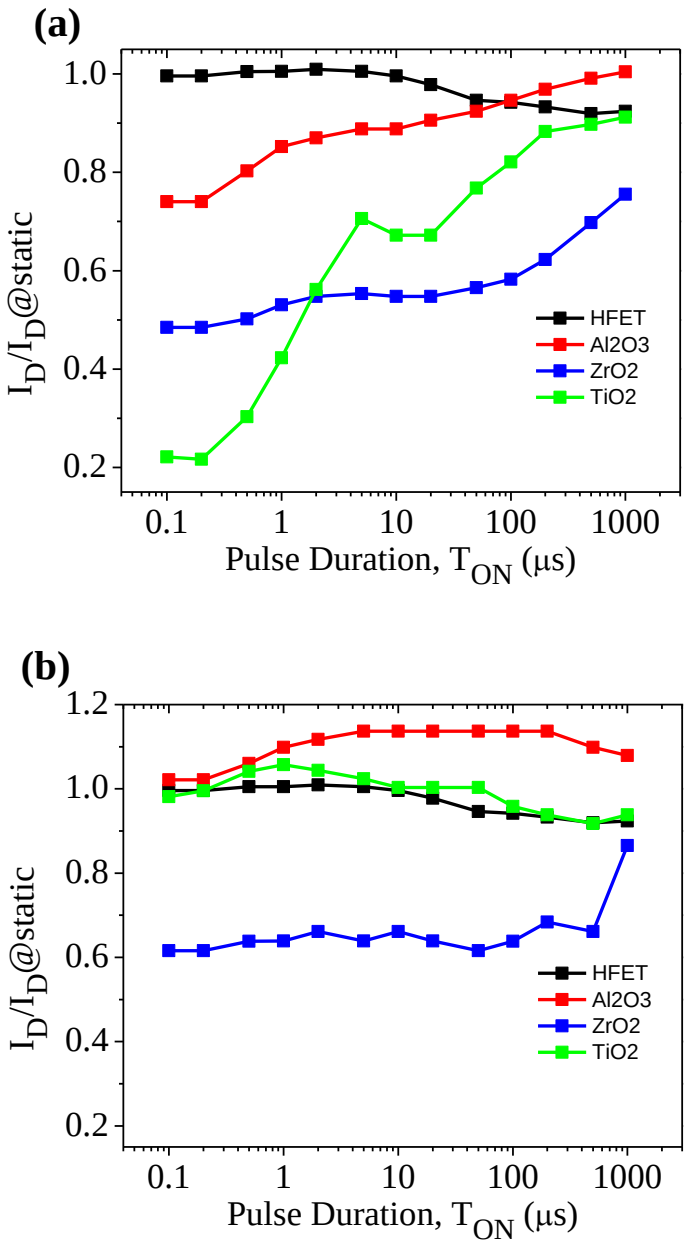


Figure 3.28 Pulsed drain current normalized to static drain current density for (a) un-passivated and (b) Si_3N_4 passivated MOSHFETs

3.3.2.a(v) Mobility:

The gate voltage and temperature dependent mobility of HFET and MOSHFETs was extracted using a technique that we have successfully employed in past for our AlGaN channel MOSHFETs [19] as well as GaN channel MOSHFETs [90]. The 2D channel electron mobility μ is extracted from the measured channel conductance [19]:

$$G_{ch} = qN_s\mu\frac{W}{L_G} \quad (3.6)$$

where W is the width of the channel and L_G is the gate length. The electron sheet concentration N_s can be found from the Capacitance- Voltage measurement using the following formula:

$$qN_S = (V_G - V_T)C_G \quad (3.7)$$

where q is the charge of electron, V_T is threshold voltage, V_G is the range of voltage above threshold and C_G is the measured gate capacitance per unit area. Figure 3.24 **(a-c)** insets illustrates that the N_S value for ZrO_2 MOSHFET at zero gate voltage is ~1.5×10^{13} cm^{-2} which is independent of temperature. In equation (3) the G_{ch}, Ns, μ are functions of gate voltage V_G. The channel conductance G_{ch} in turn, can be calculated from the measured drain- source resistance $R_{DS,}$ the contact resistances of drain and source ($2R_C$) and access region resistances from gate- drain (R_{GD}) and gate- source (R_{GS}):

$$G_{ch}(V_G) = 1/[R_{DS}(V_G) - 2R_c - R_{GD} - R_{GS}] \quad (3.8)$$

The contact resistance (R_C) and sheet resistances (R_{SH}) were extracted from the TLM measurements. R_{GS} and R_{GD} were found from the extracted R_{SH} value and calculated with corresponding contact spacing L_{GS} and L_{GD}.

Figure 3.29 shows MOSHFET channel electron mobility plot as a function of gate voltage and temperature while the inset figures show the power law fitting of temperature dependent mobility. At room temperature the mobility for ZrO_2, Al_2O_3 and TiO_2 MOSHFETs varies from ~200 $cm^2 V^{-1}s^{-1}$ to ~550 $cm^2 V^{-1}s^{-1}$, ~300 $cm^2 V^{-1}s^{-1}$ to ~650 $cm^2 V^{-1}s^{-1}$ and ~240 $cm^2 V^{-1}s^{-1}$ to ~480 $cm^2 V^{-1}s^{-1}$ at zero gate voltage and depleted channel conditions respectively while for HFET it varies from ~ 250 $cm^2 V^{-1}s^{-1}$ to ~ 1200 $cm^2 V^{-1}s^{-1}$. The extracted mobility and sheet carrier density are comparable to the earlier reported mobility and sheet carrier density of AlGaN channel HEMTs from our research group as well as reports of other groups. Baca et.al, reported their 70-85% HEMT with RT mobility value of 390 $cm^2 V^{-1}s^{-1}$ and sheet carrier density of 7.2×10^{12} cm^{-2} [91]**.** Klein et. al, in their AlGaN channel HEMT reported value of mobility 240 $cm^2 V^{-1}s^{-1}$ and sheet carrier density of 1.4×10^{13} cm^{-2} [32].

Table 3.4 shows that, at V_G= 0 V, ZrO_2 MOSHFET mobility is least affected by temperature change. The ZrO_2 MOSHFET mobility drops by < 40% from RT mobility where all other oxides' mobility drops by up to ~60% of RT mobility. On the other hand, in depleted channel condition, the TiO_2 is least affected by temperature. The mobility is decreased by ~17% while in other MOSHFETs it reduces by up to ~85%. Thus, the mobility in MOSHFETs with higher density of oxide charges (Q_{ox}) is less affected by increase of temperature.

The carrier mobility, μ increased with more negative gate voltage i.e. as the carrier concentration decreases (see inset of Figure 3.24 (a-c)). This N_s dependence implies the presence of phonon scattering. The temperature dependence of the MOSHFET channel electron mobility follows a power law $\mu \sim T^{-\alpha}$, with α varying between 1 and 3, further

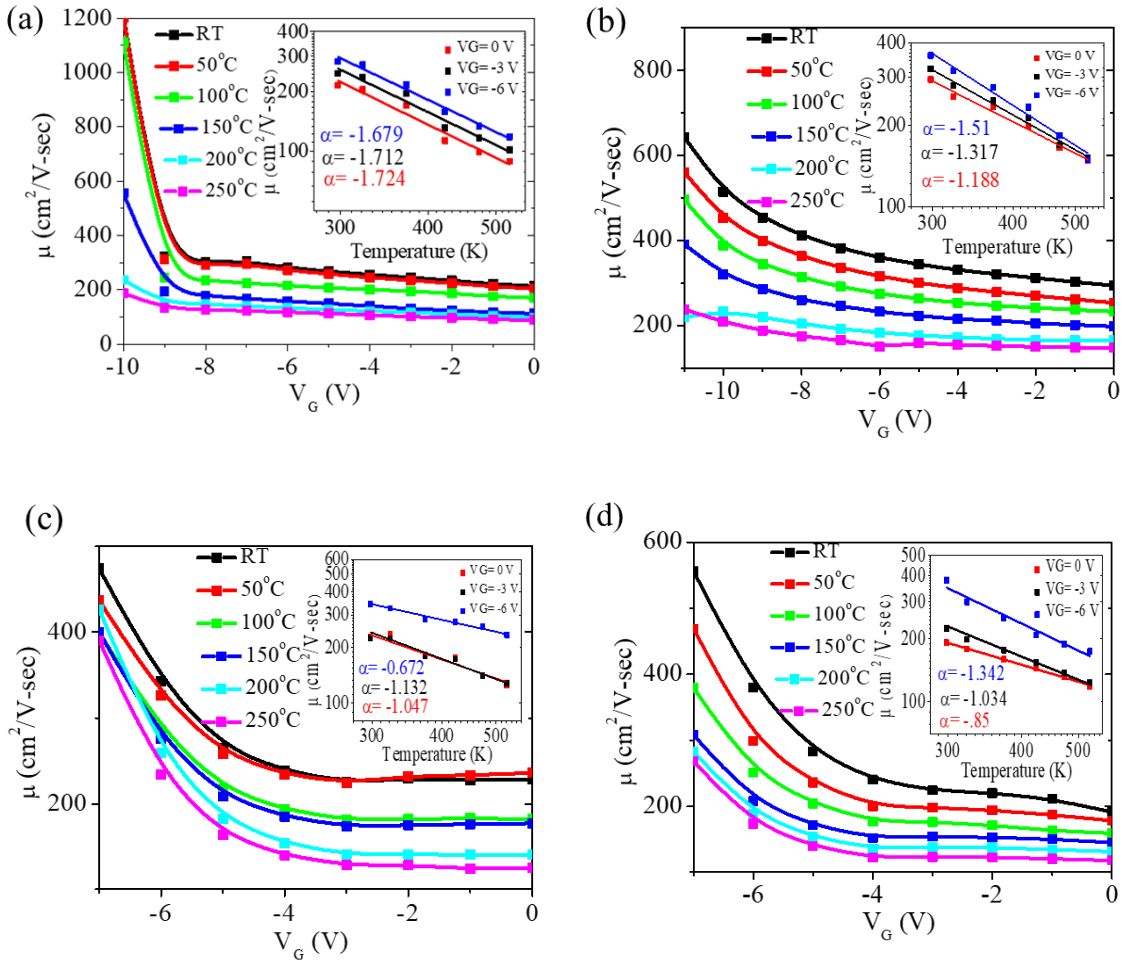


Figure 3.29 Temperature dependent mobility as a function of gate voltage for (a) HFET (b) Al_2O_3 (c)TiO_2 and (d) ZrO_2. Inset figures show power law fitting of mobility vs temperature plot to extract the power coefficient, α.

Table 3.4 Summary of electron mobility variation with temperature for different dielectrics

	RT mobility at V_G=0 V ($cm^2 V^{-1}s^{-1}$)	250°C mobility at V_G=0 V ($cm^2 V^{-1}s^{-1}$)	RT mobility at depleted channel ($cm^2 V^{-1}s^{-1}$)	250°C mobility at depleted channel ($cm^2 V^{-1}s^{-1}$)
HFET	207	87 (58% drop)	1188	188 (84% drop)
Al_2O_3	293	146 (50% drop)	641	240 (62% drop)
ZrO_2	191	118 (38% drop)	554	267 (51% drop)
TiO_2	233	125 (46% drop)	473	388 (17% drop)

supporting the phonon scattering as the dominant mobility limiting process [92]. We exclude the possibility of roughness scattering as the epilayer roughnesses were measured to be <1nm rms. While alloy scattering cannot be conclusively excluded, we note that it will be similar for all the gate dielectrics, given that the samples were cut from the same epitaxial wafer. We ascribe the small variations in μ, and in the temperature dependence, between the different dielectrics to ionized impurity/coulomb scattering, from charge introduced at the oxide/AlGaN barrier interface. The presence of this charge was demonstrated in Table 3.3 and is reflected in the threshold voltage shift.

3.4 Summary:

In summary, we demonstrate the mechanism of threshold voltage control in high-*k* ALD MOSHFETs, the high temperature gate oxide annealing eliminated negative threshold voltage shift caused by the dielectric layer and enabled operation at high forward gate bias, up to +18V compared to +2V for the Schottky gate HFET, as a result doubling the HFET maximum channel current. Our process also reduced the off-state leakage, improved the SS, while bringing V_{TH} into a range useful for practical applications. We show the improvement to be primarily due to a large change in fixed charge density at the ZrO_2/AlGaN interface induced by the annealing. The resulting $n_{ox,intf} = -4.2\times10^{13}$ cm^{-2} partially depleted the channel 2DEG to bring V_{TH} under control, while maintaining the current handling and the extremely low gate leakage currents. In second part of this chapter, we present a detailed study of high-*k* ALD MOSHFETs where we choose the gate oxide based on three different sets of dielectric constant and bandgap. MOSHFETs with higher bandgap oxide show superior leakage suppression while MOSHFETs with higher *k* show very good threshold control. The ZrO_2 shows maximum positive threshold shift and Al_2O_3

shows maximum gate leakage suppression. This leads us to design new dielectric layer combining these two materials that will be used for next generation device fabrication to maximize the device performance. Up to the measured temperature of 250 °C, the devices withstood repeated temperature cycles without catastrophic degradation or breakdown, underscoring the promise of these materials. The results discussed in this chapter shows the viability of ALD gate dielectrics for UWBG AlGaN channel MOSHFETs for high power applications.

CHAPTER 4: DEPLETION MODE HIGH CURRENT MOSHFET DEVICES

4.1 Background:

As discussed in the previous chapter, to take advantage of their high breakdown field, several research groups at present are developing ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ (x>0.4) channel heterostructure field effect transistors (HFETs) for high-temperature, high-voltage, and high-power applications [12][23]. Devices with channel alloy compositions of 40% or higher have been reported by several groups including ours [13][28][36][30][37]. To date, all these reported AlGaN channel devices have their drain currents well below 1 A/mm which is a typical value for GaN channel HFETs with micron size gate lengths [93][94][95][96][97]. The fundamental current limiting factors in UWBG AlGaN-channel devices are: i) difficulty of forming low resistivity ohmic contact ii) high sheet resistance that results in higher value of series resistance thus limiting the drain current. The AlGaN material suffer from alloy scattering which leads to low 2-dimensional electron gas (2DEG) mobility in UWBG AlGaN channel layers approximately a factor of 3-5 lower than that of GaN [30][98][99]. Thus, the sheet resistance values for UWBG AlGaN channel HFETs are typically 2000 Ω/□ as compared to around 300 Ω/□ for GaN channel devices [100][89]. iii) insulating gate plays a very important role where a positive gate-bias can be used for increasing the drain-currents.

To decrease the contact resistivity and increase the peak drain currents in UWBG AlGaN channel HFETs and MOSHFETs, several approaches have been explored. Xue et. al. used highly *n*-doped $Al_xGa_{1-x}N$ selectively grown contact layers on top of the UWBG AlGaN barrier layers [101]. However, the lowest achieved contact resistivity was still around 3.9 Ω-mm and, even with 0.16 μm long gates in a 1.2 μm access opening, the peak currents were limited to only 0.42 A/mm (at a gate voltage of +0V). As mentioned in the previous chapter, in our MOSHFET devices with 10 nm ALD oxides and *n*-doped barrier layers we achieved a contact resistivity as low as 1.6 Ω-mm and peak drain currents as high as 0.6 A/mm at a gate-voltage of +6V for 2 μm gate-length devices (access region 6 μm) [19]. More recently, we have also reported on a microchannel approach for reducing the effective contact resistance. For a 1:6 (fill factor), a 100 nm long gate in a 1.6 μm long access region, a peak drain-current of 900 mA/mm was measured at a gate voltage of +2V (Schottky gate) [102]. The processing sequence for fabricating these micro-channel devices was complicated with several steps needing precise e-beam lithography. Moreover, high gate leakage in these HFET devices limits usage of positive gate bias and it also reduces the breakdown voltage.

In this chapter, we address the second and third current limiting factors. To reduce the access resistance, we have used a perforated channel geometry which was shown to significantly reduce source and drain access resistances in GaN-channel devices [103]. Hybrid gate insulator (ZrO_2/Al_2O_3) is designed that allows to apply high positive gate bias. Incorporating these two novel approaches, we report Al_2O_3/ZrO_2-$Al_{0.6}Ga_{0.3}N$-$Al_{0.4}Ga_{0.6}N$ depletion mode (D-mode) MOSHFETs with peak drain current I_{Dmax} more than 1.3 A/mm which is state of the art for AlGaN-channel devices.

4.2 Experimental Details:

4.2.1 Epilayer structure:

The epilayer structure used in this study is similar to the structure we used for studies in previous chapter. Figure 4.1 (a) shows the sheet resistance of the as grown sample measured by Lehighton contactless sheet resistance mapping system. The on wafer C-V measurement by mercury probe C-V measurement system shows depletion voltage of the $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HEMT structure is ~10 V (Figure 4.1 (b)).

4.2.2 Device Fabrication:

The process flow for the $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ perforated channel (PC) MOSHFET devices used in this study is shown below in Figure 4.2. The fabrication process is similar to what described in the previous chapter except the steps: perforated channel etching, thick SiO_2 deposition and contact pad opening. The thick SiO_2 is deposited in order to avoid air breakdown while measuring the breakdown voltage. Figure 4.3 shows the schematic of the final processed device.

4.2.3 Perforated Channel:

In the PC design, the gate area consists of the alternating regions of conducting straits (W_S) separated by non-conducting islands (W_B) where the channel material is completely removed (only under the gate but not in the G-S and G-D regions) (see Figure 4.4 (a-c)). The current flowing out of the gate straits therefore spreads out into larger area G-S and G-D regions which leads to smaller gap and contact access resistances. Each elementary section of PC-MOSHFET can be viewed as a device with the channel width equal to that of conducting straight W_S but with the access and contact regions about twice

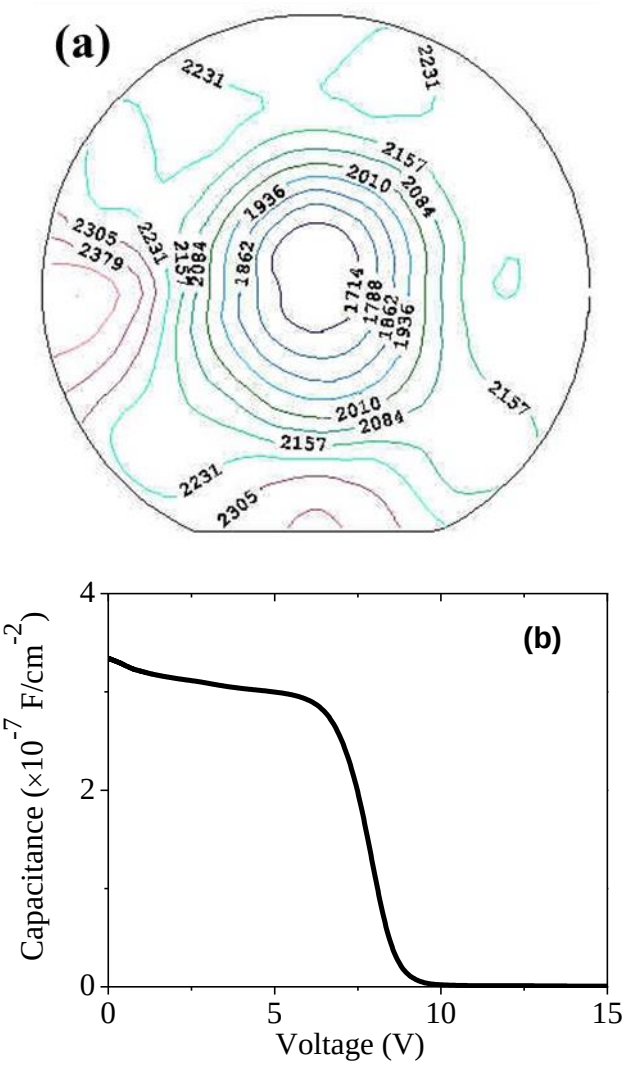


Figure 4.1 (a) Sheet resistance measured by Lehighton sheet resistance mapping system (b) C-V characteristics measured by mercury probe C-V measurement system.

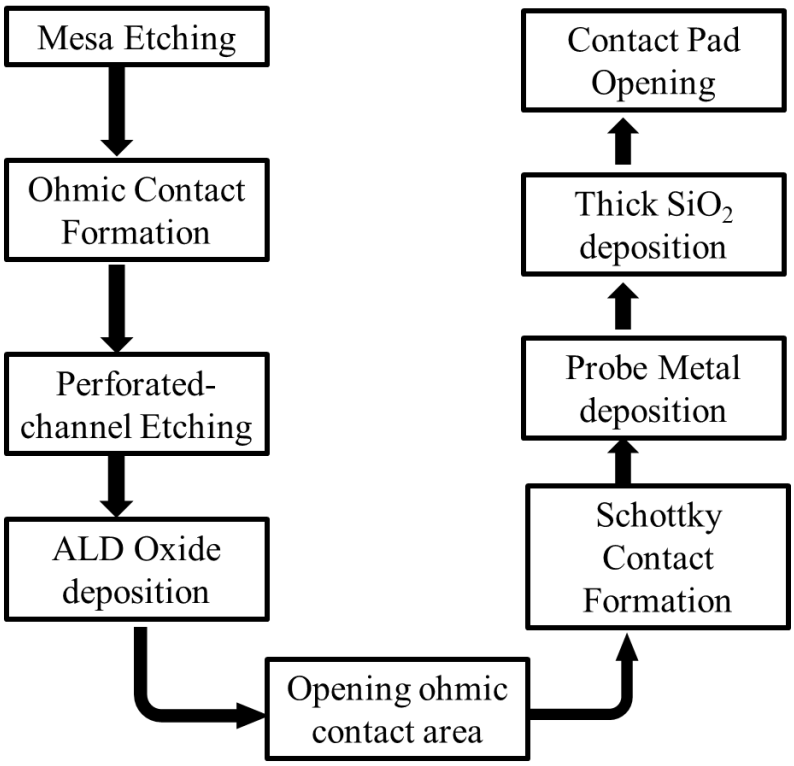


Figure 4.2 Process flow for the perforated-channel (PC) $Al_{0.4}Ga_{0.6}N$-channel MOSHFET fabrication

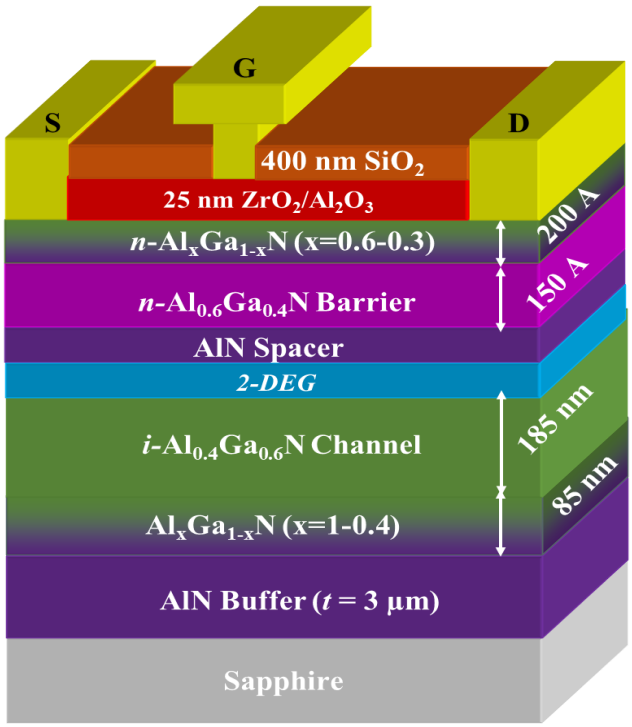


Figure 4.3 Schematic of epitaxial heterostructure and device geometry of perforated-channel $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ MOSHFET device.

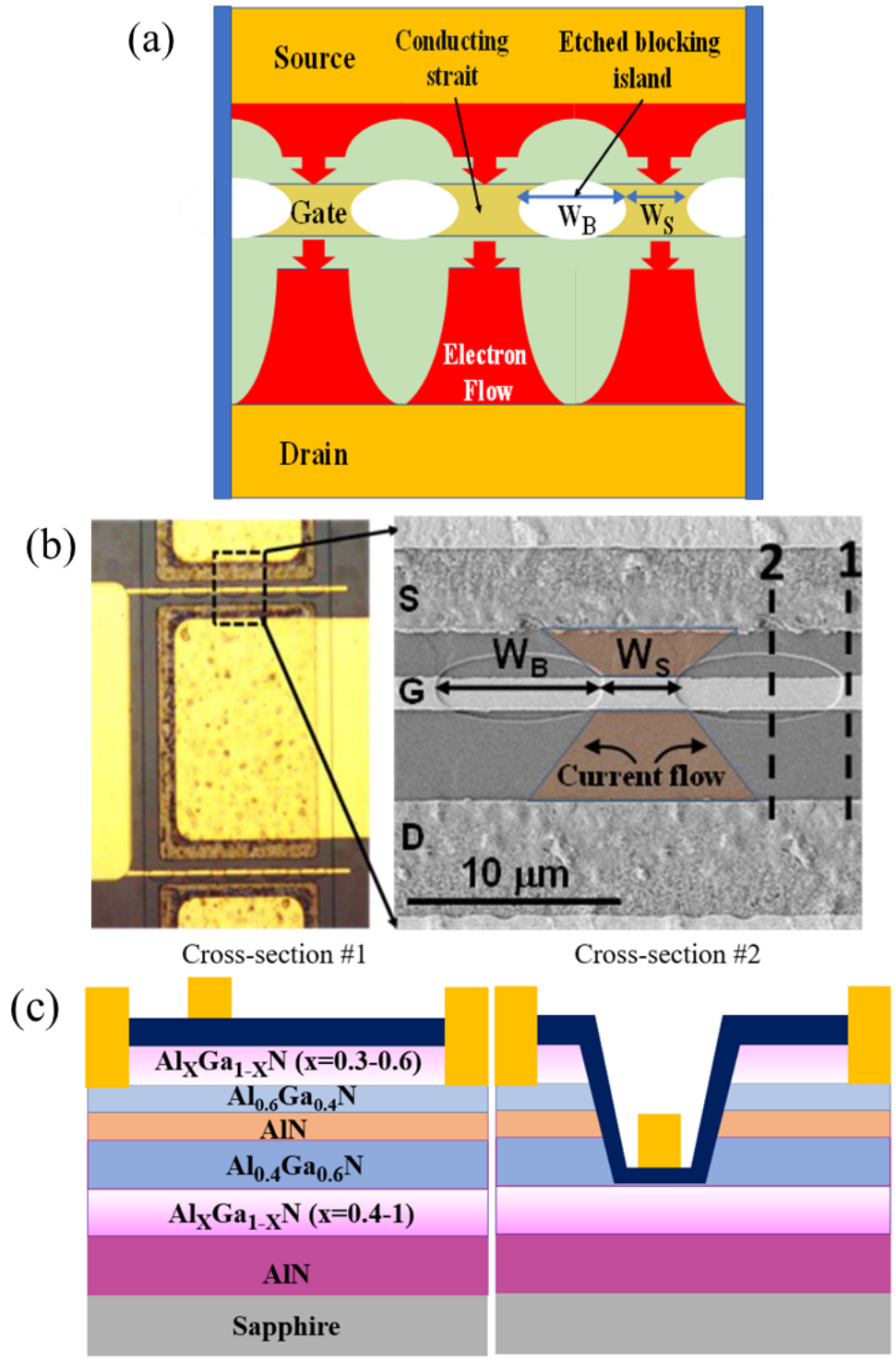


Figure 4.4 (a) layout of the perforated channel MOSHFET (b) The optical and SEM image of the perforated channel (PC) MOSHFETs showing the conducting straits and isolation between them where, W_B= width of the blocking gaps and W_S= width of the conducting straits. (c) cross- sectional view of PC-MOSHFET where 1 and 2 represent the un-perforated and perforated portion respectively.

as wide. Due to this, while intrinsic channel resistance and capacitance do not change, the total resistance per single elementary section is significantly reduced.

2D simulations show that 4 μm away from the gate edge the current density in between the channel straits is only two times lower than that along the strait center. As a result, the equivalent width of the S-G and G-D access regions, including the contact regions is larger than that of the gate strait hence leading to substantially lower access resistances. Importantly, the HFET capacitance coming mainly from the strait regions does not increase in PC design (see more on this below). The maximum reduction of the access resistances, by a factor of 2 – 3, occurs when the gap between the straits is around twice the width of the straits and the gate-drain distance is larger or comparable to the strait width [103]. In addition, in the PC layout, the reduction in average power density reduces the device temperature and also enables higher channel currents. Figure 4.5 shows I-V characteristics of a conventional and PC-MOSHFET on a test AlGaN-channel device where the PC-MOSHFET shows almost 2× drain current compared to conventional MOSHFET at same gate voltage.

For the fabrication of PC-MOSHFET devices in this study, we selected the width of the straits $W_S \approx 3.75$ μm and blocking gaps between them $W_B \approx 8.25$ μm (see Figure 4.4 (b)). These dimensions were confirmed using Scanning Electron micrographs. This geometry corresponds to an optimal island/gap ratio of 2-2.5 as was determined following the procedure outlined in reference [103]. As shown in the cross-sectional view in Figure 4.4 (c), the 250 nm deep current blocking islands were formed using a Cl_2 based RIE process with an etch rate of ~ 10 nm/sec after the formation of the source-drain ohmic contacts. Measurement on test structure shows that islands are completely insulating. The

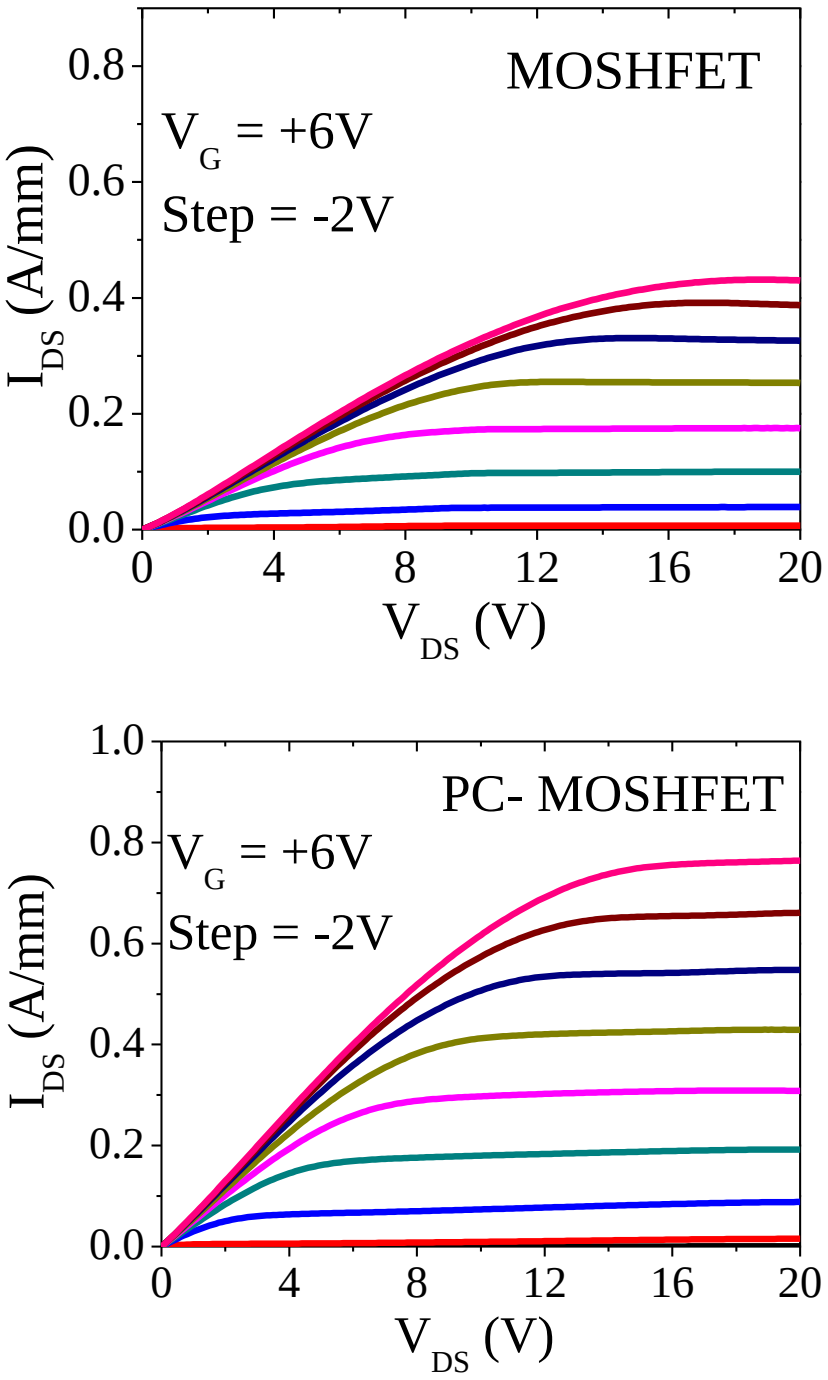


Figure 4.5 I-V characteristics of a (a) conventional and (b) PC-MOSHFET

threshold voltage of perforated channel device was found to be same as that of non-perforated control device.

4.2.4 Gate Design and Fabrication:

Threshold voltage and gate leakage are the two most important key parameters in any MOSHFET device. Threshold is a direct function of *k* value of the material while leakage is directly dependent on bandgap (E_G). For an ideal high-*k* dielectric it is desired to have both *k* and E_G values to be higher, in order to have low threshold shift and high gate leakgae suppresion. Figure 4.6 (a) shows a clear trade-off between *k* and E_G. Materials with higher *k* values lack high E_G and vice-versa. One potential solution to this issue is making hybrid oxide by combining two different materials to achieve higher effective *k* and E_G.

In chapter 3, we have studied the performance comparison of $Al_{0.4}Ga_{0.6}N$-channel MOSHFETs with high-*k* ZrO_2, Al_2O_3 and TiO_2. Al_2O_3 shows good gate leakage suppression in both forward and reverse direction compared to other two oxides. This is due to its highest bangap among these set of oxides (Figure 4.6 (b)). ZrO_2 and TiO_2 demonstrate the similar amount of positive threshold shift while TiO_2 shows very poor gate leakage characteristics due to its low bandgap (see Figure 4.6). Based on this result, in this chapter we design hybrid ZrO_2/Al_2O_3 gate oxide where the material with higher *k* value (ZrO_2) is in contact with the semiconductor material for better threshold control and material with higher bandgap is on top of the first oxide layer to provide better leakage performance.

From Figure 3.19 in the previous chapter we see that, the 20 nm ZrO_2 shows the maximum gate leakage suppression among the three different oxide thicknesses in both

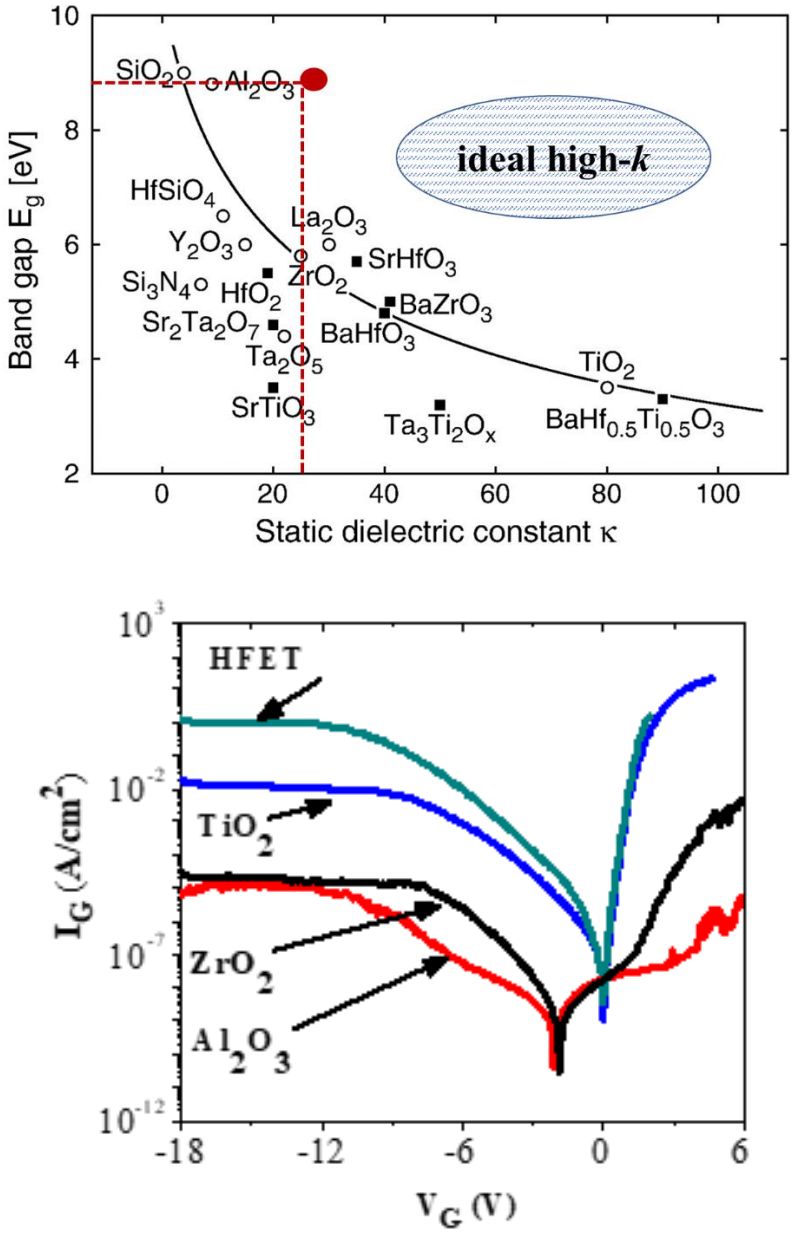


Figure 4.6 (a) Dielectric constant and bandgap plot of well-known oxide materials (b) Gate leakage characteristics of HFET and high-*k* ALD MOSHFETs.

voltage direction with large forward gate swing. Hence, for the fabrication of PC-MOSHFET devices in this study we choose 20 nm ZrO_2 coated with 5 nm Al_2O_3, resulting the total thickness 25 nm. After the perforated channel etching step, hot tetramethylammoniu hydroxide treatment was used to remove post plasma etch residue [104]. Atomic Layer Deposition (ALD) was then used to deposit Al_2O_3/ZrO_2 bilayer for the gate insulator followed by e-beam gate metallization consisting of 100 nm Ni/200 nm Au. The ALD deposition step is described in the previous chapter.

4.2.5 SiO_2 deposition:

Plasma Enhanced Chemical Vapor Deposition (PECVD) has been the widely used deposition technique for SiO_2 films where a chemical vapor deposition is used to deposit thin films from a gas state to solid state on a substrate. This method allows for thin film deposition at very low temperatures compared to the thermal deposition. In this process, the desired CVD reactions take place by dissociating the chemical vapor molecules to produce highly reactive free radicals. A schematic of PECVD chamber diagram is shown in Figure 4.7.

For the PECVD deposition of SiO_2, the common sources used are SiH_4 and N_2O. Under plasma glow discharge, N_2O source breaks up into *O radicals. The reaction sequence for the deposition process are demonstrated as [105]:

$$N_2O + *X \rightarrow NO + *N$$

$$NO + *X \rightarrow *N + *O$$

The excited oxygen atoms can then (a) react with SiH_4 to produce disiloxane ($(SiH_3)_2O$) and (b) participate in the surface reaction that is necessary for the formation of SiOx films. The reaction required for producing the $(SiH_3)_2O$ can be written as

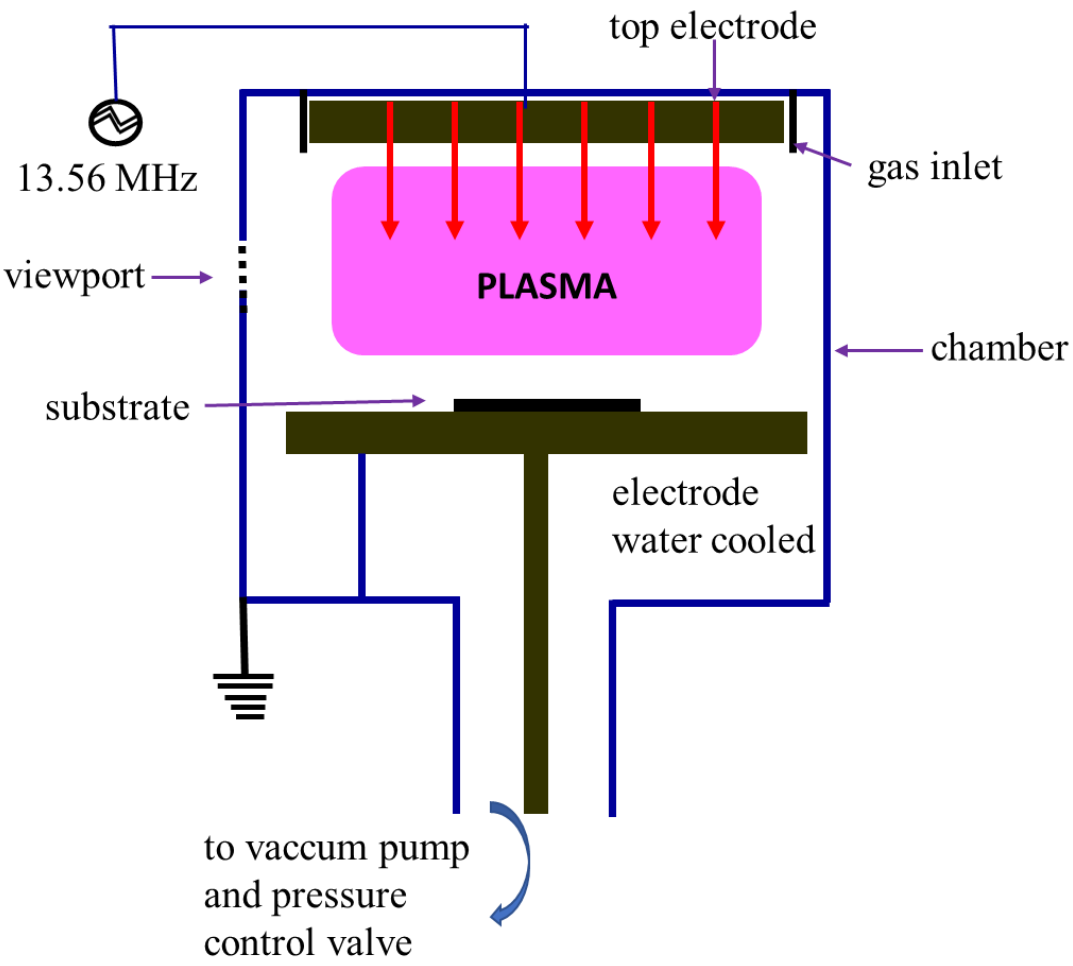


Figure 4.7 Schematic diagram of PECVD chamber

$$*X + N_2O \rightarrow N_2 + *O + X$$

$$*O + 2\ SiH_4 \rightarrow H_2 + (SiH_3)_2O$$

The surface reaction to form the SiO_x films can be expressed as

$$(SiH_3)_2O + *O \rightarrow 2\ SiO_2 + 2H_2 + H_2O$$

The deposition temperature for the devices used in this dissertation was 200 °C with a deposition rate 50 nm/min. The deposition was done all over the sample surface. In order to probe the contact pads the SiO_2 from the contact pads were selectively removed. It was done using a PR pattern that selectively opens a small portion of the contact pads of source, drain and gate contacts. The etching of siO_2 was done using dry RIE etching in $CHF_3 + O_2$ plasma. This gives an access for probes to measure the electrical performance of the device.

4.2.6 SiO_2 etching:

The etching of SiO_2 film can be done either in wet chemical etching or reactive ion etching (RIE). Wet etching is purely chemical process with no damage to the underlaying epilayers. The etching process consists of three processes: movement of the etchant species to the wafer surface, chemical reaction with the exposed surface which creates soluble byproducts, removal of the etch products from the surface. One of the most common wet etching processes of SiO_2 is etching in diluted HF solution. The etching of SiO_2 in HF is completely isotropic. The etching reaction for SiO_2 is [17]:

$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2H_2O$$

Since the wet etching is completely isotropic and sensitive to ambient temperature, the etch rate might not be constant. This results in incomplete or over-etching of SiO_2. Over etching of SiO_2 leads to undercut which is not desired in most of the cases.

In order to avoid undercut, dry etching using reactive ion etching (RIE) technique is performed for this study. Etching in plasma environment has several advantages over wet etching: i) plasmas are much easier to start and stop ii) plasmas are less sensitive to small change in wafer temperature iii) plasma etching results in much better anisotropic profiles for small features and produces less chemical waste than wet etching.

Figure 4.8 shows a schematic of a RIE chamber. An RIE system is a parallel plate reactor with one electrode powered with an RF input and the other electrode is grounded, typically to the chamber walls to increase the effective area. Si and SiO_2 surfaces are mainly etched by gases of the C_xF_y family (CF_4, C_2F_6, C_3F_6 and C_4F_8) [106]. F atoms react slowly with SiO_2 in the absence of ion bombardment [107]. This rate is too slow to cause much undercutting in most SiO_2 etching processes. Cl, Br, and H do not react with SiO_2 at room temperature. Ion bombardment greatly accelerates the etching of SiO_2 by F atoms. The typical conditions of such processes are gas pressure < 10 mTorr and input power > 0.1 W/cm^3, which ensure the plasma density at the level of 10^{10}- 10^{11} cm^{-3} and the mean free path in the plasma is in the order of millimeters. Moreover, due to the enhanced directionality of the plasma, the etch profiles are highly anisotropic. Following heterogeneous reaction takes place during the etching process:

$$SiO_y + xF \rightarrow SiF_x + yO$$

In the ion-stimulated chemical reaction the ion bombardment provides the formation of centers of chemisorption for fluorine atoms and the cleaning of the surface from nonvolatile unsaturated silicon fluorides [106]. Etching with C_xF_y gas produce rough surface that makes the process less useful, while it is found that the addition of CHF_3 with C_xF_y produces very smooth etch surface [108].

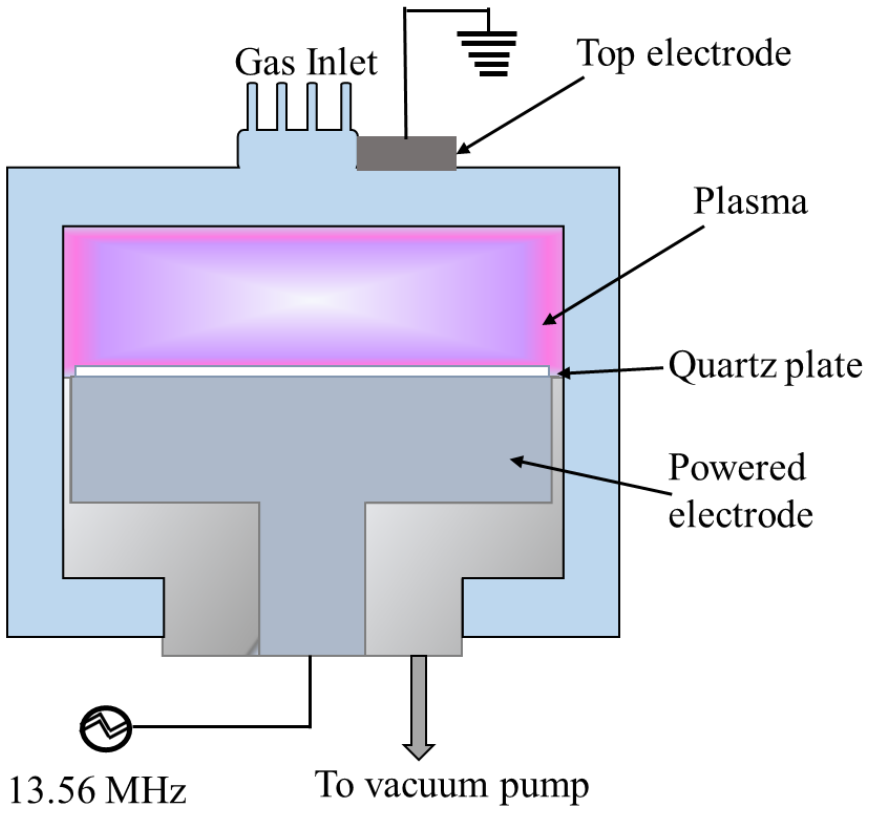


Figure 4.8 Schematic of a reactive ion etching (RIE) chamber

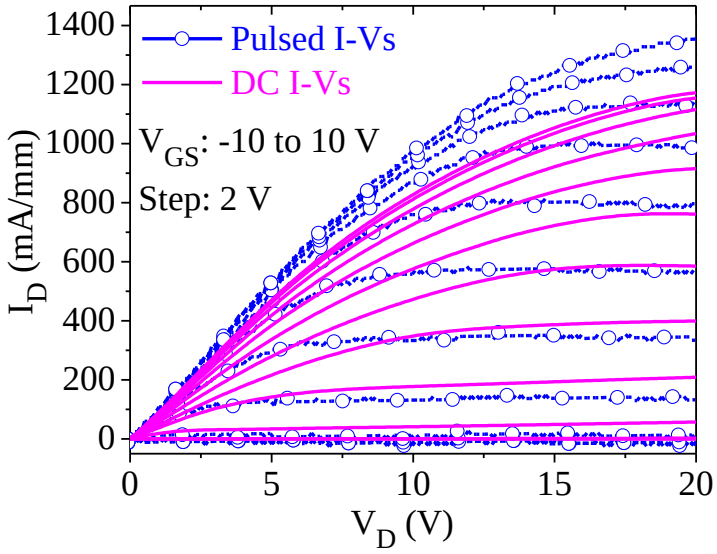
The SiO_2 etching for this study was accomplished by a SAMCO RIE model. Mixture of CHF_3, Ar and SF_6 was used as etching gas that provides an etch rate of ~ 60-70 nm/minute.

4.3 Device Characterization:

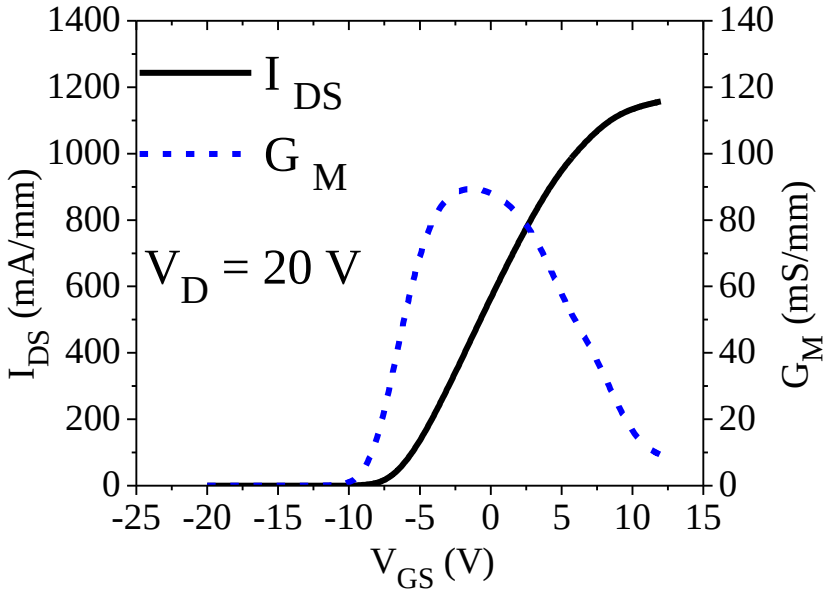
The sheet and contact resistances were measured using TLM patterns. The ohmic contact resistance was found to be 1.7 Ω-mm which is one of the lowest reported to date for UWBG $Al_xGa_{1-x}N$-channel HEMTs.

4.3.1 DC and Pulsed I-Vs:

In addition, the fabricated MOSHFETs were characterized in both the DC and the pulse regimes to reduce heating effects at high drain currents. Short-pulse I-Vs were measured using DIVA D260 dynamic IV analyzer with pulse duration of 500 ns and low duty cycle of 0.1%. Current-voltage characteristics of the MOSHFET with $L_{SD} \approx 8$ μm ($L_{GD} = 4$ μm) are shown in Figure 4.9 (a). The drain currents are normalized to the channel width. For the PC-device the channel width is taken as the total width of all straits. This way of accounting for the total channel width is very similar to that used in large periphery multi-finger FETs. In those devices, substantial (50 – 150 μm long) portions of the gate metal are used to connect elementary sections of multi-finger device; the length of these connections is not included in the total width when calculating the normalized current. In PC design the gate lines connecting straits perform the same function as section-to-section connections in multi-finger design. The hybrid gate dielectric allows operation at a positive gate bias as high as 12 V without any excessive gate-leakage. As seen, pulse drain saturation current is as high as 1.33 A/mm (at V_{GS}=+12V). Even in DC mode the peak drain current exceeds 1.17 A/mm. In Figure 4.9 (b) we include device transfer



(a)



(b)

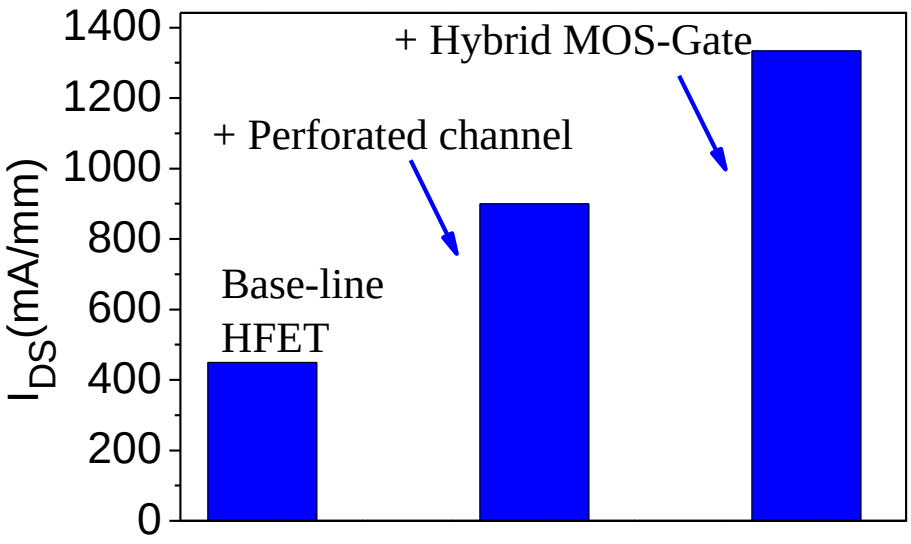
Figure 4.9 (a) IV characteristics of MOSHFET in DC (solid lines), and pulse mode (open circles). (b) DC transfer curve and transconductance at V_D=20 V

characteristics and the transconductance curve in DC mode. The measured transconductance value of 90 mS/mm for DC mode (as high as 110 mS/mm for pulse mode) is also more than twice that of the reported value on identical geometry SiO_2-MOSHFET devices in the past [19]. The total on-resistances for the PC devices, extracted from the I-V slopes at low drain voltage are $R_{ON}(PC) \approx 10$ Ω-mm which is about of factor of two less than R_{ON} of the (CC) device with the same L_{SD}. The threshold voltage Vth = -11 V was the same for both the CC and the PC layouts and was not affected by introduction of additional epi-layers compared to previously reported results [19].

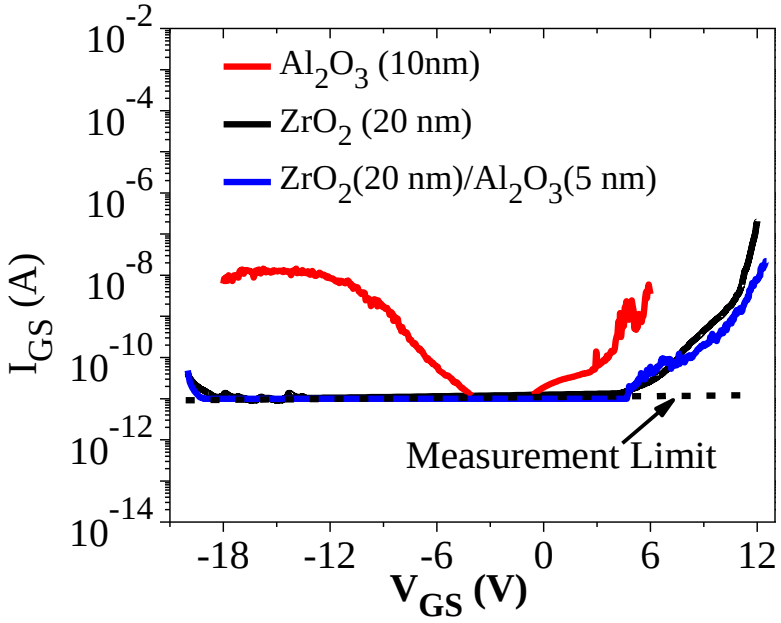
Relative contributions of the three key features employed in current design, namely – (1) perforated channel layout and (2) MOS- gate design – towards maximum drain current are shown in Figure 4.10 (a). It was found that channel perforation doubles the maximum drain saturation current of HFET and hybrid gate oxide increase the device peak current ~1.5×. Figure 4.10 (b) shows reduction of the gate-leakage current that results from hybrid oxide. For the Al_2O_3/ZrO_2 MOSHFET, the gate leakage current remains in μA/mm range even at a gate voltage as high as +12V. The dramatic decrease of the gate leakage current allows device to be operated in positive gate bias regime thus pushing saturation current well above 1.3 A/mm.

4.3.2 Channel Temperature measurement:

As seen from Figure 4.9 (a) the difference between pulse and DC drain currents which we attribute to self-heating is relatively small. To evaluate the self-heating effects, we extracted the active region temperature in the CC and the PC-MOSHFETs by comparing short-pulse drain saturation currents (no self-heating) at different ambient temperatures with DC drain saturation current at the same drain voltage. Short-pulse I-Vs



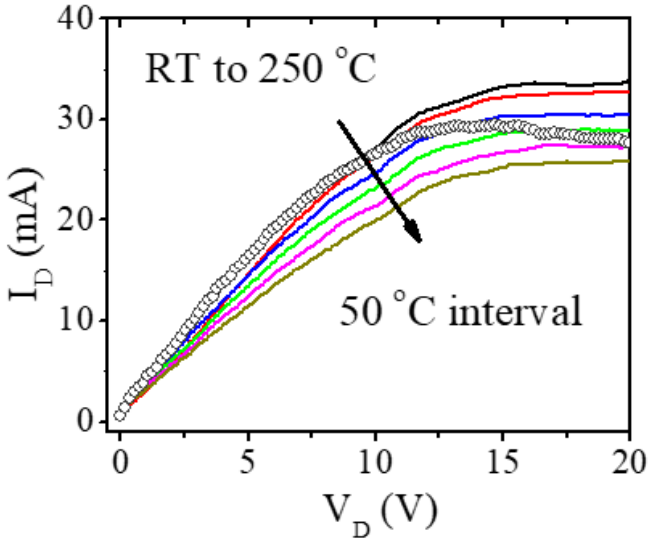
(a)



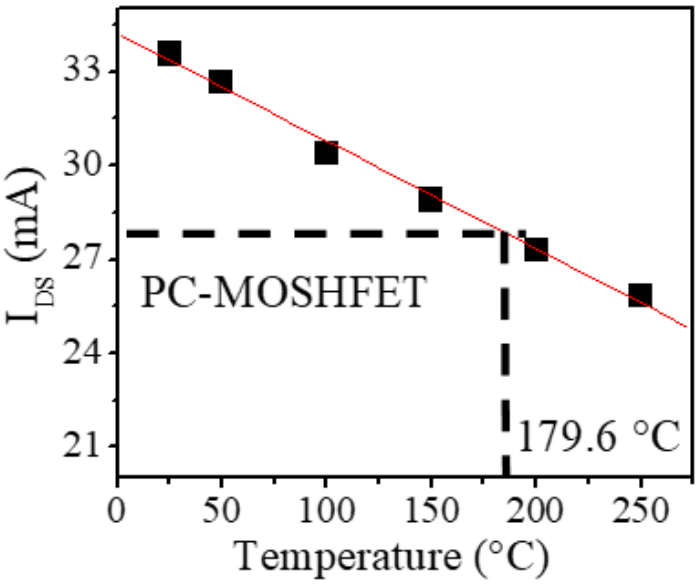
(b)

Figure 4.10 (a) Effect of key factors incorporated in the MOSHFET design on (a) maximum drain current and (b) gate leakage current.

were measured using DIVA D265 dynamic IV analyzer at different ambient temperatures. The probe station stage temperature was varied from room to 250 °C in 50 °C increments. Due to short pulse duration of 200 ns and large duty cycle of 0.04%, we assume that the self-heating effects in these pulse I-Vs can be ignored. To obtain nearly same dissipated power values, conventional and PC-devices with the same total channel width of around 50 μm were selected for this study (thus the full width of PC-MOSHFET was around 150 μm). After that static I-Vs at room temperature were measured for both type of devices, and their saturation currents (obtained from static IVs) were compared with the pulsed saturation current at different temperatures. The temperature at which pulse saturation current is equal to that in CW mode was taken as the active region temperature due to self-heating. Similar techniques were used in the past to extract thermal resistance of III-Nitride devices in [109][110]. To illustrate the method, pulsed I-Vs of the PC-MOSHFET at different temperatures and static I-V of the same device in CW mode are shown in Figure 4.11 (a); Figure 4.11 (b) shows how the device active region temperature was extracted. Similar technique was used to extract the active region temperature for conventional geometry MOSHFET. We found that the channel temperatures for the CC- and the PC-MOSHFET were 329 °C (at dissipated power 0.497 W) and 179.6 °C (at 0.560 W) respectively. The thermal resistance was then found as $R_{TH} = \Delta T / P$, where ΔT is the temperature increase due to self-heating. The obtained thermal resistance for the PC-MOSHFET was $R_{TH\text{-}PC}$ =13 K.mm/W; that of the CC-MOSHFET $R_{TH\text{-}CNV}$ = 29 K.mm/W; therefore, R_{TH}-PC $\approx 0.40 \times R_{TH\text{-}CNV}$. The obtained $R_{TH\text{-}PC}$ value is also smaller than 25K.mm/W reported for III-N HFETs on sapphire in ref [109]. Because the total channel width and hence the power density are about the same for CC- and PC-MOSHFETs, we



(a)



(b)

Figure 4.11 (a) Static (open circles) and pulsed (solid lines) I-Vs of PC-MOSHFET measured at different temperatures as indicated on the graph, pulse width =200 ns; pulse period = 500 μs, V_{GS} =+4V. (b) PC MOSHFET saturation current - temperature dependence in pulse mode (black symbols) and saturation current at room temperature in CW mode (horizontal dashed line). Similar technique was used for conventional geometry MOSHFET.

conclude that the PC design also offers significant improvement in the heat removal. We attribute this improvement to a better heat spreading in the buffer and the AlN template under the straits of PC-MOSHFET.

4.3.3 Breakdown measurement

Figure 4.12 shows the breakdown voltage dependence for devices with different gate to drain spacings of 2, 4 and 8 μm. As seen from the data, breakdown voltage increases to nearly 1000V for the largest spacing. The maximum breakdown field of 2.08 MV/cm achieved for the 2 μm gate–drain spacing exceeds most reported for AlGaN-channel devices [26][24][111]. Note, these devices had no field-plates and they did not undergo any special surface treatment other than the SiO_2 coating. We therefore expect that the breakdown field and the device operating voltages to further go up with better surface treatment and field-plating.

4.3.4 Baliga High-Frequency Figure of Merit (BHFFOM):

An important characteristic of transistor switches is Baliga High-Frequency Figure of Merit BHFFOM [112]. BHFFOM = $f_{BHF} = 1/(R_{ON} \times Cin)$, where R_{ON} is the device on-resistance and C_{in} is the input capacitance. For FETs, $C_{in} \approx C_G$ where C_G is the gate capacitance. At zero gate voltage, $V_G = 0$, the capacitances of the CC- and PC- devices were 8.7 pF/mm and 2.7 pF/mm respectively (see Figure 4.13). Hence, the gate capacitance C_G of the PC-MOSHFET is around 3 times smaller than that of the CC-MOSHFET. Experimentally obtained values of R_{ON} and C_G allow to compare the BHFFOM for conventional and PC-MOSHFETs: $f_{BHF\text{-}CC} = 4.6$ GHz and $f_{BHF\text{-}PC} = 8$ GHz. As evidenced by these results, the maximum switching frequency for PC-MOSHFET is significantly higher than that of a conventional continuous channel geometry device.

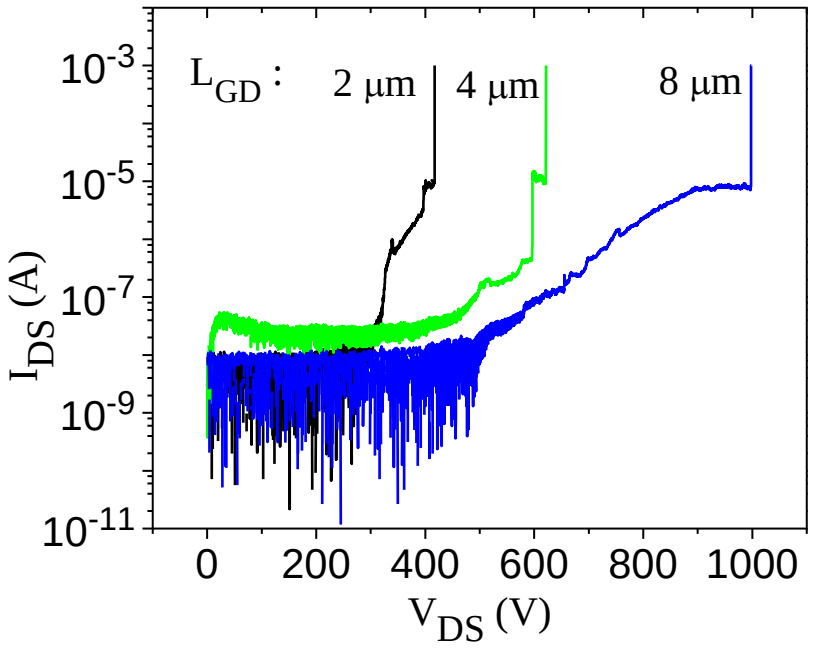


Figure 4.12 Breakdown characteristics of MOSHFETs with different gate-drain spacing.

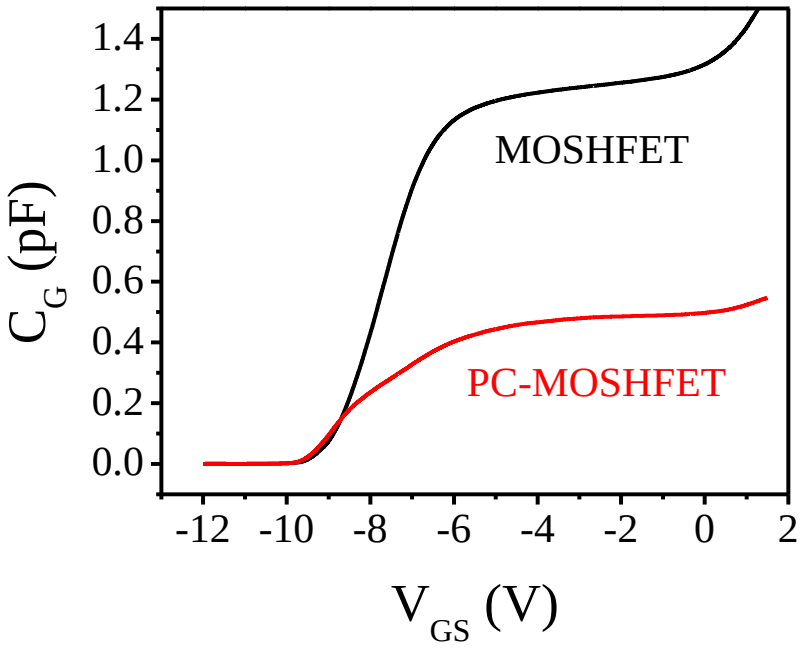


Figure 4.13 C-V characteristics of conventional and PC-MOSHFETs

4.4 Summary

In this chapter, for the first time we have demonstrated perforated channel UWBG AlGaN MOSHFET, with the saturation drain current exceeding 1.3 A/mm. The devices with a new gate-insulator design exhibit a three terminal breakdown field higher than 2 MV/cm and an extremely low gate-leakage current. The PC-MOSHFET device design leads to a factor of two lower access resistance due to the current spreading that occurs between the conducting channel sections and the larger area source and drain contacts. As a result, the PC-device design has nearly a two times higher unit-width channel current and Baliga high-frequency figure of merit. In addition, due to enhanced heat spreading, their thermal resistance is also more than two times lower than a continuous channel device on the same epilayer structure.

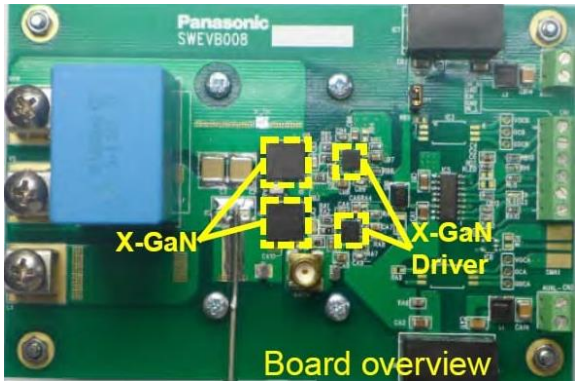
CHAPTER 5: ENHANCEMENT MODE MOSHFET DEVICES

5.1 Background:

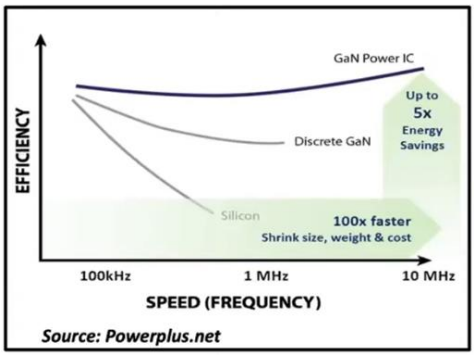
GaN devices are by nature normally-on devices, since the 2DEG channel is immediately present in an AlGaN/GaN heterojunction. However, power electronics industry strongly wished normally-off devices. In several applications, enhancement-mode (E-mode) HFETs are preferable as they provide short-circuit protection power switches [111], eliminate the need of negative bias [113], and are useful in direct-coupled Field-Effect-Transistor logic [114] etc.

Figure 5.1(a) shows a typical cascode GaN power converter circuit where the D-mode GaN power transistor is controlled by the Si power driver. These two are connected with thick Cu wires. Although GaN can operate at very high frequency, due to the parasitic parameters that arise from the circuit arrangement the practical operating frequency is much lower than its capability. Figure 5.1 (b) shows that the efficiency in GaN based IC is pretty much constant over the whole frequency range while it decreases with frequency for discrete GaN as well as Si based GaN power converter. Many researchers are working with GaN based IC to get the full benefit of the material. As a result, there are already some products off the shelf based on integrated E-mode/ D-mode GaN technology as shown in Figure 5.1(c).

Achieving E-mode operation in AlGaN-GaN HFETs has been accomplished by: (i) decreasing the barrier thickness [115][116][117][118][119], (ii) adding cap layers



(a)



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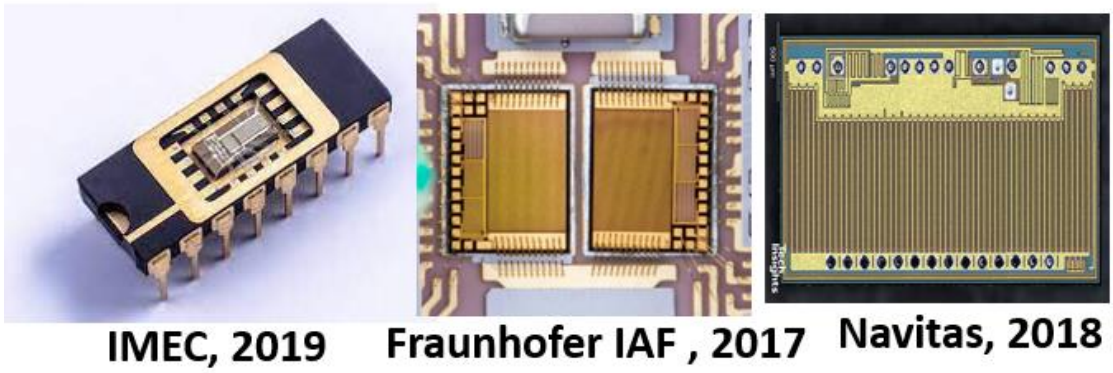


(c)

Figure 5.1 (a) Conventional cascode GaN power converter (b) GaN power converter efficiency as a function of frequency (c) commercially available integrated E-mode/D-mode technology

[120][121][122], and (iii) using fluoride-based treatment [123][124]. Kanamura et al. reported GaN MOSHFET with the highest peak drain current of 0.8 A/mm (at V_G=+10 V) and OFF-state breakdown voltage of 320 V at V_G=0 V [125]. Using linear extrapolation for threshold-voltage (V_{THLE}) they obtained V_{THLE}=+3 V. Asubar et al. demonstrated GaN MOSHFETs with V_{THLE} ~+5 V and a peak current of 425 mA/mm [119]. Several research groups are developing ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ channel E-mode devices for high-temperature, high-voltage, and high-power applications. Recently using fluorine treatment, Klein et al. reported E-mode UWBG $Al_{0.7}Ga_{0.3}N$ channel HFET with V_{TH}=+0.5 V (at I_{DS}=0.1 mA/mm) with a peak current of only 35 mA/mm (at V_G=+6.6V) [32]. In this chapter we discuss fabrication and characterization of high current and high threshold voltage $Al_{0.4}Ga_{0.6}N$-channel E-mode HEMTs that was achieved via gate recess technique. The channel perforation and hybrid oxide that was used for fabricating high current D-mode devices, same techniques were applied here to enable realization of high-current $Al_{0.4}Ga_{0.6}N$-channel E-mode devices.

5.1.1 High-*k* for recessed gate E-mode devices:

Figure 5.2 shows the schematic of a recessed gate AlGaN MOSHFET. In recessed gate devices, in the gate region the AlGaN barrier layer is removed by plasma etch and the recessed region is passivated by an insulator. This device is a hybrid transistor connecting in series the recessed MIS-channel with two access regions having a lower resistance due to the presence of 2DEG. The total on-resistance of this transistor R_{on} is given by the sum of different contributions

$$R_{on} = 2R_C + R_{SG\_2DEG} + R_{CH} + R_{GD\_2DEG} \qquad (5.1)$$

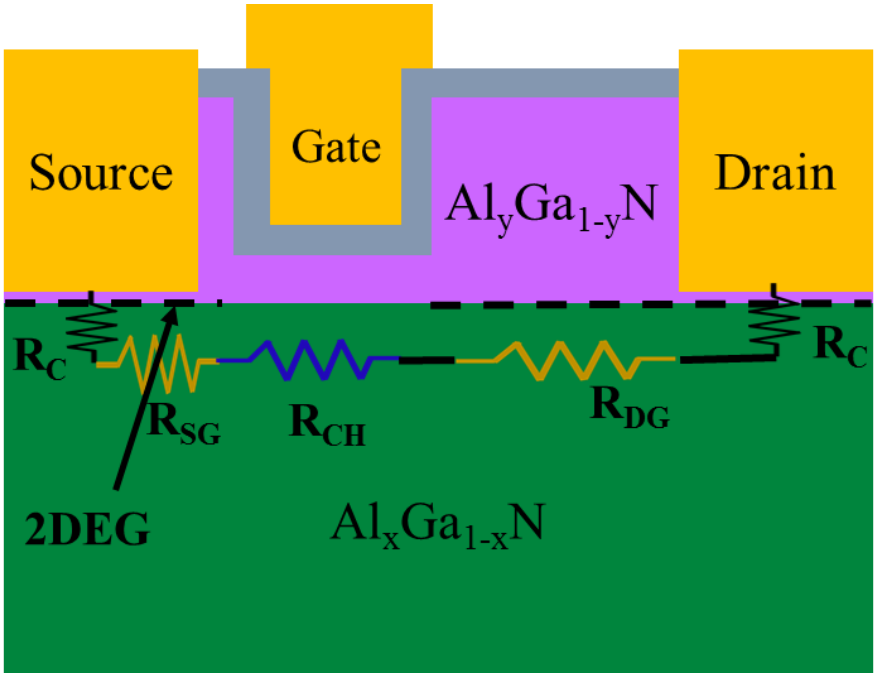


Figure 5.2 Schematic of a recessed gate MOSHFET

The channel resistance R_{ch} is proportional to the gate length Lg and decreases with increasing the channel mobility μ_{ch} [126]. The recessed gate region is the most important part of the normally-off transistor. In particular, the surface roughness of the recessed area, the quality of oxide/semiconductor interface and the presence of electrically active defects can have a significant impact on the channel mobility with subsequent effect on the total resistance. ALD oxides have shown very smooth surface due to its layer by layer deposition compared to PECVD deposited SiO_2 [21]. Interface state density is another important parameter that has adverse effect on field effect mobility. High-*k* oxides shows better screening of the interface state density, thus improving mobility compared to SiO_2 [126]. Most importantly, we have seen in previous chapters that, these high-*k* oxides shift the threshold voltage towards positive direction as opposed to negative shift in SiO_2, which is a major step in E-mode device fabrication. Hence, to fabricate E-mode device high-*k* oxides provide excellent benefits compared to low-*k* SiO_2.

5.2 Experimental Details:

The epilayer structure that was used to fabricate perforated channel D-mode devices, part of the same wafer was used to fabricate perforated channel E-mode devices.

5.2.1 Device Fabrication:

Figure 5.3 (a-f) shows the major steps of E-mode device fabrication. The processing consisted of Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) for mesa-isolation (Figure 5.3 (a)) followed by the formation of source drain ohmic-contacts. Zr/Al/Mo/Au (150/1000/400/300 Å) was deposited with E-beam evaporation and annealed for 30 seconds at 950 °C under N_2 ambient using rapid thermal annealing (RTA) (Figure 5.3 (b)). Perforated channel was made by partially etching the channel material using ICP-

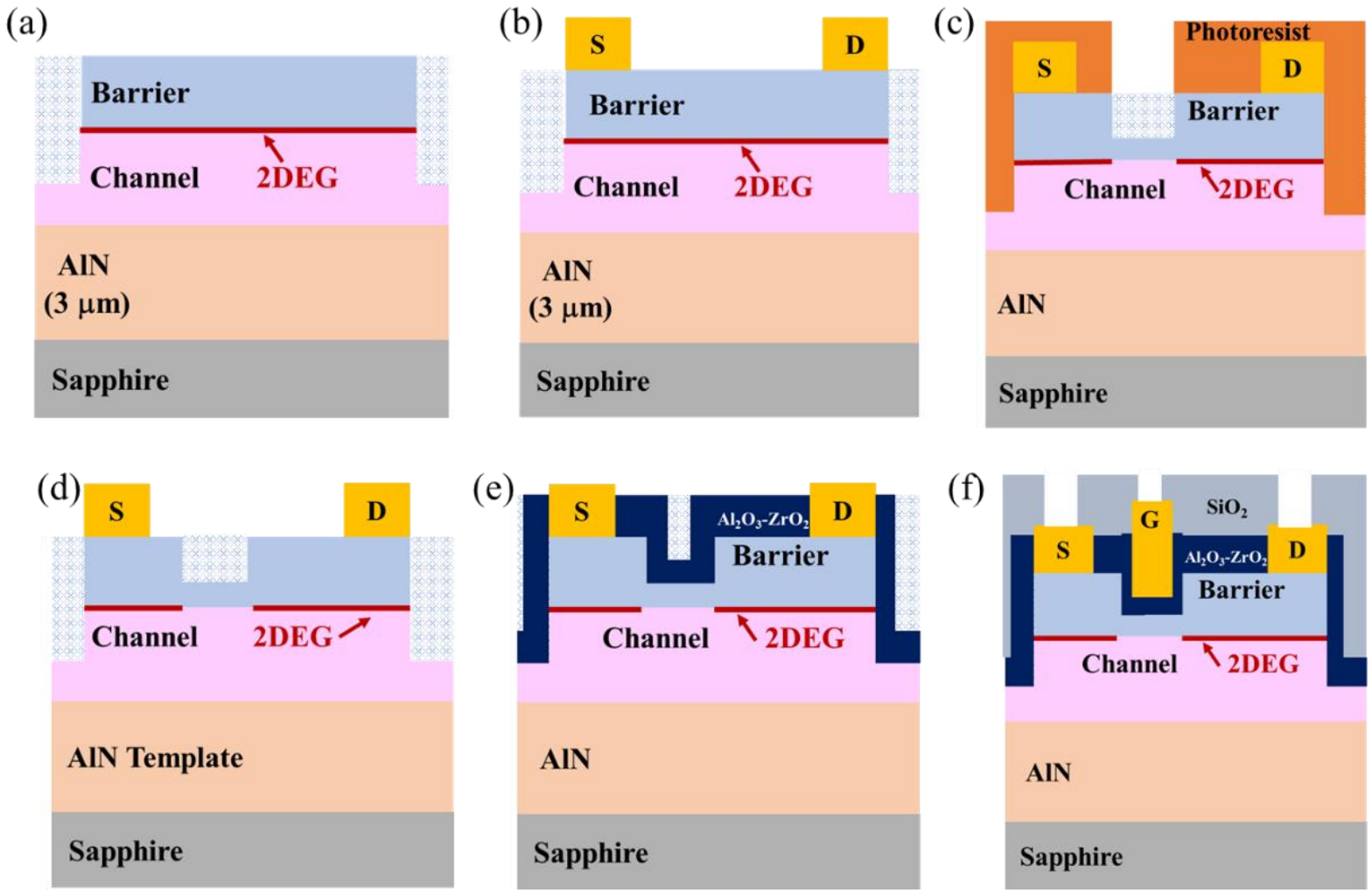


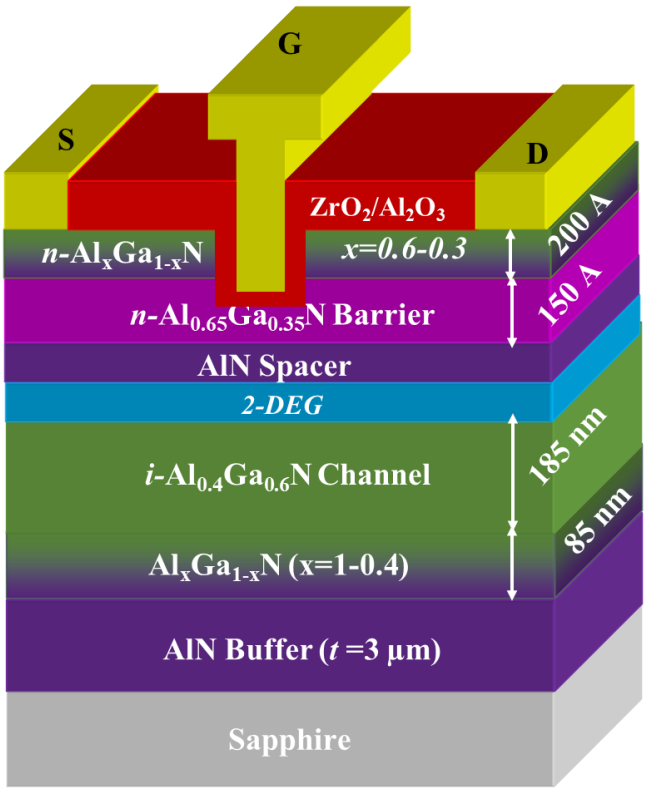
Figure 5.3 major steps of E-mode device fabrication process

RIE which was conducted by exactly same process as described in the previous chapter. As shown in Figure 5.3 (c,d), the barrier was recessed to ~10 nm thickness using a slow ICP-RIE etching process with BCl_3/Cl_2 gas mixture followed by chemical treatment of etched surface with tetramethylammonium hydroxide (TMAH) solution to smooth out the surface as has been done with III-nitrides previously [104][127]. The etch rate of 1 nm/sec was calibrated using Atomic Force Microscopy (AFM). Then a 25 nm thick ZrO_2-Al_2O_3 insulator (ZrO_2 followed by Al_2O_3) stack was deposited in the recess region using Atomic Layer Deposition (ALD) technique before the formation of the Ni/Au gates. The gate-length, gate-source and gate-drain spacings were respectively $L_G \approx 2.0$ μm, $L_{SG} \approx 1.5$ μm and $L_{GD} \approx 2.5$ μm. The transistor surface was protected with PECVD deposited 400 nm thick SiO_2 film for high-voltage breakdown measurements.

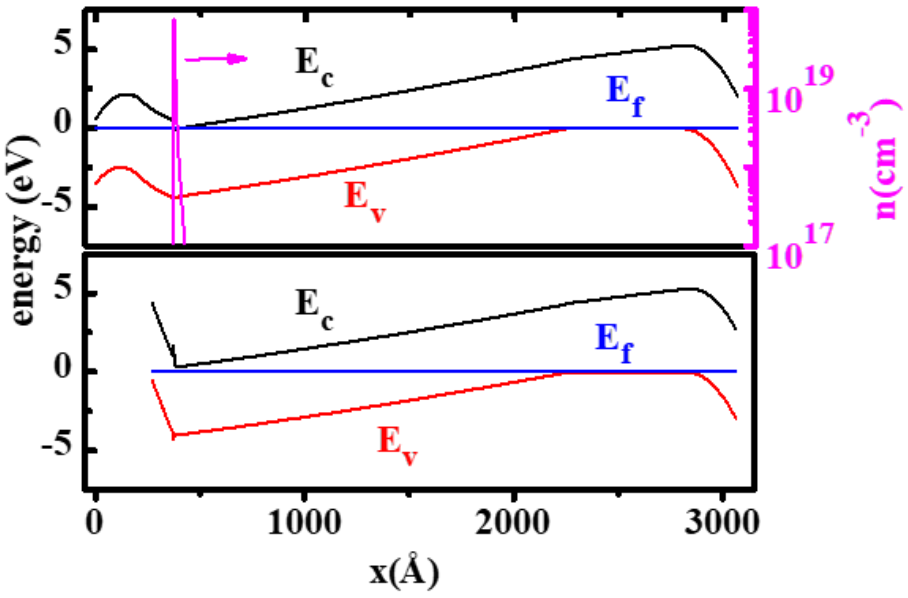
Figure 5.4 (a) shows the schematic of epilayer structure and device geometry of the fabricated E-mode MOSHFET. Figure 5.4 (b) shows the simulated energy band diagram of structure epilayer structure of Figure 5.4 (a) in the cases of barrier recess (bottom) and without barrier recess (top). For recessed barrier structure, the bottom of the conduction band is above E_f, indicating absence of 2DEG at $V_G=0$ V which means normally-off operation, while for structure without barrier recessing there is clear dip of E_c below E_f.

5.2.2 E-mode MOSHFET characterization:

TLM was used to estimate the sheet-resistance (R_S) and the contact resistance to be ~1700 Ω/□ and ~1.7 Ω-mm respectively. The R_S value was within 10% of that measured using rf-eddy current approach. Then perforated channel devices were measured and the drain currents were normalized to the conducting portion of the channel width which is 15.6 μm (W_S) for a 50 μm (W_S+W_B) width unperforated device.



(a)



(b)

Figure 5.4 (a) Schematic layout of recessed gate MOSHFET and (b) Band diagram for epilayer structure of Figure 4.1 (a): without recessed barrier (top) and recessed barrier (bottom).

5.2.2.a DC and pulsed I-Vs:

Figure 5.5 (a) inset shows the source-drain characteristic curves for the recessed-gate Al_2O_3-ZrO_2/PC-MOSHFET with $L_G \approx 2.0$ μm, $L_{SG} \approx 1.5$ μm and $L_{GD} \approx 2.5$ μm. A peak current of 0.48 A/mm was measured at a gate bias of +12 V while it is 0.15 A/mm when normalized to the full channel width (W_S+W_B). Even with normalized to full channel width, the current density is the highest reported value till date for UWBG AlGaN channel E-mode devices. Pulsed I-V measurement was done using DIVA D-265 dynamic IV analyzer with a pulse duration of 500 ns and low duty cycle of 0.1% to avoid self-heating. At V_G = +10 V, the pulsed current was found to be 0.38 A/mm (see Figure 5.5 (b)), a slight increase from 0.36 A/mm DC current. We estimated an ON-resistance (R_{ON}) of 18 Ω-mm. In Figure 5.5 (a) we find V_{TH}=+3.6 V, from linear extrapolation, with a transconductance of 70 mS/mm ($L_G \approx 2.0$ μm). To estimate the V_{TH} variation, ten random devices were measured, spread over 1.5 cm to be representative of the whole quarter of a 2" wafer. The mean V_{TH}= 2.75 V with a standard deviation of 0.57 V (Figure 5.8). The V_{TH} variation across the wafer could be due to following two reasons: i) recess depth variation ii) variation of sheet resistance across the wafer. The most likely cause is recess depth variation ~2nm, which would cause ~0.6 V V_{TH} shift [128], potentially accounting for the observed variation. The sheet resistance variation is most likely caused by variations in carrier mobility across the wafer, as C-V measurements on the as-grown wafers showed similar N_s across the sample.

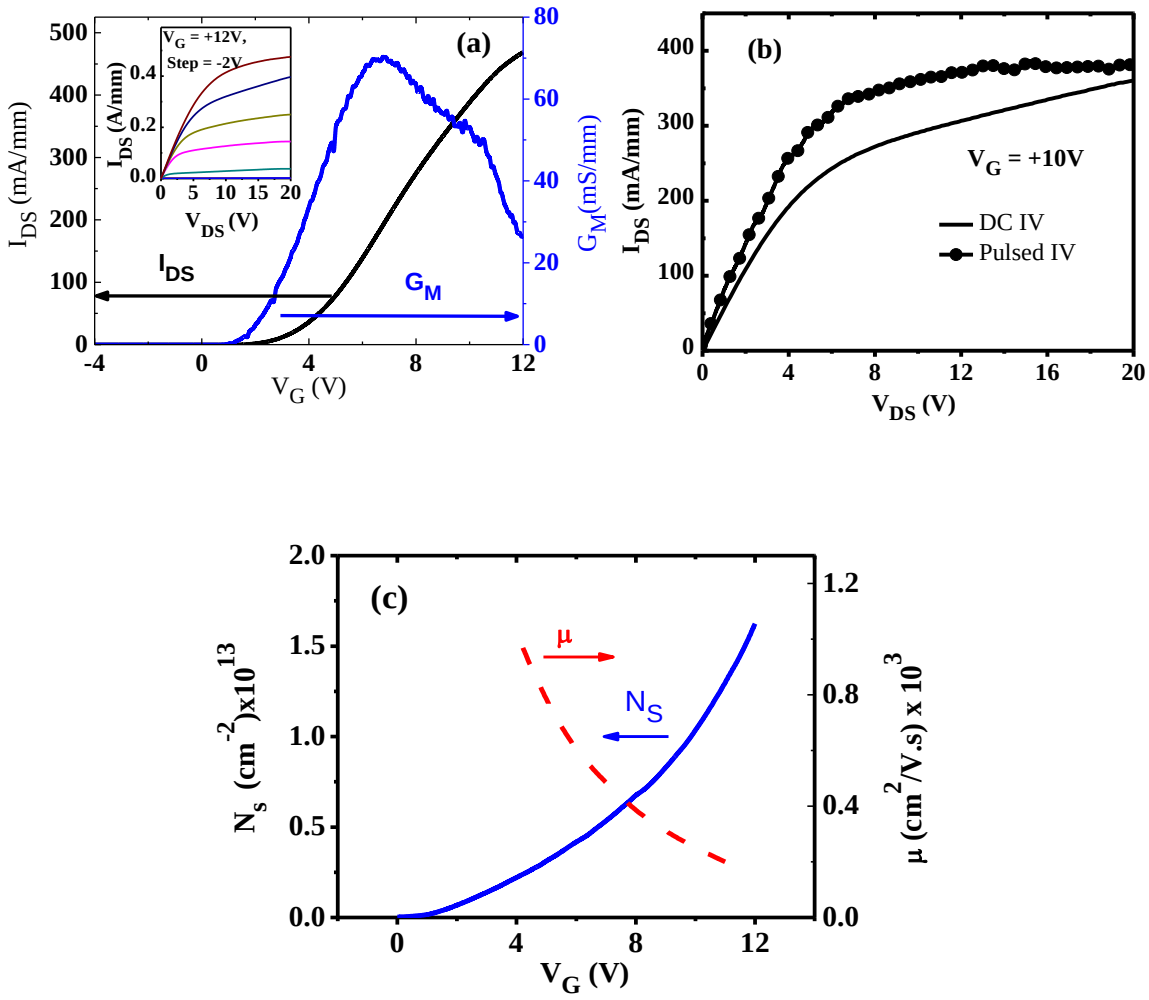


Figure 5.5 (a) source- drain I-V characteristics of a recessed-gate E-mode Al_2O_3-ZrO_2/PC-MOSHFET with L_G=2μm, L_{SD}=6μm and gate-width W_G=50μm (b) DC and pulsed I-v characteristics of E-mode PC-MOSHFET (c) Ns and μ -V_G dependencies for the E-mode MOSHFET device.

5.2.2.b Ns and μ:

To determine the factors leading to the high drain current we extracted the gate voltage dependencies of N_S and μ. Figure 5.5 (c) shows N_S reaching 1.6×10^{13} cm^{-2} at V_G=+12 V. μ is as high as 1050 $cm^2/(V.s)$ near threshold V_G=4 V and decreases to 200 $cm^2/(V.s)$ at V_G +12 V, consistent with the high-*k* MOSHFETs discussed in chapter 3 [129].

5.2.2.c Transfer and gate leakage characteristics:

Figure 5.6 (a) compares the semi-log transfer characteristics for the device of Figure 5.5(a) measured at V_{DS}=+20 V with that for an identical geometry D-mode device (no gate-recess) fabricated on the same wafer, showing a V_{TH} shift of +12.2 volts due to the gate recess. The E-mode device shows a hysteresis of 0.8 V between forward and reverse sweep of gate voltage, higher than that of D-mode (0.2 V) indicating higher trap charges at semiconductor/oxide interface or bulk [125][130]. We speculate this higher trap density might be from barrier recessing. This is supported by the slight increase in subthreshold swing (SS) increase after barrier recess from 105±8 mV/decade for the non-recessed control devices to 138 ± 19 mV mV/decade. The best E-mode device showed SS=128 mV/decade and an ON/OFF ratio > $1.5x10^8$, while I_{GS}<10 μA/mm over the entire V_G range (Figure 5.6(a)).

5.2.2.d Breakdown characteristics:

Three terminal breakdown voltage at V_G=0 V for a device with L_{GD}=4.1 μm, was found to be +700 V (Figure 5.7) which is above +600 V, required for power devices in automotive applications, and has not been reported for UWBG AlGaN E-mode devices [32][131].

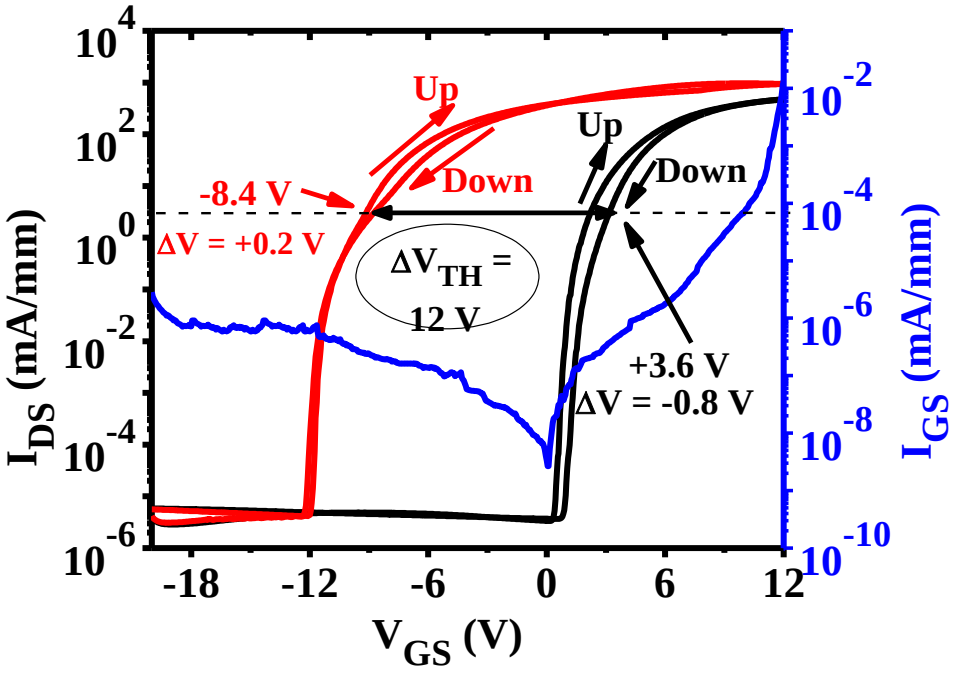


Figure 5.6 (a) Semi-log double- sweep transfer characteristics measured at V_{DS}=+20V for the E-mode device of Fig. 3. The transfer curve for a D-mode device at V_{DS}=+20V is shown for comparison. Also plotted is the gate leakage current of the E-mode device.

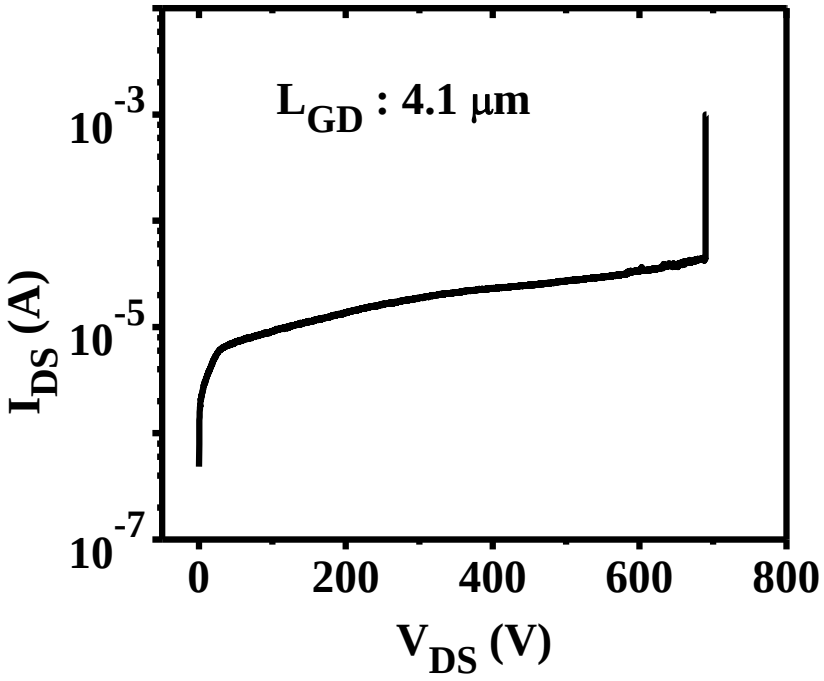


Figure 5.7 Breakdown voltage data for the E-mode device of this study.

We benchmark the Al_2O_3-ZrO_2/$Al_{0.4}Ga_{0.6}N$ channel E-mode devices against other wide (GaN) and ultrawide bandgap (β-Ga_2O_3 and AlGaN) channel E-mode devices in Figure 5.8, where for GaN channel we only included devices with I_{DS} >400 mA/mm [132] [133][134][135][136][137]. Our results show highest current density among ultrawide bandgap materials while compare favorably to some of the best values for GaN despite the greater maturity of GaN-channel HFET technology.

5.3 Summary:

In this chapter, we have demonstrated a recessed-gate enhancement-mode Al_2O_3-ZrO_2/$Al_{0.6}Ga_{0.4}N$/$Al_{0.4}Ga_{0.6}N$ Metal-Oxide-Semiconductor heterostructure field-effect transistor (MOSHFET) with drain current as high as 0.48 A/mm at a gate-source voltage of +12 Volts by applying the perforated channel and hybrid gate oxide that enabled realization 1.3 A/mm record drain current for depletion mode MOSHFETs. The device exhibited a threshold-voltage (V_{TH}) of 2.75±0.57 V with absolute maximum V_{TH} =3.6 V, a +12.2 V shift from that for a depletion-mode MOSHFET fabricated on the same wafer. A 3-terminal breakdown voltage of 700 V was measured in the off-state, showing the viability of E-mode UWBG AlGaN for power electronics.

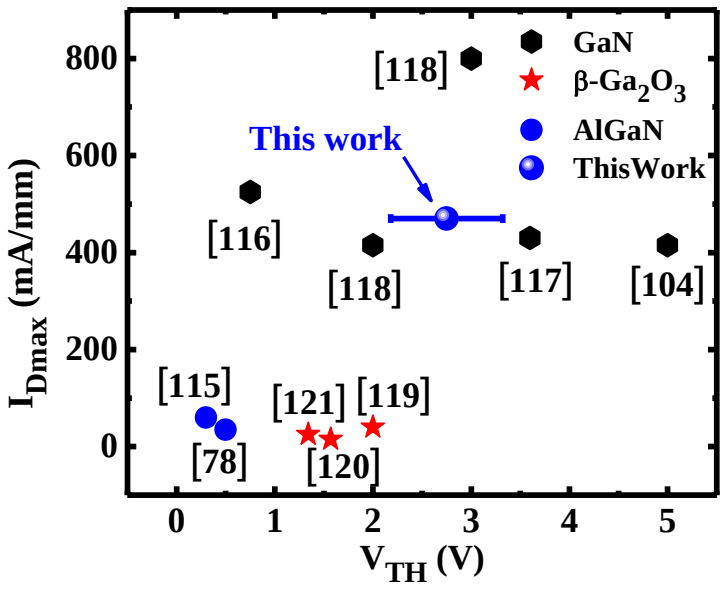


Figure 5.8 Comparison of our reported results with I_{DMAX} and V_{TH} of some normally-off wide bandgap GaN as well as UWBG AlGaN and Ga_2O_3 channel HEMTs reported in literature.

CHAPTER 6: TEMPERATURE CHARACTERISTICS OF HIGH-CURRENT UWBG ENHANCEMENT AND DEPLETION MODE ALGAN-CHANNEL MOSHFETS

6.1 Background:

Due to their high FOM III-nitride (III-N) based power switching transistors are destined to operate over broader temperature ranges. Hence, their temperature (T)-dependent behavior and stability are of critical significance to the III-N power circuits and systems. III-N depletion and recessed-gate enhancement mode MOSHFETs as two predominant types of III-N power devices featuring insulated gate structures, are encountered with challenges of V_{TH} instability originating from the interface traps at the gate-dielectric/III-N interface [138]. The thermally sensitive electron emission processes of the interface traps make such studies critically important for devices intended for high-power, high-temperature and harsh environment condition operation. In this chapter we present the studies of performance characteristics of the high current D-mode and E-mode devices at elevated temperatures up to 150 $^{\circ}$C. The measurement for this study were done using heated probe station.

6.2 Temperature dependent characterization:

6.2.1 Drain current density:

Figure 6.1 (a-c) shows the output characteristics of the D- and E-mode MOSHFETs at elevated temperature. As the temperature increases the D- and E-mode MOSHFETs

behave differently. While the output current decreases in D-mode MOSHFETs, it increases in E-mode MOSHFETs. Details about the mechanism will be discussed in the later part of this chapter.

6.2.2 V_{TH} and μ:

Next, we studied the temperature dependencies of the threshold voltages of D- and E-mode MOSHFETs. The temperature dependent V_{TH} are shown in Figure 6.2 (a). As seen, for the D-mode MOSHFET, the V_{TH} experiences positive V_{TH} shift of + 1.7 V from RT to 150 °C; for the E-mode MOSHFET the shift is negative: -2.9 V. Figure 6.2 (b) shows the mobility variation with temperature, μ(T), for a sheet carrier density $N_S=1\times10^{13}$ cm^{-2}. μ(T) in D-mode devices decreases with temperature while it increases for E-mode devices.

6.2.2.a Dominant mobility mechanism in D- and E-mode MOSHFETs:

By power law fitting of μ(T), indices (α) in the equation $\mu= AT^{\alpha}$ were obtained as -0.4 and +0.5 for D and E-mode devices respectively. This means that in D-mode devices the mobility is dominated by phonon scattering (typically in GaN $-2<\alpha<-1$) mixed with alloy scattering ($\alpha\approx0$) while in E-mode it is dominated by ionized impurity or charge scattering (typically in GaN $+1<\alpha<2$) and alloy scattering ($\alpha\approx0$) [139][140]. We attribute the increased charge scattering in E-mode devices to the additional fixed charges and interface traps introduced by barrier recess, as will be discussed separately below. For the D-mode device, the V_{TH} gets more positive with temperature increase. This means that the total channel charge decreases, along with μ(T). We therefore expect the drain current to decrease with temperature. For the E-mode device, the V_{TH} gets more negative reflective of an increased channel charge, as μ(T) also increases. Therefore, the overall drain current is expected to increase with the temperature, as was observed (see Figure 6.1).

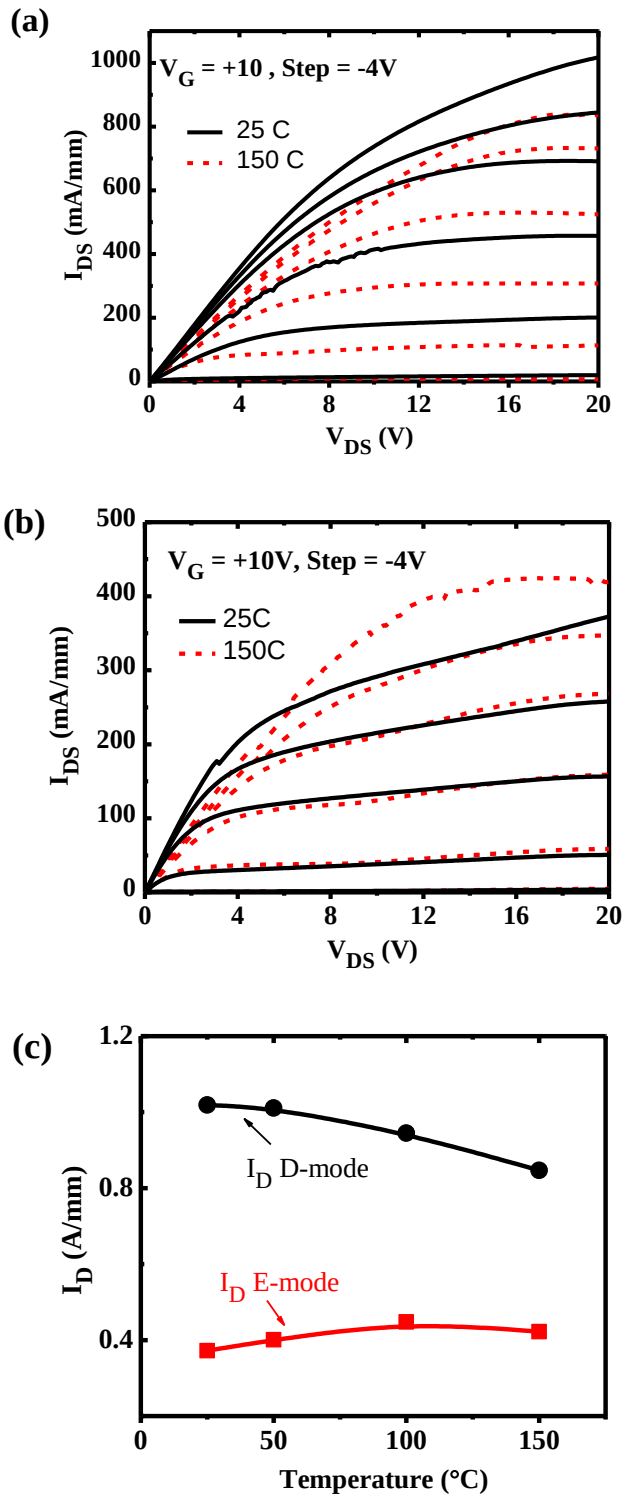


Figure 6.1 Drain current density of D- (a) and E-mode (b) devices at room temperature and 150 °C (c) Drain current plot as a function of temperature for D- and E-mode devices.

6.3 Temperature induced threshold instability mecanism:

To further analyze the mechanisms leading to significant V_{TH} shifts with temperature in MOSHFETs, we compared them with those of a similar device having Schottky gate (no dielectric). As seen from Figure 6.2 (a), the V_{TH} shift for HFET is significantly smaller, +0.2 V. This shows that the V_{TH} shift is mainly due to the charges in dielectric or at dielectric-barrier interface. The extracted subthreshold swing (SS) value for D and E-mode devices were 99 mV/decade and 134 mV/decade giving ideality factor (n) of 1.7 and 2.3 respectively (Figure 6.3 (a)), indicating an increased density of interface traps at the recessed interface in the E-mode device [141]. Frequency dependent C-V measurements were carried out to identify interface state density (D_{IT}) in the depletion and enhancement mode MOSHFETs. In Figure 6.4 we include the C-V data at room temperature. The extracted values of D_{IT} as a function of temperature are plotted in Figure 6.5. Like the observed V_{TH} shifts, the D_{IT} for E-mode MOSHFET is higher than that for D-mode device. We attribute this larger D_{IT} value in E-mode devices to the barrier recessing process which introduces traps at the oxide/semiconductor interface, consistent with the increased SS. Similar trends have been observed in a study from Yang et. al [142].

In addition to D_{IT} causing the V_{TH} shift, we will argue that fixed oxide charges (Q_{ox}), as measured by C-V are also responsible. For these C-V measurements, we used devices with gate-length L_G= 80 µm, and gate-width W=200 µm. With the measured C-V data, we conducted electrostatic analysis determine the fixed oxide charges[46]. The detailed procedure is described in chapter 3. The extracted Q_{ox} (T) is plotted in Figure 6.5. It shows that in D-mode device, Q_{ox}(T) is much higher than D_{IT}(T). These are fixed negative charges which deplete the channel, and shifts V_{TH} more positive, giving a

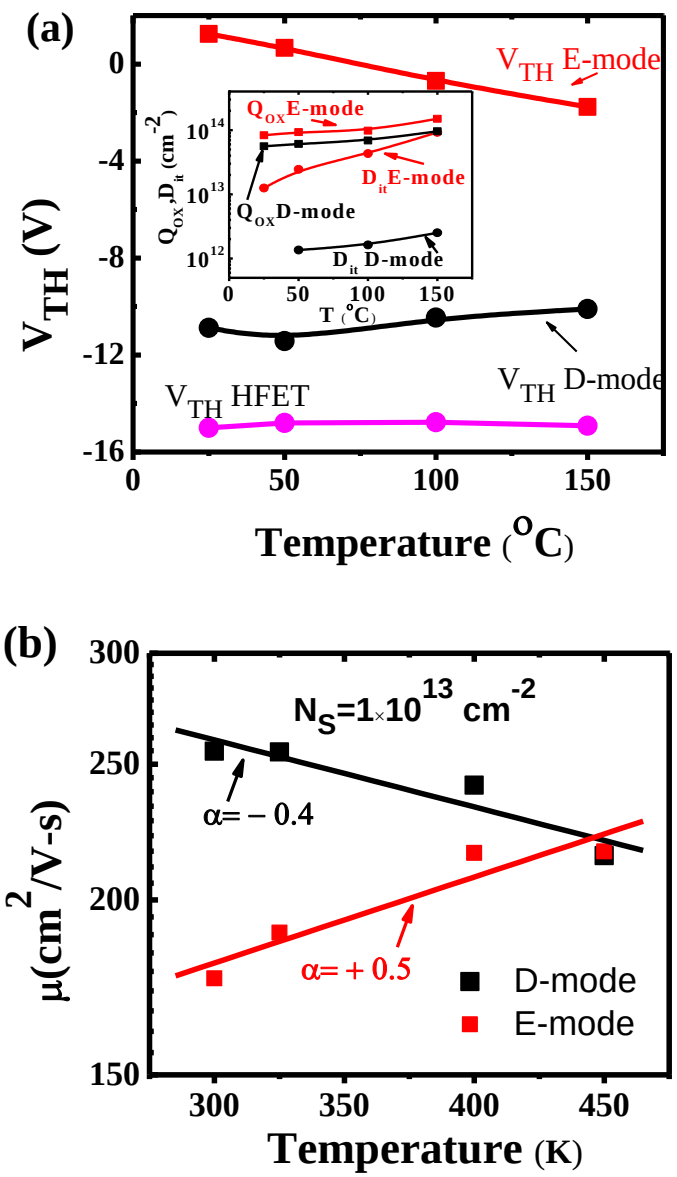


Figure 6.2 (a) Temperature-dependent threshold voltages for D- and E-mode devices. The V_{TH} shifts from RT to 150 °C are -2.9 V for E-mode and + 1.7 V for D-mode MOSHFETs; For comparison, the V_{TH} shift of +0.2 V for Schottky-gate D-mode HFET is also shown. (b) Power law fitting of mobility versus temperature to extract power law indices (α).

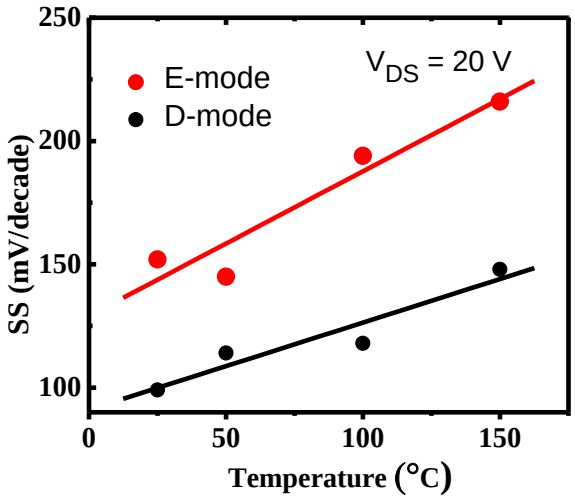


Figure 6.3 Temperature dependent subthreshold swing (SS) for D and E mode devices.

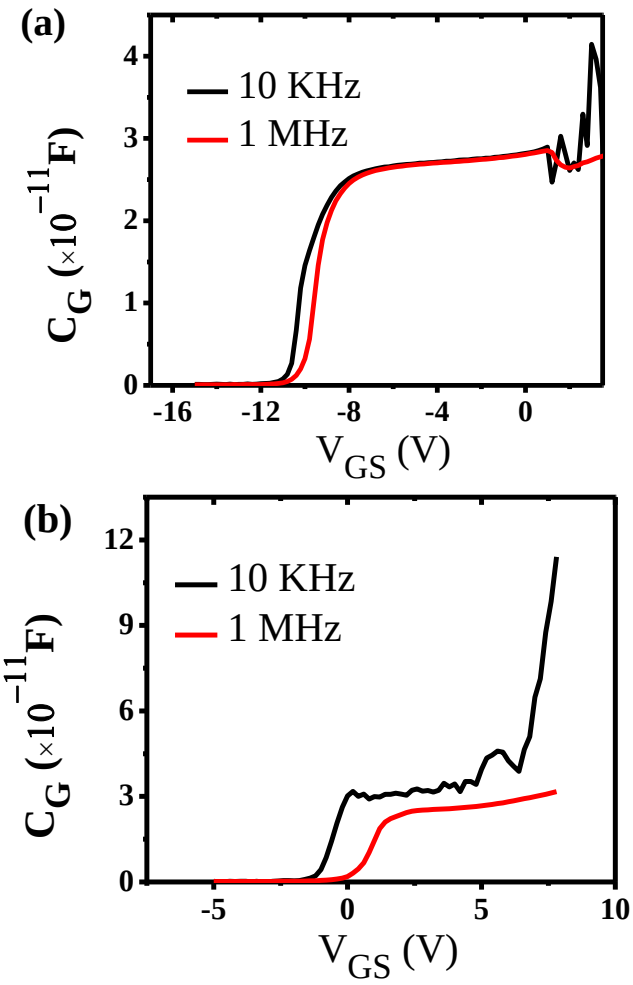


Figure 6.4Frequency dependent C-V characteristics of D- (a) and E-mode (b)

MOSHFETs.

total shift of +1.7 V from RT to 150 ^{O}C. In E-mode device, the Q_{ox} and D_{IT} values are comparable, thus the effect of Q_{ox} is compromised by D_{IT}, thus shifting the V_{TH} in opposite direction. We use these values of fixed charges in a 1-D Poisson Solver simulation [143] and observe similar V_{TH} shift from from RT to 150 ^{O}C. The experimental and simulated data are plotted in Figure 6.6.

Our results suggest that a deep sub-bandgap trap level (E_t) located near mid-bandgap plays the role for positive and negative V_{TH} shift in D and E-mode devices respectfully as has been done with AlGaN/GaN HEMT's [144]. We assume this state is donor-like, neutral when occupied and positive when empty. In D-mode device, at RT majority of the trap states contribute electrons (positively charged) to form N_S and the fermi level (E_f) is well above the bottom of the conduction band (Figure 6.7) [16]. As the temperature increases trap states start occupying electrons from 2DEG, moving E_f down towards the intrinsic midgap position. At elevated temperature, the 2DEG density is less than that of room temperature. As a result, less negative voltage is required to deplete the channel compared to room temperature, causing a positive threshold shift.

In the E-mode devices, at RT the E_f is between E_t and E_v. With temperature rise the E_f moves up, filling more trap states. Electron transfer then occurs to conduction band of $Al_{0.4}Ga_{0.6}N$ which is close to E_t. As the temperature keep increasing, more and more electrons transfer from the trap states to 2DEG. Additional negative voltage required to deplete the excess electrons causing a more negative threshold shift.

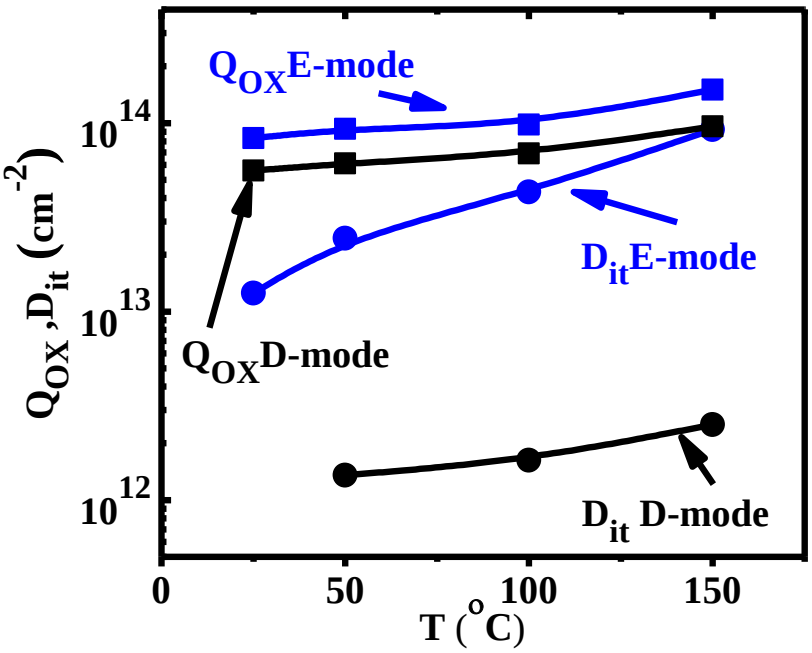


Figure 6.5 the temperature dependence of interface state density (Dit) and oxide charge(Qox))

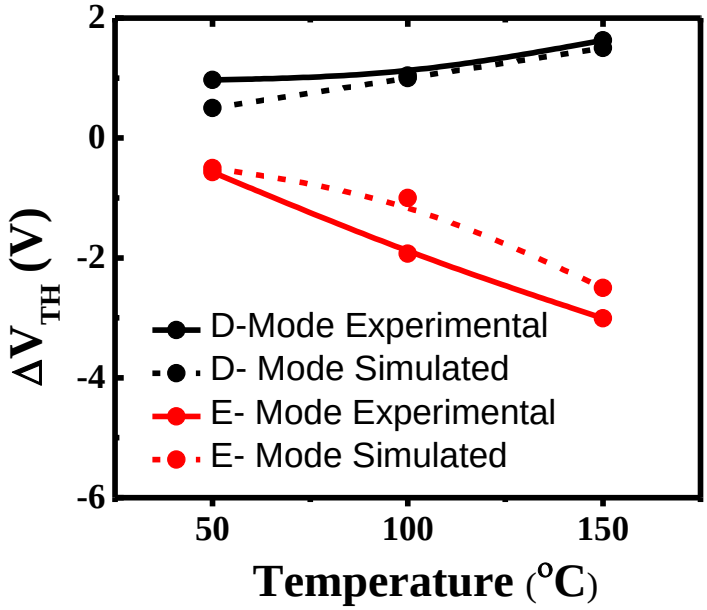


Figure 6.6 Experimental and simulated V_{TH} shift as a function of temperature. The simulated data were achieved using 1-D Poisson solver.

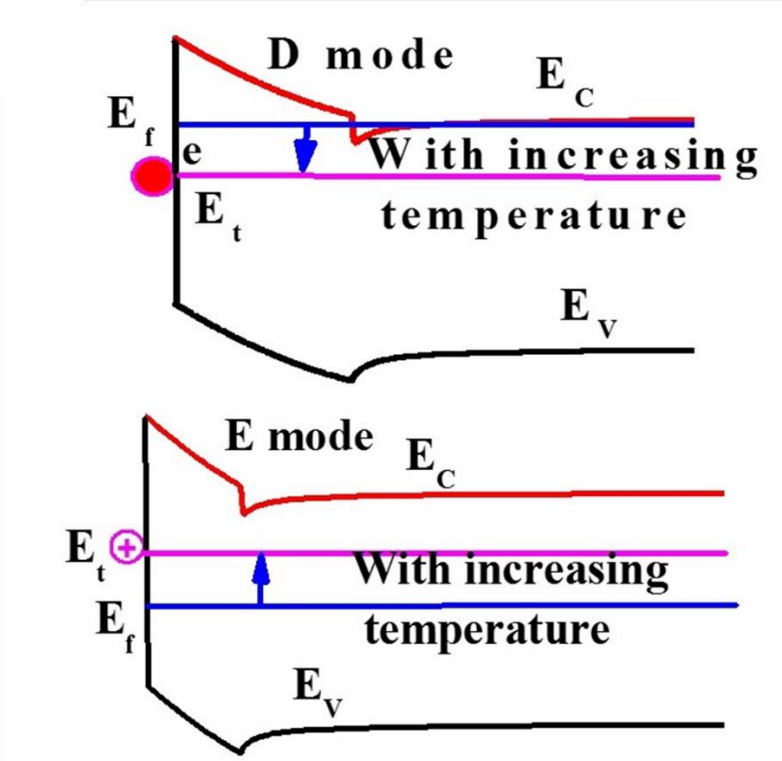


Figure 6.7 Schematic energy band diagram showing the trap energy level (E_t) and position of the Fermi level relative to E_t.

6.4 Summary:

In summary, we presented temperature dependent electrical characteristics of high-current depletion (D-mode) and barrier-recessed enhancement-mode (E-mode) ultrawide bandgap (UWBG) $Al_{0.4}Ga_{10.6}N$ channel insulated gate heterojunction field-effect transistors (MOSHFET's) fabricated on the same wafer. Over a temperature range of 125 °C, the V_{TH} shifted in opposite direction for D and E-mode devices with a rate of +13.5 mV/K and -23 mV/K respectively giving an overall shift of +1.7 V and -2.9 V. This was attributed to changes in the fixed and trapped charge densities in the dielectric and at the dielectric–AlGaN barrier interface. A single deep sub-bandgap trap level was sufficient to explain the threshold shifts in both devices. The effective channel mobility in the E-mode devices was argued to be limited by charge scattering, arising from the same charges introduced during barrier recessing that shifted V_{TH}.

CHAPTER 7: CONCLUSION AND FUTURE WORK SUGGESTION

7.1 Conclusion:

This thesis has studied the issues of threshold voltage control and gate leakage in high power metal-oxide semiconductor heterojunction field effect transistors (MOSHFETs) which were based on ultrawide bandgap (UWBG) AlGaN channels. UWBG AlGaN materials, despite their clear benefits due to higher figure of merit, large V_{TH} in AlGaN-MOSHFET devices compared to HFET devices limit their usage for practical application and this have been a bottleneck for high performance MOSHFET device fabrication. Through this dissertation novel solutions to this problem have been proposed and high-performance devices have been demonstrated.

A large portion of this thesis is dedicated to understanding the mechanism of threshold voltage shift in UWBG AlGaN-channel MOSHFETs and demonstrates the V_{TH} control using high-*k* gate dielectrics that was achieved using high temperature gate oxide annealing. Several high-*k* ALD oxides such as ZrO_2, Al_2O_3 and TiO_2 were studied. For these, in addition to the V_{TH} control and gate-leakage reduction, the effect on other device parameters such as mobility, sheet carrier density and current collapse were also studied. Our analysis shows that, in these high-*k* ALD MOSHFETs the polarity of the

interfacial oxide charges can be controlled using high temperature annealing which in turns enable positive V_{TH} shift. Positive V_{TH} shift is an important step in achieving low threshold D-mode as well as E-mode device fabrication. All the fabricated MOSHFETs show severe current collapse under the application of gate and drain pulses due to the presence of additional interfacial and bulk oxide charges, Si_3N_4 passivation shows effective removal of current collapse in these high-*k* ALD MOSHFETs.

State of the art depletion and enhancement mode UWBG AlGaN-channel devices were realized using hybrid ZrO_2/Al_2O_3 gate dielectric in combination of pseudomorphic epilayer structure and perforated channel geometry to achieve lower access resistance. Hybrid oxide layer enabled realization of forward gate voltage swing as high as +12 V, resulting record drain current density of 1.3 A/mm and 0.48 A/mm for D- and E-mode MOSHFETs, respectively. These devices offer extremely low gate leakage current. A breakdown voltage of +700 V was achieved in these devices for a gate-drain spacing of 4.1 μm without any field plate. The high ON-state drain current density and OFF-state breakdown voltage make these devices potential candidate for high power switching application. Moreover, these devices will find applications in high power/voltage amplifiers and will operate at temperatures in excess of 250 °C.

Despite significant progress in AlGaN channel device performance demonstrated in this thesis, still there are room for improvements. In the following sections, novel approaches are discussed that can further improve the AlGaN-channel device performance in the future.

7.2 Future Work:

7.2.1 Monolithically Integrated D- and E-mode MOSHFET:

Most of the commercially available drive modules or peripheral logic control for GaN-based power converters are still implemented with Si integrated circuits (ICs) [145] [146]. Such a hybrid scheme with GaN power devices and Si ICs inevitably consumes more board space and yields larger parasitic inductance, which could limit the performance of GaN power switches under high-frequency operation [147]. Instead, the direct-coupled FET logic (DCFL) ICs with monolithically integrated Enhancement/Depletion-mode n-channel devices offer a straight-forward and convenient approach to implementing GaN digital ICs [148][149]. Several groups have developed GaN channel based ICs [149][150][151], while till date there is no report on AlGaN channel-based ICs.

Taking the advantages of the high-performance D and E mode UWBG AlGaN channel devices discussed in this dissertation, for future work we suggest design and fabricate AlGaN channel based integrated device for high temperature, high voltage and high-power application. Figure 7.1 shows the schematic of monolithically integrated D- and E-mode MOSHFETs.

7.2.1.a Mask Layout Design:

To fabricate the D/E-mode integrated HEMT we will need Photoresist mask for each level of fabrication. The mask will be designed using AutoCAD design tool. Following are the mask levels that will be required to accomplish the work:

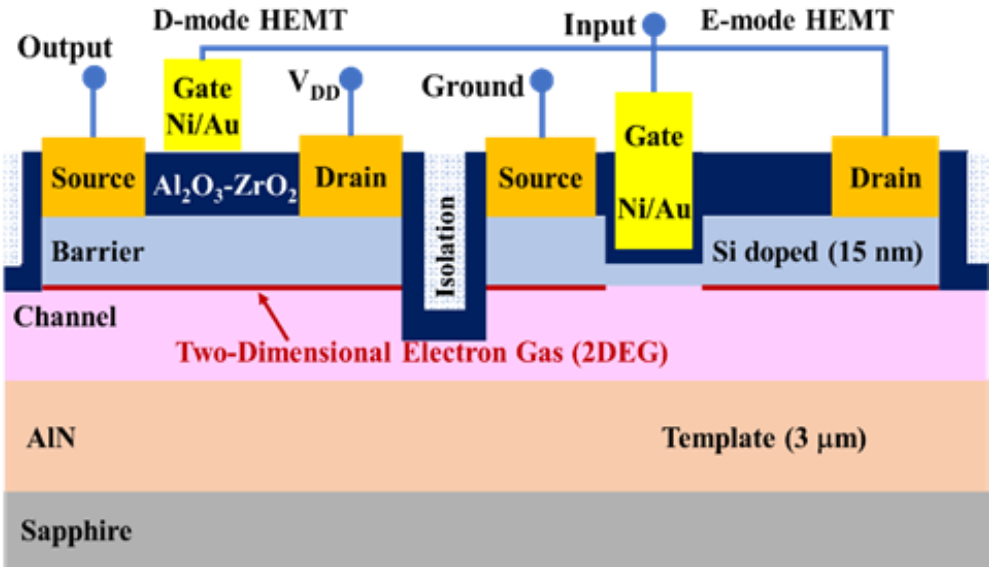


Figure 7.1. Schematic of monolithically integrated D and E mode MOSHFET

i) MESA etching

ii) Ohmic contact formation

iii) E-mode Gate recess

iv) Ohmic opening after Oxide deposition

v) Depletion and Enhancement mode Gate Forming

vi) Interconnection

7.2.1.b Device Fabrication, Characterization:

The major processing steps are shown in Figure 7.2. The device fabrication will be followed by detailed characterization in order to extract the device performance parameters (breakdown voltage, mobility, sheet carrier density, peak current) at room temperature as well as elevated temperature.

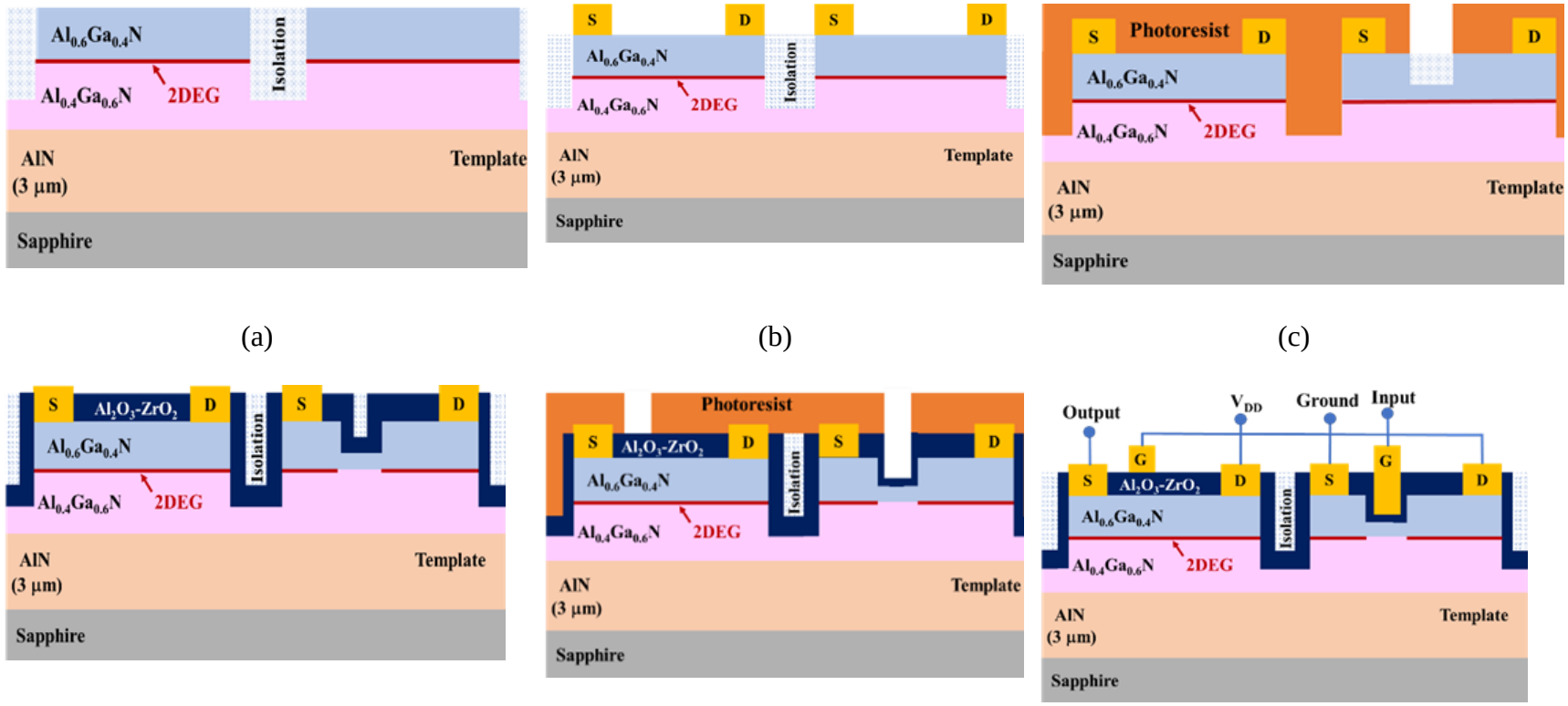


Figure 7.2 Major Processing steps (a) MESA isolation between Depletion and Enhancement mode (b) Ohmic (Source/Drain) contact formation (c) E-mode device gate definition and recess (d) Al_2O_3-ZrO_2 gate insulator deposition using Atomic Layer Deposition (ALD) technique and ohmic contact (Source/Drain) region opening (e) D and E-mode device gate definition with photoresist (f) D and E-mode device gate metallization and interconnections .

7.2.2 Enhancement of Breakdown Field:

7.2.2.a Field Plate:

In GaN-channel devices, the use of field plate have shown to significantly increase the breakdown. The main purpose of the field plate is to reshape the electric field distribution in the channel and to reduce the peak value on the drain side of the gate. The benefit is an increase of the breakdown voltage and a reduced high field trapping effect. The breakdown field for the AlGaN-channel MOSHFETs reported in this dissertation is ~ 1.7 MV/cm which is much lower than the theoritical breakdown field for 40% Al AlGaN channel layer i.e, ~7 MV/cm. The application of field plate will further improve the device performance to enhance the potential of these high performance devices. Figure 7.3 shows a typical MOSHFET device with source connected field plate.

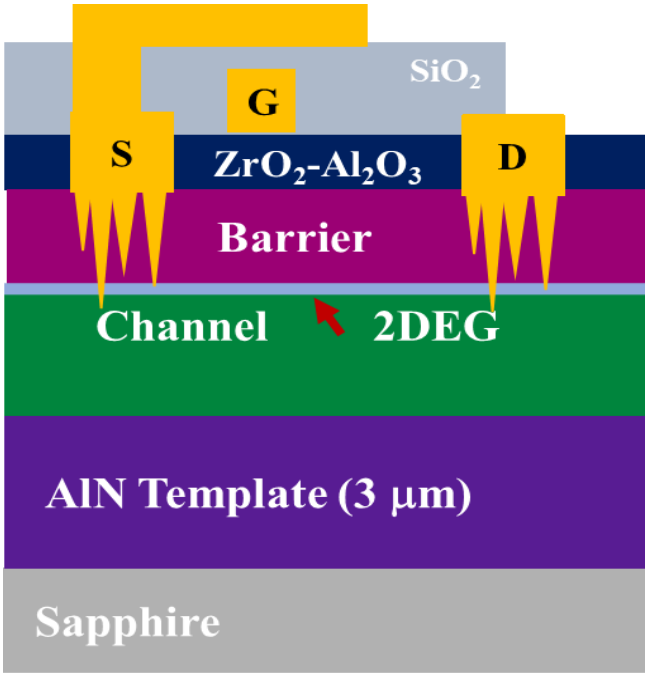
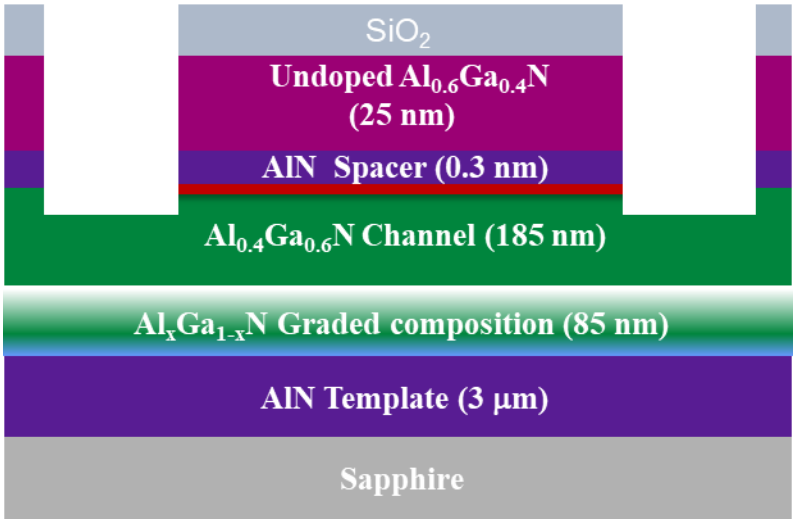


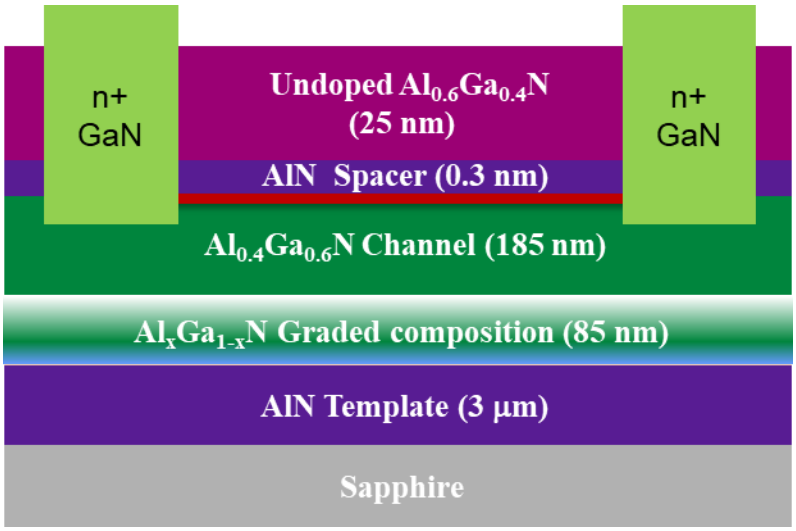
Figure 7.3 MOSHFET device with field plate design

7.2.2.b Undoped Barrier/Selective area contact regrowth:

The MOSHFET devices reported in this dissertation contains very highly doped AlGaN barrier layer to form low resistance ohmic contact. High barrier doping facilitates ohmic contact formation but it accelerates the device breakdown thus reducifng the breakdown field. To achieve the full potential of AlGaN material it is extremely important to enhance the breakdown voltage that demands undoped barrier epilayer structure design. The alternate and more promising way of contact formation on undoped barrier layer is selective area contact regrown technique which is integrated growth and process based technology. In this approach the whole wafer is covered with SiO_2 hard mask. Source and drain contact region are defined dusing photolithography followed by the SiO_2 removal and epilayer etching using ICP-RIE as shown in Figure 7.4(a). Extremely doped GaN is grown in the ohmic contact area as shown in Figure 7.4 using MOCVD system that ideally proives connection between the source/drain metal and the 2DEG. In this way the drawback of early breakdown coming from the doped barrier design can be avoided. There are growth and device processing challanges with this approach. Research is going on to solve these challanges by many groups all over the world including ours. Current ongoing research and development at the Photonics and Microelectronics Lab in the University of South Carolina directed by Prof. Asif Khan is giving hope to solve these issues and moving to next step of achieving theoritical limit of UWBG AlGaN based HEMTs.



(a)



(b)

Figure 7.4 (a) source and drain ohmic region recessed for n+GaN regrowth (b) n+GaN regrown contacts

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