Modeling and Loss Analysis of SiC Power Semiconductor Devices for Switching Converter Applications

Soheila Eskandari

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Modeling and Loss Analysis of SiC Power Semiconductor Devices for Switching Converter Applications

by

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DEDICATION

This dissertation is dedicated to my dear husband, Dr. Rahim Ghorbani, my lovely sister, Dr. Sonia Eskandari and my sweet son, Ryan for their love, endless support and encouragement.
ACKNOWLEDGMENTS

First and foremost, I would like to express my sincere gratitude and appreciation to my PhD advisor, Dr. Enrico Santi, for his guidance, patience and support throughout my doctoral study. His support and guidance were invaluable and essential to my success.

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Since its inception, power electronics has been to a large extent driven by the available power semiconductor devices. Switching power converter topologies, modes of operation, switching frequencies, passive filtering elements are chosen based on the switching and conduction characteristics of power semiconductor devices. In recent times new wide bandgap power semiconductor devices, such as SiC MOSFETs, are emerging with superior performance as compared to conventional silicon devices.

In switching power converter design, power losses of the power semiconductor devices play a crucial role in determining the physical characteristics of power converter systems in terms of size, weight, efficiency and, ultimately, cost. Switching losses impose an upper limit to the switching frequency, which in turn determines passive filtering element sizes and dimensioning of the cooling system. An accurate power loss model of the power semiconductor devices is needed for switching power converter design and optimization and to quantify the system-level advantages of novel SiC devices compared to conventional silicon devices.

Since power semiconductor device performance plays a key role in power electronics applications, power electronics designers need circuit-oriented device models to simulate the in-circuit performance of power devices in different applications. The basic objective in device modeling is to obtain a predictive description of the current flow through the device as a function of the applied voltages and currents, environmental conditions, such as temperature and radiation, and physical characteristics, such as geometry, doping levels, and so on. In general, there is a trade-off between computational speed and model accuracy. The required accuracy and simulation time
are crucial factors considered by device model designers when making this tradeoff.

In this dissertation, the analysis and applications of wide bandgap power devices can be divided into two parts: development of analytical loss model for wide bandgap power devices, and development of wide bandgap power semiconductor device models.

In the first part, a simple and accurate analytical switching loss model for SiC power devices is developed. This model considers the device capacitances and the parasitic inductances in the circuit, which have a strong impact on switching losses. In addition, the reverse recovery effect of the body diode of SiC MOSFET is considered. The detailed analysis of turn-on and turn-off transitions is presented. The accuracy of the proposed model is validated by experimental results, and the accuracy of the proposed loss model and conventional piecewise linear loss model is compared. The proposed analytical loss model has several advantages: it gives insight into the switching process, showing how different parameters and parasitics affect switching waveforms and determine switching losses; it provides accurate and simple closed-form switching loss calculation; it is useful for optimization given the fast calculation speed and the absence of numerical convergence problems; all power device parameters can be derived from datasheets (but requires parasitics estimation); it includes MOSFET body diode reverse recovery; it provides piecewise linear estimate of actual switching waveforms.

In the second part, a simple and accurate circuit-simulator compact model for silicon carbide (SiC) MOSFET is proposed and validated under both static and switching conditions. A novel feature of the proposed model is that it takes into account the nonlinear parasitic capacitances of the device and parameter extraction requires only data from device manufacturer datasheet. A parameter extraction procedure is proposed. A simulation model is built in Pspice software tool. The PSpice simulation results are compared with datasheet results. The comparison shows good agreement between simulation and datasheet results for both static and dynamic characteris-
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CHAPTER 1

INTRODUCTION

1.1 SILICON CARBIDE DEVICES FOR POWER ELECTRONICS APPLICATIONS

Semiconductor technology has always been a driving force in the evaluation of power electronics. Until recently silicon-based power semiconductor devices have been widely used in the power electronics and power system applications. The performance of silicon-based devices has been improving over the last decades. However, as the needs and requirements for electric energy continuously grow, silicon (Si) devices are reaching their theoretical limits in performance due to the inherent physical limitations of Si material properties, which make them unsuitable for future demands, especially for high voltage, high temperature, high frequency, high efficiency and high-power density applications. For example, current Si insulated-gate bipolar transistors (IGBTs) are able to handle high voltage and high current; however, these devices have relatively slow switching speed, which reduces the efficiency and increases size and weight of the power electronics systems using these devices [1].

On the other hand, Si metal-oxide-semiconductor field effect transistors (MOSFETs), are well-suited for high-switching frequency applications up to MHz frequencies, however they suffer from relatively high on-state resistance as the blocking voltage increases which results in high conduction loss.

Moreover, the maximum operating temperature for silicon devices is around 150°C, which determines the thermal management system size and weight. For example, a
variety of applications in the aircraft or automotive industries require power conversion systems to operate at an ambient temperature above 200°C, far beyond Si material limits. Therefore, there is a prompt need to develop new power electronics devices for high temperature thermal environment or reduced cooling, high voltage and high efficiency systems.

The emerging silicon carbide (SiC) technology is the most promising solution to improve the performance of semiconductor devices, thanks to its superior material properties compared to Si [2, 3, 4, 5, 6, 7]. Excellent electrical properties of silicon carbide (SiC) material, such as wider bandgap, higher thermal conductivity, and higher critical breakdown electric field, make it a very attractive semiconductor material for power switching devices. Table 1.1 compares the physical properties of Si and 4H-SiC materials [8].

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>4H-SiC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap Energy</td>
<td>1.1</td>
<td>3.26</td>
<td>eV</td>
</tr>
<tr>
<td>Relative permittivity</td>
<td>11.8</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Critical electric field, $E_C$</td>
<td>300</td>
<td>2200</td>
<td>kV/cm</td>
</tr>
<tr>
<td>Electron saturated drift velocity</td>
<td>1.0</td>
<td>2.0</td>
<td>$\times 10^7$ cm/s</td>
</tr>
<tr>
<td>Electron mobility, $\mu_n$</td>
<td>1500</td>
<td>1000</td>
<td>$cm^2/V \cdot s$</td>
</tr>
<tr>
<td>Hole mobility, $\mu_h$</td>
<td>600</td>
<td>115</td>
<td>$cm^2/V \cdot s$</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.5</td>
<td>4.9</td>
<td>W/cm · K</td>
</tr>
</tbody>
</table>

As seen in Table 1.1, the band gap of SiC (3.26 eV) is approximately three times that of Si. A large bandgap results in lower leakage currents than Si, which allows the SiC-based devices to operate at much higher temperatures. The higher breakdown electric field of SiC, $2.2 \times 10^6 V/cm$, which is almost ten times larger than Si, makes it...
possible to design wide bandgap power devices with thinner and more highly-doped voltage-blocking layers, resulting in lower conduction losses.

Based on the Baliga’s figure of merit, the ideal specific on-resistance is given as Equation 1.1.

$$R_{on,sp(ideal)} = \frac{4V_{BR}^2}{\varepsilon_{SiC}H_nE_C^3}$$

(1.1)

This equation shows that specific on-resistance of a unipolar devices having breakdown voltage $V_{BR}$ is inversely proportional to the cube of critical breakdown electric field $E_C$ of the semiconductor material. Since the SiC critical breakdown electric field is almost 10 times more than Si, the ideal specific on-resistance of SiC is more than 250 times smaller than that of Si, when accounting for the lower electron mobility of SiC with respect to Si. As a result of that, a lower on-resistance and conduction loss for a given breakdown voltage is achievable.

The higher thermal conductivity of SiC, coupled with the large bandgap, allows high-temperature operation of SiC-based devices at temperatures easily exceeding 200°C [9, 10, 11]. Operation of Si at higher temperature is limited by doping concentration, since the intrinsic carrier concentration ($n_i(T)$) increases exponentially with temperature, when the intrinsic carrier concentration reaches the maximum limit ($n_i(T) > \max (N_a, N_d)$) in the structure, the structure becomes all intrinsic and the structures fail to behave as a semiconductor any longer. However, SiC not only have very fewer intrinsic carrier concentration compare to Si, but also has a wider band gap. It means that the energy required for an electron to jump from the valence band to the conduction band within the semiconductor is too large which enables SiC materials to operate at higher temperature (above 200°C). All of the above advantages make wide bandgap semiconductor devices an ideal substitution to Si-based devices in future high-voltage and high-power converter systems.

A significant amount of research and development activity has occurred over the past two decades in the development of SiC power devices. Therefore, high voltage
SiC unipolar power switches (from 600V to 1200V), such as JFETs and MOSFETs have become commercially available since 2011 from Cree (now Wolfspeed), Infineon and other manufacturers [12]. These SiC active power devices offer much lower on-state resistance per unit area than conventional Si MOSFETs with the same voltage rating and much faster switching speed than Si IGBTs and GTOs. The superior performance of SiC has also encouraged the commercialization of SiC Schottky diodes with blocking voltages from 600V up to 1200V by Cree, GeneSiC and other device manufacturers. These SiC Schottky diodes have ultra-fast switching speed and almost zero reverse recovery, compared with conventional Si p-i-n diodes.

1.2 RESEARCH MOTIVATIONS AND OBJECTIVES

The analysis and applications of wide bandgap power devices require a substantial research effort, including the development of circuit-oriented device models for wide bandgap power devices, and loss modeling of wide bandgap power devices. This dissertation contributes in two areas: 1. Development of analytical loss model for wide bandgap power devices. 2. Development of circuit-oriented wide bandgap power semiconductor device models.

1.2.1 Accurate Analytical Switching Loss Model for High Voltage SiC MOSFETs Includes Parasitics and Body Diode Reverse Recovery Effects

The switching converter design process is typically an optimization process based on a spreadsheet that estimates performance as a function of design parameter values within the design space. This parameter-based optimization process requires an accurate analytical loss model with closed-form equations that relate switching losses to system parameters.

Given the high switching speed of SiC MOSFETs, the effect of device parasitic
capacitances and parasitic inductances on switching losses is significant and must be considered [13, 14, 15, 16]. In early SiC MOSFET products the body diode could not be reliably used and separate antiparallel Schottky diodes were typically added, but in newer generation SiC MOSFETs the body diode can be used to provide bidirectional current capability. Note that the body diode is a bipolar device with a PiN structure and exhibits reverse recovery at turn-off, which causes increased switching loss [17].

SiC power MOSFETs have now become commercially available with voltage rating of 1.2 kV, and the maximum operating temperature of SiC power MOSFET products is 150°C - 200°C, partly due to limitations of their plastic packages rather than intrinsic device limitations. High junction temperature operation of SiC MOSFETs can lead to a smaller cooling system being required. Therefore, performance of SiC MOSFETs operating at high temperatures is of interest to power electronics engineers [18, 19, 20]. Therefore, we propose a novel analytical loss model for SiC MOSFETs. Novel features of the model are: modeling of the performance of body diode and of the effect of reverse recovery; inclusion of parasitic inductive elements and of device junction capacitances. The proposed model breaks up the switching process into several subintervals and develops analytical equations for each subinterval to calculate the switching loss.

1.2.2 Characterization and Modeling of a SiC MOSFET

Since power semiconductor devices play significant roles in power electronics applications, the power electronics designers need to evaluate the performance of the power devices in order to fully utilize the device capabilities. Therefore, compact, i.e., circuit-oriented power device models are needed to be used during the design process in circuit simulators such as PSpice, MATLAB Simulink, Saber and so on [21].

Developing accurate SiC device models able to predict the details of fast inductive switching waveforms is very challenging. A good device model for circuit design
should be able to predict static I-V characteristic with reasonable accuracy. Because of the important role of the built-in device parasitic capacitances in the device dynamic behavior, a device model should include an accurate model for all these parasitic capacitances. The model should be temperature dependent, which means that the model should capture temperature-dependent behavior over the entire temperature operating range of the switching converter applications. Also, the model should have as few parameters as needed to accurately capture device behavior including static and dynamic characteristics.

In the literature, the presented device models for SiC MOSFETs and Schottky diodes can be categorized in two major groups: 1) analytical models which uses the finite element solutions to obtain the model ([22, 23, 24]); and 2) circuit-simulator models which apply equation-based description of device behavior. Circuit-oriented models require much less time for simulation with acceptably accurate results compared to the analytical models which provide very high accuracy but require long simulation time and detailed information about device fabrication. Additionally, analytical models are often not compatible with detailed circuit simulation.

The goal of this work is to create a simple and accurate circuit-simulator compact device model to evaluate the SiC device performance and validate it under static and switching conditions. The proposed model predicts static I-V characteristic with proper accuracy. Due to the importance of built-in devices parasitic capacitances in dynamic behavior of the device, the proposed model includes these parasitic capacitances.

1.3 STATE OF THE ART IN RESEARCH

1.3.1 ANALYTICAL LOSS MODEL FOR SiC POWER DEVICES

Power losses in power semiconductor devices includes conduction loss and switching loss. The conduction loss can be estimated from the device static IV character-
istics and the procedure is relatively straight-forward. The switching loss not only depends on device parameters, but also on circuit parameters, such as gate drive characteristics, stray inductances and device parasitic capacitances. To estimate switching loss, the conventional analytical loss model treats power switch turn-on and turn-off current and voltage waveforms as piecewise linear.

Usage of the conventional loss model results in closed form equations that can be easily used to obtain device switching loss. However, this model does not consider parasitic elements from PCB layout and devices packages. Additionally, it does not consider the nonlinear nature of device capacitances. As a result, the loss calculation based on the piecewise linear loss model is not accurate and does not match experimental results very well, especially for high frequency switching operation. Therefore, the parasitic inductances and device nonlinear capacitances should be taken into account to improve the accuracy.

There are some publications that propose analytical loss models for Si MOSFETs. The effect of the nonlinearity characteristics of MOSFET capacitances is included in the proposed loss models in [13] and [14]. The parasitic inductances from PCB and device packages are also considered in the models. The main drawback of these models is their complexity. In [15], an analytical switching loss model is proposed for synchronous buck voltage regulators. The rise and fall times equations are given in the model. The model considers the impact of parasitic inductances, however, the model is originally developed for low voltage Si MOSFETs, not for high voltage SiC MOSFETs. In addition, the reverse recovery effect of the body diode of the SiC MOSFET is not included in the model.

1.3.2 Characterization and Modeling of a SiC MOSFET

SiC MOSFET simulation models are needed for power electronics system design. The models based on PSpice simulation can be divided into three categories: behav-
ioral model, semi-physics model and physics-based model [3].

The physics-based model is based on semiconductor physics and, is very accurate, but it is not suitable for power electronics circuit simulation due to the complexity and long simulation time [25, 26].

The semi-physics model is partly based on semiconductor physics, and some equations and sub-circuits are included in the model. The developed semiphysics models in [27] and [28] are based on the traditional Si MOSFET structure, combined with secondary sub-circuits, and are consequently simpler than physics-based model. On the other hand, traditional Si MOSFET model in PSpice has many parameters which are coupled with each other, therefore it is difficult to obtain accurate parameters to fit the characteristic curves of SiC MOSFET.

Behavioral model is based on behavioral equations of SiC MOSFET, and the information about the internal structure and physical parameters of SiC MOSFET is not necessary, therefore it is very suitable for power electronics circuit simulation. The commonly used method is using segmented equations to describe the static characteristics of SiC MOSFET. The behavioral model developed in [29] uses three equations, which represents the cutoff region, linear region and saturation region. But, the segmented equations are not continuously differentiable, which causes the behavioral model to suffer from simulation convergence problems [30].

1.4 CONTRIBUTIONS

There are two original contributions in this dissertation. First, a simple and accurate analytical loss model for SiC power devices is developed. This model considers device capacitances and the parasitic inductances in the circuit, which have a big impact on switching losses. In addition, the reverse recovery effect of the body diode of SiC MOSFET is considered. The detailed analyzed turn-on and turn-off transitions are presented. The accuracy of the proposed model is validated by many experimen-
tal results, and the accuracy of the proposed loss model and conventional piecewise linear loss model is compared.

Second, a simple and accurate circuit-simulator compact model for silicon carbide (SiC) is proposed and validated under both static and switching conditions. A novel feature of the proposed model is that it takes into account the nonlinear parasitic capacitances of the device and only device manufacture datasheet is required for the parameter extraction. A parameter extraction procedure is proposed. A simulation model is built in Pspice software tool, considering the parasitic elements associated with the PCB interconnections and other components (load resistor, load inductor and current shunt monitor). The PSpice simulation results are compared with datasheet results. The comparison shows good agreement between simulation and datasheet results for both static characterization and dynamic characterization.
Chapter 2

Accurate Analytical Switching Loss Model for High Voltage SiC MOSFETs Includes Parasitics and Body Diode Reverse Recovery Effects

In recent times, with the fast development of wide bandgap devices, considerable progress has been made in power electronics applications like electric vehicles, aircrafts, electric ships and so on [3, 31, 32, 33, 34]. These applications require high-switching-frequency and high temperature operation. SiC power MOSFET is one of the most promising active power switching devices for high-speed, low-loss power electronics applications. On-state resistance of the wide bandgap devices is much lower than that of their silicon counterparts for the same die area. In addition, wide bandgap devices have much lower device capacitances, which makes faster switching with lower losses possible in power converter applications. The total size of a given power converter is expected to be decreased by using the new power semiconductor devices due to higher switching frequency and reduced losses. However, this comes at the price of increased EMI issues due to faster switching which requires design improvements using novel EMI characterization methods [35].

Power losses in power semiconductor devices consist of conduction loss and switching loss. The conduction loss can be directly estimated from the device static IV characteristics. The switching loss depends not only on device parameters, but also on circuit parameters, such as gate drive current, stray inductances and device parasitic capacitances [36, 37, 38].
To estimate switching loss, the conventional analytical loss model treats the turn-on and turn-off current and voltage waveforms of the power switch as piecewise linear. This model is used as a benchmark to be compared with the proposed analytical loss model. The conventional loss model results in closed form equations that can be easily used for device switching loss calculation. However, the conventional loss model does not take into account parasitic elements from PCB layout and devices packages. Hence, this model does not accurately predict the switching device loss and does not match experimental results very well, especially for high frequency switching operation. Given the high switching speed of SiC MOSFETs, the effect of device parasitic capacitances and parasitic inductances on switching losses is significant and must be considered [13, 14, 15].

In early SiC MOSFET products the body diode could not be reliably used and separate antiparallel Schottky diodes were typically added, but in newer generation SiC MOSFETs the body diode can be used to provide bidirectional current capability. Note that the body diode is a bipolar device with a PiN structure and exhibits reverse recovery at turn-off, which causes increased switching loss [17]. Therefore, the effect of body diode reverse recovery on switching loss should be considered in the analytical loss model.

In this chapter, a simple and accurate analytical loss model for Silicon Carbide (SiC) power devices is proposed. A novel feature of this loss model is that it takes into account the package and PCB parasitic elements in the circuits, nonlinearity of device junction capacitance and reverse recovery effect. The proposed model breaks up the switching process into several subintervals and develops analytical equations for each subinterval to calculate the switching loss. Inductive turn-on and turn-off are thoroughly analyzed. A double pulse test-bench is built to experimentally characterize the inductive switching behavior of SiC MOSFETs at different junction temperatures. The analytical results are compared with experimental results. The
results show that the proposed loss model is more accurate than the conventional loss model to predict switching loss. Variations in switching behavior with junction temperatures are discussed based on switching waveforms and analytical equations.

2.1 PROPOSED ANALYTICAL LOSS MODEL

Power semiconductor device losses consist of two components: conduction loss and switching loss. The conduction loss calculation in power devices is usually straightforward. Device conduction loss is calculated from the static I-V characteristics. Therefore, switching loss calculation will be the main focus of the loss analysis in this chapter. The proposed model uses piecewise linear approximation of the power semiconductor device switching waveforms to estimate the switching power losses. This work is an extension of work presented in [39].

Fig. 2.1 shows the equivalent circuit for inductive switching of SiC MOSFETs in a phase leg configuration used to estimate the switching loss.

![Circuit with parasitic inductances and device capacitances](image)

Figure 2.1: Circuit with parasitic inductances and device capacitances
Switch S is the SiC MOSFET, D is the SiC MOSFET internal body diode. Index 1 refers to high-side SiC MOSFET S1 and index 2 refers to low-side SiC MOSFET S2. The input is a constant DC voltage source $V_{dc}$, and output is represented by a constant DC load current $I_o$. The gate signals of Switches S1 and S2 are assumed to commutate between $V_{dr-L}$ and $V_{dr-H}$, a slightly negative voltage at turn-off (-5V–2V) is applied to the gate, while a positive voltage (15V-20V) is used at turn-on. Considering the modest transconductance of SiC MOSFETs, the positive voltage is at least 18V to decrease conduction losses. $L_1$, $L_{d1}$, $L_{s1}$, $L_{d2}$, $L_{s2}$ and $L_2$ are lumped parasitic inductances extracted from device packages and PCB traces. Parasitic elements of the MOSFET considered in the model, are gate-source capacitance $C_{gs}$, gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$.

![Nonlinear capacitances](image)

**Figure 2.2:** Nonlinear capacitances $C_{gd}$ and $C_{ds}$ as a function of drain source voltage $V_{ds}$

The nonlinear capacitances, $C_{gd}$ and $C_{ds}$, are approximated with a two value piece-wise constant capacitance at low-bias voltage and at high-bias voltage, as shown in Fig. 2.2. When $V_{ds}$ is greater than $V_{gs-Vth}$, $C_{gd} = C_{gda}$ and $C_{ds} = C_{dsa}$. When $V_{ds}$ is equal to or less than $V_{gs-Vth}$, $C_{gd} = C_{gdb}$ and $C_{ds} = C_{dsb}$. $C_L$ is the load inductor equivalent parallel capacitance, and $R_L$ is the DC resistance of the load inductor.
Key waveforms during the switching transitions are shown in Fig 2.3. $V_{dr1}$ and $V_{dr2}$

Figure 2.3: Key waveforms of switching transitions in a phase leg configuration

are the gate driver output voltages, $V_{gs1}$ and $V_{gs2}$ are the gate-source voltages, $V_{ds1}$ and $V_{ds2}$ are the drain-source voltages, $I_{ds1}$ and $I_{ds2}$ are the drain currents, $I_{ch1}$ and $I_{ch2}$ are the SiC MOSFET channel currents. Without loss of generality, load current $I_o$ is assumed to be positive. In case of negative $I_o$ the roles of MOSFETs S1 and S2 are reversed. The switching waveforms of the power semiconductor devices can be divided into several time intervals based on their physical behavior. Derivations of
the loss model for the turn-on and turn off transitions are presented in the following.

2.1.1 MOSFET TURN-ON TRANSITION

The two MOSFETs are operated with complementary gate signals with a dead time during which both MOSFETs are off to prevent cross conduction. The switching transition starts at time \( t_0 \), when high side MOSFET S1 is on, and low side MOSFET S2 is off and its drain-source voltage is \( V_{dc} + V_{on} \), where \( V_{on} \) is the MOSFET S1 on-state voltage drop and \( V_{dc} \) is the input DC voltage. The entire load current \( I_o \) flows through the channel of MOSFET S1 from source to drain.

**Stage 1 \([t_0, t_1]\) diode current rise time:** At time \( t_0 \), high-side gate signal \( V_{dr1} \) commutates from \( V_{dr-H} \) to \( V_{dr-L} \). The gate-source voltage \( V_{gs1} \) of high side MOSFET S1 starts decreasing, and it reaches the MOSFET threshold voltage \( V_{th} \) at time \( t_1 \). The load current \( I_o \) is diverted from MOSFET channel to its body diode in this period. No switching loss is generated in this period.

**Stage 2 \([t_1, t_2]\) dead time period:** During this period, the body diode of MOSFET S1 is conducting the load current. No switching loss occurs, but there are additional conduction losses due to the body diode voltage drop. This is the deadtime period.

**Stage 3 \([t_2, t_3]\) turn-on delay time:** At time \( t_2 \), low-side gate signal \( V_{dr2} \) commutates from \( V_{dr-L} \) to \( V_{dr-H} \). The gate-source voltage \( V_{gs2} \) of low-side MOSFET S2 starts to increase, but the MOSFET remains in cutoff until the gate-source voltage reaches the MOSFET threshold voltage \( V_{th} \) at time \( t_3 \). The load current still flows through body diode D1. No switching loss is generated in this period. The effect of parasitic inductance \( L_{s2} \) in the circuit can be neglected because the drain current is still zero in this stage.

Gate source voltage is given by

\[
V_{gs}(t) = (V_{dr-H} - V_{dr-L})\left[1 - e^{-\frac{(t-t_0)}{\tau_{iss}}}\right] + V_{dr-L} \tag{2.1}
\]
where \( \tau_{iss} = R_g (C_{gs} + C_{gd2a}) \), \( C_{gd2a} \) is the gate-drain capacitance of switch S2 at high drain-source voltage, \( R_g \) is the gate resistance, \( V_{dr-H} \) is high level gate drive voltage and \( V_{dr-L} \) is low level gate drive voltage. This interval ends at time \( t_3 \), the instant when \( V_{gs}(t_3) = V_{th} \).

**Stage 4 [t3, t4] current rise time:** In this interval, low-side MOSFET gate-source voltage \( V_{gs2} \) exceeds \( V_{th} \), and the drain current \( I_{ds2} \) starts increasing from zero. The drain current is given by:

\[
I_{ds2}(t) = g_{fs} [V_{gs2}(t) - V_{th}] \tag{2.2}
\]

Where \( g_{fs} \) is the trans-conductance of the SiC MOSFET.

The load current \( I_o \) begins to transfer from body diode D1 to MOSFET S2. At time \( t_4 \), low-side MOSFET takes over the inductive load current \( I_o \) and the reverse recovery peak current \( I_{rrm} \) of high-side MOSFET’s body diode. The waveform in Fig. 2.6 is used to estimate \( I_{rrm} \). During this interval low-side MOSFET drain-source voltage is decreased as a result of parasitic inductance voltage drop, due to high \( di/dt \) in the circuit. At time \( t_4 \), drain-source voltage \( V_{ds2}(t_4) = V_r \).

The time duration of this period [t3, t4] is given by

\[
t_4 - t_3 = \frac{C_{iss}(V_{miller} - V_{th})}{I_{g2}} = \frac{(I_o + I_{rrm})C_{iss}}{g_{fs}I_{g2}} \tag{2.3}
\]

where input capacitance \( C_{iss} = C_{gs2} + C_{gd2a} \), \( I_o \) is the inductive load current, \( I_{rrm} \) is the reverse recovery peak current of body diode D1, \( L_{s2} \) is the common source inductance, and \( g_{fs} \) is the trans-conductance of SiC MOSFET.

The gate-source plateau voltage is given by

\[
V_{miller} = V_{th} + \frac{I_o + I_{rrm}}{g_{fs}} \tag{2.4}
\]

This expression is used to obtain the rightmost expression in 2.3.

\[
I_{g2} = \frac{V_{dr-H} - 0.5(V_{miller} + V_{th}) - L_{s2}di_{ds2}/dt}{R_g} \tag{2.5}
\]
\[
V_{dr-H} - 0.5(V_{\text{miller}} + V_{th}) - L_{s2}(I_o + I_{rrm})/(t_4 - t_3)
\]
\[
= \frac{R_g}{L_{s2}g_{fs}}\]

Where \(L_{s2}\) is the common source inductance, and \(R_g\) is the gate resistance.

Fig. 2.4 shows the equivalent MOSFET driving circuit, and the gate-source signal waveform is shown in Fig. 2.5. The average gate-source voltage is assumed to be \((V_{\text{miller}}+V_{th})/2\) in stage 4 \([t_3, t_4]\).

The time duration \(t_4-t_3\) is solved by using equations (2.3) and (2.5) as follows:

\[
t_4 - t_3 = \frac{(C_{iss}R_g + L_{s2}g_{fs})(I_o + I_{rrm})}{(V_{dr-H} - 0.5V_{th} - 0.5V_{\text{miller}})g_{fs}}\]  
(2.6)
Reverse recovery current $I_{rrm}$ as a function of reverse recovery charge $Q_{rr}$ is given by:

$$I_{rrm} = \sqrt{2Q_{rr} \frac{I_{rrm\text{-datasheet}}}{T_{rr\text{-datasheet}}}}$$

(2.7)

where $Q_{rr}$ is obtained by:

$$Q_{rr} = I_o \tau_{HL}$$

(2.8)

where $\tau_{HL}$ is the high-level life time and can be obtained by device datasheet information. Neglecting recombination in the drift region of the SiC MOSFET body diode, $\tau_{HL}$ is:

$$\tau_{HL} = \frac{Q_{rr\text{-datasheet}}}{I_{o\text{-datasheet}}}$$

(2.9)

where $Q_{rr\text{-datasheet}}$ and $I_{o\text{-datasheet}}$ are the reverse recovery charge and the load current from the device datasheet, respectively. The MOSFET drain-source voltage is reduced by the inductive voltage drop of the stray inductance in the main circuit loop $L_s$ ($= L_1+L_2+L_{d1}+L_{s1}+L_{d2}+L_{s2}$) and is obtained as follows

$$V_{ds2}(t) = V_{dc} + V_d - L_s \frac{di_{ds2}}{dt}$$

(2.10)

The drain-source voltage $V_{ds2}$ at time $t_4$ is given by:

$$V_{ds2}(t) = V_r = V_{dc} + V_d - L_s \frac{I_o + I_{rrm}}{t_4 - t_3}$$

(2.11)

The total switching energy loss during this period $[t_1, t_2]$ is:

$$E_{loss} = \int_{t_3}^{t_4} I_{ds}(t)V_{ds}(t)dt$$

(2.12)

$$= \frac{(I_o + I_{rrm})(V_{dc} + V_d)(t_4 - t_3)}{2} + \frac{(I_o + I_{rrm})(V_r - (V_{dc} + V_d))(t_4 - t_3)}{3}$$

replacing (2.11) into (2.12):

$$E_{loss} = \frac{(I_o + I_{rrm})(V_{dc} + V_d)(t_4 - t_3)}{2} + \frac{L_s(I_o + I_{rrm})^2}{3}$$

(2.13)
**Stage 5 [t4, t5] voltage fall time:** After its reverse recovery current reaches the peak value at time \( t_4 \), body diode D1 begins to block voltage, and the SiC MOSFET S2 goes into the ohmic region. \( C_{gd2b} \) is the gate-drain capacitance in ohmic region, and \( C_{ds2b} \) is the drain-source capacitance in the ohmic region. Therefore the drain-source voltage \( V_{ds2} \) of low side MOSFET S2 decreases from \( V_r \) to on-state voltage \( V_{on} \) in this period.

The average gate drive current \( I_{g2} \) in stage 5 \([t4, t5]\) is:

\[
I_{g2} = \frac{V_{dr-H} - V_{miller}}{R_g} \quad (2.14)
\]

The drain-source voltage \( V_{ds2} \) in stage 5 is decreased with a large slope \( dv/dt \), which is given by:

\[
\frac{dv_{ds2}}{dt} = \frac{-I_{g2}}{C_{gd2b}} = \frac{V_{on} - V_r}{t_5 - t_4} \quad (2.15)
\]

where gate drain capacitance \( C_{gd} = C_{gd2b} \).

By substituting (2.14) into (2.15), the time duration of this period \([t4, t5]\) is estimated as:

\[
t_5 - t_4 = \frac{C_{gd2b}R_g(V_r - V_{on})}{V_{dr-H} - V_{miller}} \quad (2.16)
\]

The total loss, including voltage-current overlap loss, is given by:

\[
E_{loss} = \int_{t_4}^{t_5} I_{ds}(t)V_{ds}(t)dt \quad (2.17)
\]

\[
= \frac{(t_5 - t_4)(V_r + V_{on})I_o}{2} + \frac{(V_r + V_{on})I_{rrm}T_{rr2}}{4}
\]

As shown in the Fig. 2.6, \( T_{rr2} \) is the time for the body diode reverse recovery current to decrease from the peak value \( I_{rrm} \) to zero and is given by

\[
T_{rr2} = T_{rr} - T_a \quad (2.18)
\]

Where \( T_{rr} \) is the total reverse recovery time and \( T_a \) is the time which the diode current reaches from zero to the peak reverse recovery current \( (I_{rrm}) \).
The reverse recovery time as a function of reverse recovery current is given by:

$$T_{rr} = \frac{2Q_{rr}}{I_{rrm}}$$  \hspace{1cm} (2.19)

where $Q_{rr}=I_o\tau_{HL}$.

Time duration $T_a$ is calculated by:

$$T_a = \frac{I_{rrm}}{I_o + I_{rrm}}(t_4 - t_3)$$  \hspace{1cm} (2.20)

By substituting (2.20b) and (2.20) into (2.18), the time duration of $T_{rr2}$ is estimated as:

$$T_{rr2} = \frac{2Q_{rr}}{I_{rrm}} - \frac{I_{rrm}}{I_o + I_{rrm}}(t_4 - t_3)$$  \hspace{1cm} (2.21)

**Stage 6 [t5, t6] MOSFET conduction time:** The gate-source voltage $V_{gs2}$ increases exponentially to $V_{dr-H}$. MOSFET S2 is on and conducts the entire load current $I_o$. This is the on-interval. No switching loss is generated in this period. The MOSFET conduction loss occurs in this time period.

### 2.1.2 MOSFET TURN-OFF TRANSITION

**Stage 7 [t6, t7] turn-off delay time:** The gate signal for low-side MOSFET S2 is set to $V_{dr-L}$ at time t6. The gate-source voltage $V_{gs2}$ drops to $V_{miller}$ at time t7. $V_{ds}$ will not increase until $V_{gs}$ decreases to $V_{miller}$. Input capacitance $C_{iss}$ is being
discharged through gate drive circuit. The gate source voltage $V_{gs}$ is given by:

$$V_{gs}(t) = (V_{dr_{-H}} - V_{dr_{-L}})e^{-\frac{(t-t_6)}{\tau_{iss}}} + V_{dr_{-L}} \tag{2.22}$$

where $\tau_{iss} = R_g(C_{gs} + C_{gd2b})$, $C_{gd2b}$ is the gate-drain capacitance at low drain-source voltage, and $R_g$ is the gate resistance. This interval ends at time $t_7$, when $V_{gs}(t_7)=V_{miller}$.

**Stage 8 [t7, t8] voltage rise time:** The MOSFET drain-source voltage $V_{ds2}$ increases in this period. The high-side MOSFET output capacitance $C_{ds1}$ is discharged by load current. The measured drain current $I_{ds2}$ is reduced from load current $I_o$ by the charging current flowing into capacitance $C_{ds1}$. The average gate drive current $I_{g2}$ in this time period is given by:

$$I_{g2} = \frac{V_{miller} - V_{dr_{-L}}}{R_g} \tag{2.23}$$

Where $V_{miller}$ is:

$$V_{miller} = V_{th} + \frac{I_o}{gfs} \tag{2.24}$$

The drain-source voltage slope is:

$$\frac{dt_{ds2}}{dt} = \frac{I_{g2}}{C_{gd}} = \frac{V_{dc} + V_d - V_{on}}{t_8 - t_7} \tag{2.25}$$

where gate-drain capacitance $C_{gd} = C_{gd2b}$. By substituting (2.23) into (2.25), the time duration of this period [t7, t8] is estimated as:

$$t_8 - t_7 = \frac{C_{gd2b}R_g(V_{dc} + V_d - V_{on})}{V_{miller} - V_{dr_{-L}}} \tag{2.26}$$

The switching energy loss during this period [t7, t8] is given by:

$$E_{loss} = \int_{t_7}^{t_8} I_{ds}(t)V_{ds}(t)dt \tag{2.27}$$

$$= \frac{(t_8 - t_7)(V_{dc} + V_d - V_{on})}{2} I_o - C_{ds1} \frac{(V_{dc} + V_d - V_{on})^2}{2}$$

**Stage 9 [t8, t9] current fall time:** After the body diode D1 becomes forward-biased at time $t_8$, the current begins diverting from low-side MOSFET S2 to body
diode D1 of high-side MOSFET S1. This interval ends when the drain current $I_{ds2}$ becomes zero and gate-source voltage $V_{gs2}$ reaches $V_{th}$. The MOSFET S2 suffers an extra voltage stress, because decreasing drain current introduces a voltage drop across the parasitic inductances.

The time duration of this period $[t_8, t_9]$ is given by:

$$t_9 - t_8 = \frac{C_{iss}(V_{th} - V_{miller})}{I_{g2}} = \frac{I_{ds2}C_{iss}}{g_fs I_{g2}}$$  \hspace{1cm} (2.28)

where MOSFET input capacitance $C_{iss} = C_{gs2} + C_{gd2a}$, $I_{g2}$ is the average gate drive current in stage 9, $C_{gd2a}$ is the gate-drain capacitance at high drain-source voltage.

The drain current of MOSFET S2 at the beginning of this stage is:

$$I_{ds2}(t_8) = I_o - C_{ds1a} \frac{V_{dc} + V_d - V_{on}}{t_8 - t_7}$$  \hspace{1cm} (2.29)

Fig. 2.7 shows the equivalent MOSFET drive circuit during stage 9.

![MOSFET gate driving equivalent circuit during stage 9](image)

Figure 2.7: MOSFET gate driving equivalent circuit during stage 9

The average gate drive current $I_{g2}$ in this period is:

$$I_{g2} = \frac{0.5(V_{miller} + V_{th}) - V_{dr-L} - Ls2di_{ds2}/dt}{R_g}$$  \hspace{1cm} (2.30)
\[
\frac{0.5(V_{\text{miller}} + V_{\text{th}}) - V_{\text{dr} - L} - L_{s2}I_{ds2}/(t_9 - t_8)}{R_g}
\]

where \(L_{s2}\) is the common source inductance value.

By substituting (2.29) into (2.30), the duration time \(t_9 - t_8\) is given by

\[
t_9 - t_8 = \frac{C_{iss}R_g + Ls2gfs}{(0.5V_{\text{miller}} + 0.5V_{\text{th}} - V_{\text{dr} - L})}(I_o - C_{ds2a} \frac{V_{dc} + V_d - V_{on}}{t_8 - t_7})
\]

(2.31)

The switching energy loss during this period \([t_8, t_9]\) is given by

\[
E_{\text{loss}} = \int_{t_8}^{t_9} I_{ds}(t)V_{ds}(t)dt
\]

(2.32)

\[
= \frac{(t_9 - t_8)(V_{dc} + V_d)}{2}(I_o - C_{ds2a} \frac{V_{dc} + V_d - V_{on}}{t_8 - t_7}) + \frac{L_s}{2} (I_o - C_{ds2a} \frac{V_{dc} + V_d - V_{on}}{t_8 - t_7})^2
\]

Stage 10 \([t_9, t_{10}]\) diode conduction time: The body diode D1 conducts the entire load current. This is the deadtime interval. No switching loss is generated.

Stage 11 \([t_{10}, t_{11}]\) turn-on delay time of S1: At time \(t_{10}\), high-side gate signal \(V_{dr1}\) commutates from \(V_{dr - L}\) to \(V_{dr - H}\). The gate-source voltage \(V_{gs1}\) increases to \(V_{th}\) at time \(t_{11}\).

Stage 12 \([t_{11}, t_{12}]\) current rise time of S1: When gate-source voltage \(V_{gs1}\) reaches \(V_{th}\), MOSFET channel current \(I_{ch1}\) begins to increase. The load current \(I_o\) begins to divert from body diode D1 to MOSFET S1. No switching loss occurs in this period.

2.2 EXPERIMENTAL VALIDATION OF THE ANALYTICAL LOSS MODEL

2.2.1 HARDWARE SETUP

In order to validate the analytical loss model, a printed circuit board (PCB) test-bench was built to conduct the inductive switching experiments with a phase-leg configuration as in Fig.2.1 using 1200V SiC MOSFET. PCB layout parasitic inductances were minimized during the design. Experimental setup for inductive switching test is shown in Fig. 2.8.
The test-bench includes two test sockets for SiC MOSFETs, a SiC MOSFET gate driver, input capacitors with very low ESL (equivalent series inductance), a load inductor, probetip- adapters, and a Pearson coil for drain current measurement. The MOSFET under test is a SiC MOSFET C2M0160120 from CREE Inc. rated at 1200V/19A. The gate driver IC IXDD609SI is from IXYS Corporation with 9A maximum source/sink drive current. The gate driver output voltage switches from -5V to 18V. Probe-tip-adapters are used to measure MOSFET’s gate-source voltage $V_{gs}$, and drain-source voltage $V_{ds}$. A Pearson coil (model 2878) with an analog bandwidth of 70MHz is used to measure the drain current $I_{ds}$. A 250µH ferrite-core inductor is used as the load inductor for inductive switching experiments. Lecroy 6100A, 1GHz oscilloscope with sampling rate of 5GS/s is used to measure the switching waveforms.

Double pulse tests are performed to study switching waveforms and energy losses. The inductive switching waveforms are measured with 800V DC input voltage, 10A load current and 47Ω gate resistance. The list of components and measuring instruments for switching experiment setup is shown in Table 2.1.
Table 2.1: List of components and measuring instruments for inductive switching experimental setups

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET</td>
<td>C2M0160120D</td>
</tr>
<tr>
<td>Gate Driver</td>
<td>IXDD609SI (maximum 9A source/sink drive current)</td>
</tr>
<tr>
<td>Load Inductor</td>
<td>250μH ferrite-core inductor</td>
</tr>
<tr>
<td>Current Measurement</td>
<td>Pearson coil(model 2878)</td>
</tr>
</tbody>
</table>

2.2.2 Parameter extraction

Device parameter values are extracted from manufacturer’s datasheets. The threshold voltage $V_{th}$ and MOSFET transconductance $g_{fs}$ are extracted from device transfer characteristics curve. Drain-source capacitances $C_{ds1}$ and $C_{ds2}$ are obtained from device output capacitance curve as a function of drain-source voltage. Reverse transfer capacitances $C_{gd1}$ and $C_{gd2}$ are extracted from device transfer capacitance curve as a function of drain-source voltage. Gate-source capacitances $C_{gs}$ is obtained from device input capacitance curve. Table 2.2 lists the extracted model parameter values for the analytical loss model.

2.2.3 Switching waveforms

Double pulse switching tests are performed to obtain switching waveforms. In this experiment the input voltage is 800V and the probe deskew is performed before the measurements to correctly measure the power loss. Fig. 2.9 and Fig. 2.10 show the turn-on and turn-off transient waveforms of the lower switch (drain-source voltage $V_{ds}$, and drain current $I_{ds}$) for inductive load switching at 800V input, 10A load current, and 47Ω gate resistance.

The switching stages of the proposed analytical model are identified in the figures
Table 2.2: Parameter values and parasitic element values

<table>
<thead>
<tr>
<th>Section</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Circuit</strong></td>
<td>Main loop parasitic inductance $L_{pcb}$</td>
<td>67nH</td>
</tr>
<tr>
<td></td>
<td>Common source parasitic inductance $L_s$</td>
<td>15.2nH</td>
</tr>
<tr>
<td></td>
<td>Load inductor equivalent capacitance $C_L$</td>
<td>64pF</td>
</tr>
<tr>
<td><strong>Gate Driver circuit</strong></td>
<td>High level gate drive $V_{dr-H}$</td>
<td>18V</td>
</tr>
<tr>
<td></td>
<td>Low level gate drive $V_{dr-L}$</td>
<td>-5V</td>
</tr>
<tr>
<td>SiC MOSFET C2M0160120D</td>
<td>Gate threshold voltage $V_{th}$</td>
<td>3.25V</td>
</tr>
<tr>
<td></td>
<td>Transconductance $g_{fs}$</td>
<td>1.5S</td>
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<tr>
<td></td>
<td>Gate-source device capacitance $C_{gs}$</td>
<td>580pF</td>
</tr>
<tr>
<td></td>
<td>Low level gate-drain device capacitance $C_{gd1}$</td>
<td>15.5pF</td>
</tr>
<tr>
<td></td>
<td>High level gate-drain device capacitance $C_{gd2}$</td>
<td>300pF</td>
</tr>
<tr>
<td></td>
<td>Low level drain-source device capacitance $C_{ds1}$</td>
<td>100pF</td>
</tr>
<tr>
<td></td>
<td>High level drain-source device capacitance $C_{ds2}$</td>
<td>700pF</td>
</tr>
<tr>
<td></td>
<td>Reverse recovery time $T_{rr-datasheet}$</td>
<td>23ns</td>
</tr>
<tr>
<td></td>
<td>Reverse recovery charge $Q_{rr-datasheet}$</td>
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</tr>
<tr>
<td></td>
<td>Reverse recovery current $I_{rrm-datasheet}$</td>
<td>9A</td>
</tr>
</tbody>
</table>

and should be compared with Fig. 2.3. In the turn-on transition, an overshoot of drain current $I_{ds}$ is observed in the period $[t3, t4]$, due to the SiC MOSFET reverse recovery current. Turn-off transition switching waveforms are shown in Fig. 2.10. As seen in the figure, the gate-source voltage $V_{gs}$ drops to threshold voltage $V_{th}$ only when the drain current $I_{ds}$ decreases to zero at time $t9$. This matches the model waveforms of Fig. 2.3. The piecewise-linear switching waveforms predicted by the proposed analytical model are plotted and compared with the experimental waveform for turn-on transition in Fig. 2.11 and turn-off transition in Fig. 2.12 when the load current is 10A and gate resistance is 47Ω.

It is remarkable that the proposed analytical loss model based on closed-form equations provides reasonably accurate prediction of actual time-domain switching
waveforms. Some small mismatch in the waveforms is probably caused by some simplifying assumption, such as constant MOSFET transconductance $g_{fs}$ and two-value step-wise approximation of nonlinear capacitances $C_{gd}$ and $C_{ds}$.

Fig. 2.13 shows the device measured turn-on switching energy, turn-off switching energy and total switching energy, as a function of load current $I_o$, when the gate
Figure 2.11: Comparison between measured (solid lines) and analytical (dashed lines) waveforms for (a) $I_{ds}$ and $V_{ds}$ (b) $V_{gs}$ and $V_{ds}$ at turn-on transition (10 A load current, 47Ω gate resistance)

Resistance is 47Ω. The DC input voltage $V_{dc}$ is 800V in experimental measurements. As the load current increases, the turn-on switching energy and turn-off switching energy increase as well. However, turn-off energy loss does not increase as fast as the turn-on switching energy loss, due to lower increase of turn-off time at a higher load current.

This can be seen in Fig. 2.14, showing the device turn-on and turn-off times as a function of load current, when gate resistance is 47Ω. Both turn-on and turn-off times increase with load current, but turn-off time shows only a modest increase.

Fig. 2.15 shows the measured losses (solid line) in experiments as a function of load current compared to model predicted losses (dash line). Good agreement is achieved between the losses calculated by the proposed model and the simulated losses at
Figure 2.12: Comparison between measured (solid lines) and analytical (dashed lines) waveforms for (a) $I_{ds}$ and $V_{ds}$ (b) $V_{gs}$ and $V_{ds}$ at turn-off transition (10 A load current, 47Ω gate resistance)

different load current levels.

The measured device switching times (solid lines) in experiments as a function of load current are compared to model predicted times (dash line) in Fig. 2.16. Good agreement is achieved between the calculated switching times from the proposed model and the measured times.

In Fig. 2.17, the device turn-on, turn-off and total switching loss energies are shown as a function of the gate resistance at 10A load current. As seen, the switching loss energy varies approximately linearly with gate resistance. With increasing gate resistance, the switching loss energy increases due to slower switching transition (both voltage and current rates).

Fig. 2.18 shows the device total turn-on and turn-off times as a function of gate
The experiments measured losses (solid line) are compared to model predicted losses (dashed line) as a function of gate resistance in Fig. 2.19. Good agreement is achieved between the losses calculated by the proposed model and the measured losses.

Switching losses (Eq. 2.13) during the current transfer interval \([t_3, t_4]\) are strongly
affected by the duration (Eq. 2.6) of this time interval. Equation (2.6) shows the dependence of this time duration on the gate drive circuit ($C_{iss}R_g$ term) and on the parasitic source inductance ($L_{s2}g_{fs}$ term). It can be said that inductance $L_{s2}$ introduces a negative feedback from MOSFET current to the gate driver voltage that slows down both MOSFET turn-on and MOSFET turn-off, increasing losses. Considering this inductive effect is particularly critical for SiC high-voltage devices given the high di/dt during switching. A similar phenomenon occurs at turn-off, see
equation 2.31. Also, switching losses (Eq. 2.17) during the reverse recovery interval \([t4, t5]\) are affected by reverse recovery time duration and reverse recovery current (\(T_{rr}I_{rrm}\) term).

Fig. 2.20 compares the reverse recovery current and time as a function of load current between the analytical loss model and experimental results. There is a good matching between the reverse recovery current and reverse recovery time calculated using analytical loss model and obtained from the experiment. This shows that good
matching can be obtained using the proposed model with all parameters extracted from device datasheet.

At this point a comparison between the proposed model and the conventional loss model is performed. The switching loss energy calculated by proposed model for various load current is compared with the switching loss energy obtained by conventional loss model and switching loss energy obtained by experiment. The comparison is shown in Fig. 2.21. The gate resistance is 47Ω.

As pointed out, the conventional loss model does not take into account the parasitic inductances and device nonlinear capacitances and the predicted switching loss has significant errors in all cases. As the load current increases, the error in calculated switching loss energy by conventional loss model increases because it neglects the effect of the parasitic inductances. At load current $I_o=15A$, the measured switching loss is $1783.9\mu J$, while the predicted switching loss based on conventional loss model is only $1221.842\mu J$.

In Fig. 2.22, the same comparison of SiC MOSFET switching losses is shown for various gate resistance, when the load current is 10A. Similarly, the conventional loss
Figure 2.20: Comparison between measured (solid lines) and analytical (dashed lines) (a) reverse recovery current (b) reverse recovery time as a function of load current

model consistently underestimates switching losses. The relative error decreases as the gate resistance increases. This is due to the fact that a larger gate resistance slows down switching transitions, increasing losses but reducing the impact of parasitic inductances..
2.2.4 IMPACT OF HIGH TEMPERATURE ON REVERSE RECOVERY OF SiC MOSFET BODY DIODE

In order to study the body diode of SiC MOSFET switching behavior at high temperatures, double pulse switching tests are carried out at 10A load current and 800V input voltage. Fig. 2.23 shows the experimental lower MOSFET drain current
at turn-on at different temperatures. The current overshoot is due to the upper body diode reverse recovery current, which increases with temperature.

![Graph showing temperature dependency of reverse recovery of SiC MOSFET body diode](image)

Figure 2.23: Temperature dependency of reverse recovery of SiC MOSFET body diode

Elevated temperature increases the stored charge within the drift region and carrier lifetime which prolong the reverse recovery time. Increasing peak reverse recovery current ($I_{rrm}$) occurs due to the increasing stored charge in the drift region of the body diode. Equation (2.17) shows that resulting increase in the reverse recovery time and reverse recovery current increases the power loss. Fig. 2.24 shows the device measured turn-on switching energy $E_{on}$, turn-off switching energy $E_{off}$ and total switching energy, as a function of junction temperature.

### 2.2.5 EFFECT OF PARASITIC INDUCTANCES ON SWITCHING LOSSES

One of the main advantages of the proposed analytical loss model is that it captures the different effect on switching losses of two types of parasitic inductances: the main loop parasitic inductance $L_s$ and common source inductance $L_{S2}$. Fig. 2.25 shows the calculated turn-on and turn-off switching loss energies with different main loop inductances ($L_s$) for inductive load switching at 800V input, 10A load current, and
Figure 2.24: Switching loss energies v.s. SiC MOSFET junction temperature

47Ω gate resistance.

Figure 2.25: Turn-on and turn-off switching energy losses as a function of main loop parasitic inductance

The turn-on switching loss energy decreases when the main loop parasitic inductance increases, since the inductive voltage drop of $V_{ds}$ in period $[t3, t4]$ increases. This reduces the voltage-current overlap, which causes the loss. The turn-off loss slightly increases with the increase of $L_s$, mainly because of a larger voltage overshoot of $V_{ds}$ and a slower decrease of $I_{ds}$ in period $[t8, t9]$. The effect of $L_s$ can
be explained as a turn-on snubber, decreasing turn-on losses but increasing turn-off losses.

Fig. 2.26 shows the calculated turn-on and turn-off switching loss energies with different common source inductances \( L_{s2} \) for inductive load switching at 800V input, 10A load current, and 47\( \Omega \) gate resistance. Both turn-on and turn-off switching loss energies increase with the increase of \( L_{s2} \), due to the smaller rate of change of \( I_{ds} \) and longer duration in periods \([t3, t4]\) and \([t8, t9]\). It can be said that inductance \( L_{s2} \) introduces a negative feedback from MOSFET current to the gate driver voltage that slows down both MOSFET turn-on and MOSFET turn-off, increasing losses.

Figure 2.26: Turn-on and turn-off switching energy losses as a function of common source parasitic inductance

2.3 SUMMARY

A simple and accurate analytical switching loss model for SiC MOSFETs in a phase leg configuration is developed. This model considers device capacitances and parasitic inductances in the circuit, and the body diode reverse recovery, which significantly affect switching losses. The turn-on and turn-off transitions are divided in subintervals and analytical equations are derived for each subinterval. The accuracy
of the proposed analytical loss model is validated by comparison with experimental re-
sulted switching waveforms and of the actual time-domain switching waveforms. The
difference between real switching losses and measured switching losses is discussed,
and the influence of the parasitic inductances on switching losses is demonstrated.
Chapter 3

Characterization and Modeling of a

SiC MOSFET

3.1 POWER MOSFETs

Power semiconductor device development has always been a driving force for power electronics systems. Silicon-based power devices have dominated the power electronics applications for a long time. As the requirements for electric energy continuously grow, silicon (Si) devices are coming to face some fundamental limits in performance due to the inherent limitations of Si material properties, which make them unsuitable for future demands, especially in high-voltage, high frequency, high-efficiency, and high-power-density applications. As an example, currently Si insulated-gate bipolar transistors (IGBTs) are able to handle high voltage over 5 kV and high current over 1000 A, however the bipolar nature of the device limits the switching frequency of converter systems below 100 kHz and hence the efficiency of the system [1]. On the other hand, Si metal-oxide-semiconductor field effect transistors (MOSFETs), despite their high-switching-frequency capability in applications up to MHz, suffer from relatively high on-state resistance and hence high conduction loss at higher blocking voltage, which effectively restricts their use to low voltage applications less than 600 V. In addition, the general 150°C limit of maximum junction temperature further constrains the use of Si devices in high-temperature and high-power-density situations.

The emerging silicon carbide (SiC) technology with its superior material properties compared to Si, brings solutions to all the above problems. As a wide bandgap
material, SiC offers a critical electric field of $2.2 \times 10^6 V/cm$, an order of magnitude higher than Si. This increases the voltage blocking capability of SiC power devices and allows them to be fabricated with much thinner and higher doped drift layers. As a result, the on-state resistance and conduction loss reduce significantly. The high thermal conductivity of SiC improves heat dissipation and, together with the wide bandgap energy (3.3 eV), allows high-temperature operation above 300°C. All of the above advantages of SiC material make it an attractive alternative to Si in the future for high voltage, high power, high frequency, high temperature, and high efficiency converter systems [5, 6, 40, 7]. Table 3.1 lists important material properties of Si and SiC [5].

Table 3.1: Comparison of Si and SiC material properties

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>4H-SiC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap Energy</td>
<td>1.1</td>
<td>3.3</td>
<td>eV</td>
</tr>
<tr>
<td>Critical electric field</td>
<td>0.3</td>
<td>2.0</td>
<td>MV/cm</td>
</tr>
<tr>
<td>Relative permittivity</td>
<td>11.8</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>Electron saturated drift velocity</td>
<td>1.0</td>
<td>2.0</td>
<td>$\times 10^7 cm/s$</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>1.5</td>
<td>4.9</td>
<td>W/cm.K</td>
</tr>
</tbody>
</table>

The lower on-resistance makes SiC power MOSFETs an attractive choice in high power applications, offering similar conduction loss as Si IGBTs while operating at a much higher switching frequency [41, 42, 43, 44]. Due to lower device capacitance of SiC power MOSFET, for the similar voltage and current ratings, the switching loss of a SiC power MOSFET is much lower than Si IGBT or Si GTO. In inductive hard switching, SiC MOSFET body diode can be used if no external anti-parallel diode is connected [45].

Power MOSFET was the first commercially successful unipolar device developed using silicon material, after improving the metal oxide semiconductor interface for CMOS technology. Power MOSFET operation is dependent on the conductive channel formation at the surface of the semiconductor under the gate oxide layer [46].
Based on the gate structure there are several kinds of vertical power MOSFET, including VMOSFET for the V-shaped gate region, DMOSFET for the planar double-diffusion technology of the gate and UMOSFET for the U-groove gate structure. As an example the power DMOSFET structure is shown in Fig 3.1. Blocking capability of the MOSFET is determined by the thickness and doping concentration of drift region. Lower doping concentration results in higher blocking voltage but leads to higher on-resistance.

![Figure 3.1: Power DMOSFET structure](image)

As seen in the structure of Fig. 3.1, there is a parasitic NPN bipolar transistor in the MOSFET structure. This NPN transistor is a parasitic BJT and should be kept off in all operating modes of the MOSFET, otherwise it could lead to device latch-up and loss of gate control. To keep the BJT off, the P-base region is shorted to the source contact through the P+ region. As shown in the Fig. 3.1, this creates a P-N junction connecting the source region to the drain region, called built-in body diode.
of the MOSFET.

3.1.1 STATIC I-V CHARACTERISTICS

When the gate-to-source voltage is sufficiently positive, a conductive electron channel is formed at the surface of the semiconductor under the gate as shown in Fig. 3.1. This channel creates an electron current flow path between drain and source. The on-resistance during conduction is determined by the total resistance of the current path, which includes the resistances of the N+ region connected to the source, of the channel, of the JFET region, of the N- drift region and of the N+ substrate. Usually the resistances in the N+ substrate and the N+ region that is connected to the source can be neglected since the doping concentration is high in these regions. Since the on-resistance determines the current capability of the device, it is a very important parameter in the MOSFET [46]. The on-resistance can be extracted from the slope of the I-V characteristics in the linear region at low voltage.

As shown in the Fig. 3.2, when drain-source voltage $V_{ds}$ increases to a certain value, the drain-source current $I_{ds}$ saturates and the device operates in the so-called saturation region.

![Figure 3.2: I-V Characteristics of Power MOSFET](image-url)
In the saturation region device losses are high, because voltage and current are both high at the same time. In switching applications, if the power MOSFET is working as a switch, it is necessary to avoid the device operating in the saturation region due to high power dissipation.

Power MOSFET has blocking voltage capability and can support a large drain-to-source voltage $V_{ds}$ across the P-base/ N-drift region junction when the gate-source voltage $V_{gs}$ is zero or negative, with a small leakage current going through the device. As seen in Fig. 3.1, during turn-off transition, the depletion layer extends out from the P-base/ N-drift region junction to support the applied drain-to-source voltage. Extension of the depletion layer during turn-off transition of power MOSFET for both low and high drain-to-source voltage $V_{ds}$ is shown in Fig. 3.3. The blocking capability of power MOSFET is limited not only by the thickness of the devices and the doping concentration of N-drift region, but also by the structure inside the device, for example by the P-well spacing.

![Figure 3.3: Extension of depletion layer of a power MOSFET](image-url)
According to the superior material properties of SiC compared with Si, the breakdown voltage of SiC can get almost 100 times larger than breakdown voltage of Si for the same doping concentration since SiC has almost 10 times larger critical breakdown electric field than Si. Equation 3.1 express the relationship between breakdown voltage and breakdown electric field.

$$V_{BR} = \frac{\varepsilon_{SiC} E_{C}^2}{2q.N_D}$$ (3.1)

3.1.2 Dynamic characteristics

There are three main parasitic capacitances in power MOSFET, which are the gate-source capacitance $C_{gs}$, the gate-drain capacitance $C_{gd}$ and the drain-source capacitance $C_{ds}$. These capacitances are shown in Fig. 3.4.

![Device parasitic capacitances of power MOSFET](image)

Figure 3.4: Device parasitic capacitances of power MOSFET

In order to accurately model the dynamic behavior of the power MOSFET, the parasitic capacitances should be modeled accurately, especially the modeling of the gate-to-drain capacitance ($C_{gd}$), which affects the output switching waveforms due to the “Miller” effect. The dynamic characteristics of power MOSFET is generally dominated by the charging and discharging of the input capacitance seen from the

45
controlling gate terminal. During the switching transient, due to Miller effect, the equivalent input capacitance of the MOSFET will be the gate-source capacitance $C_{gs}$ in parallel with the amplified value of gate-drain capacitance $C_{gd}$ ($C_{iss} = C_{gs} + C_{gd}$). Usually, there are two methods to improve the switching speed of the power MOSFET. One is decreasing the gate resistance $R_G$, the other one is reducing the input capacitances $C_{gs}$ and $C_{gd}$. Reducing the gate-source capacitance decreases the charging and discharging time of the MOSFET and minimizing the gate-drain capacitance $C_{gd}$ decreases the Miller effect and as a result, the switching time can be faster. Fig. 3.5 shows the C-V characteristics of a power MOSFET [47].

![Figure 3.5: C-V characteristic of a power MOSFET](image)

As seen in the figure the gate-source capacitance $C_{gs}$ is almost constant with increasing drain-source bias. But the gate-drain capacitance $C_{gd}$ (same as $C_{rss}$) decreases with increasing drain-source voltage. One can see that this Miller capacitance increases abruptly at low voltage, which affects the dynamic behavior of the MOSFET during switching time. Hence, in order to develop an accurate model for power MOSFET, it is very important to consider the non-linear gate-drain capacitance $C_{gd}$. 

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3.2 SIC POWER MOSFET MODEL

Silicon power MOSFET has been suitable device for low voltage switching converter applications due to low on-resistance and fast switching speed. For higher voltage applications, silicon MOSFETs becomes impractical due to the very large on-resistance. Superior electrical properties of silicon carbide (SiC) material make it a very attractive semiconductor material for power switching devices. Specially, 4H-SiC MOSFET is one of the most promising devices for high-speed and low-loss power switching applications.

SiC MOSFETs have become commercially available since 2011 from Cree, Infineon and other manufacturers [12]. So, it is necessary to develop accurate models for SiC power devices to evaluate the performance of SiC devices in different applications and guide the switching converter designs.

Therefore, compact power device models are needed to be used during the design process in circuit simulators such as PSpice, MATLAB Simulink, Saber and so on [21]. Developing accurate SiC device models able to predict the details of fast inductive switching waveforms is very challenging. The goal of this work is to create a simple and accurate circuit-simulator compact device model to evaluate the SiC devices performance and validate it under static and switching conditions. The proposed model predicts static I-V characteristic with proper accuracy. Due to the important effect of built-in device parasitic capacitances on the dynamic behavior of the device, the proposed model includes these parasitic capacitances. The proposed model will be validated by comparison with simulation waveforms.

3.2.1 LITERATURE REVIEW OF SIC MOSFET MODELING

Many models have been proposed in the literature to predict the static and dynamic characteristics of Si and SiC power MOSFETs to support the development process of SiC-based converters and evaluate their performance [27, 48, 49, 50, 51,
52, 23, 53, 25, 54]. The device models can be divided in two main groups: 1) analytical models; and 2) circuit-oriented models which utilize equation-based description of device behavior. There is extensive literature describing analytical models for SiC MOSFET [26, 55, 56], but there are few publications about the implementation of circuit-oriented models in simulators such as PSpice [53, 27].

The circuit-oriented models can be divided in two main categories: behavioral models and physics-based models. In behavioral models a mathematical fitting of the device characteristics is performed, which results in simple equations and fast simulation time. The drawback is that behavioral models tend to work well only for the operating conditions under which the curve fitting was performed and may not work well under all conditions. On the other hand, physics-based models include the physical properties the device, and often utilize more complex numerical methods such as finite-element analysis. A physics-based model can estimate in a satisfactory level of detail of the MOSFET’s performance, if the parameters are correctly identified.

In [26], the physics-based numerical model is based on the drift diffusion equations and accounts for incomplete ionization and charging and discharging of interface states. This model can capture the effects of surface phenomena, but it is very complex and requires long simulation times, which make the model unsuitable for circuit simulator implementation. A simple SPICE behavioral model for SiC power DMOSFETs is presented in [27]. The model is obtained by modifying the conventional level-1 Si power MOSFET model available in commercial SPICE simulators. The models requires several fitting factors to be extracted from device characteristics to obtain good matching.

Behavioral model is based on mathematical equations to describe the behavior of SiC MOSFET, and the information about the physical structure and physical parameters of SiC MOSFET is not necessary, therefore it is very suitable for power electronics circuit simulation. The general method to describe the static character-
istics of Si MOSFET, is to use three equations, which represents the cutoff region, linear region and saturation region, respectively. Behavioral models typically use this three-region description. However, these equations are not suitable for SiC MOSFET modeling, since due to the lower transconductance of SiC MOSFETs compare to Si MOSFETs, the statics characteristics of SiC MOSFET have more smooth transition between the regions. Hence, the conventional behavioral model, which utilizes the modified level-1 Si power MOSFET to model the SiC power MOSFET, suffers from the simulation convergence problem [30]. In order to improve the simulation convergence, the proposed model describe a new behavioral model with smooth continuous equations [57].

3.2.2 Simulation Model of SiC Mosfet

The proposed circuit simulator compact SiC model is shown in Fig. 3.6. The model consists of a voltage-dependent current source $I_{ds}$, gate-drain voltage-dependent capacitance $C_{gd}$, drain-source voltage dependent capacitance $C_{ds}$, gate-source constant capacitance $C_{gs}$. The voltage-dependent current source $I_{ds}$ is used to describe the static characteristic of SiC MOSFET.

The dynamic behavior is strongly affected by the parasitic device capacitances. The internal gate resistance $R_g$ and drain and source contact resistances $R_d$ and $R_s$ are included.

3.2.3 Voltage dependent current source $I_{ds}$

In conventional models, $I_{ds}$ uses separate equations for the cutoff region, linear region, and saturation region. But for SiC MOSFET, it is difficult to accurately determine the boundary drain–source voltage $V_{ds}$ between linear region and saturation region, and dividing $I_{ds}$ description into several regions may cause convergence problems when the model used in power electronics circuit simulations. Based on this,
the proposed method uses fitting method with smooth continuous equations to define $I_{ds}$.

The voltage-dependent current source $I_{ds}$ models the SiC MOSFET’s static I-V characteristic, and comprises both output characteristic and transfer characteristic equations. The transfer characteristic equation is a function of gate-source voltage $V_{gs}$, and the output characteristic equation is a function of both gate-source voltage $V_{gs}$ and drain-source voltage $V_{ds}$.

The transfer characteristic curve of SiC MOSFET is fitted by the voltage-dependent current source $I_{ds}$ equation. The proposed equation for transfer characteristic is given by

$$I_{ds1} = K_1 \cdot \ln[1 + \exp\left(\frac{V_{gs} - b_1}{c_1}\right)]$$  \hspace{1cm} (3.2)

where $K_1$, $b_1$ and $c_1$ are the fitting parameters of the transfer characteristic.

For the fitting of the datasheet output characteristic, the output characteristic equation is function of both the gate-source voltage $V_{gs}$ and drain-source voltage $V_{ds}$. 

Figure 3.6: Structure of the SiC model
For the output characteristic, the characteristic curves under different gate-source voltage $V_{gs}$ are fitted. Then the output characteristic parameters are fitted with the drain-source voltage $V_{ds}$ as variable. The output characteristic equation can be expressed in:

$$I_{ds2} = \frac{\{K_2 \cdot e^{a_1(V_{gs} - V_{th})} + b_2\} \cdot V_{ds}}{1 + \{K_3 \cdot e^{a_2(V_{gs} - V_{th})} + b_3\} \cdot V_{ds}}$$ \hspace{1cm} (3.3)$$

where $K_2$, $a_1$, $b_2$, $K_3$, $a_2$ and $b_3$ are the fitting parameters of output characteristic. The voltage-dependent current source $I_{ds}$ is obtained by combination of the current equation resulted of transfer characteristic and the current equation resulted of output characteristics and is given by:

$$I_{ds} = I_{ds1} \cdot I_{ds2} = K \cdot \ln[1 + e^{(V_{gs} - b_1)/c_1}] \cdot \frac{\{K_2 \cdot e^{a_1(V_{gs} - V_{th})} + b_2\} \cdot V_{ds}}{1 + \{K_3 \cdot e^{a_2(V_{gs} - V_{th})} + b_3\} \cdot V_{ds}}$$ \hspace{1cm} (3.4)$$

where $K$ is the related fitting parameter and differs from $K_1$ and $K_2$. Note that if $V_{gs} < V_{th}$, the drain-source current is zero.

By fitting the transfer characteristic and output characteristic together, the related fitting parameters can be obtained. In section 3.2.5 the fitting process is demonstrated. According to the datasheet, the trend of the curves is basically the same at different temperatures, but the current values are different. The final static model equation with temperature dependence is given by:

$$I_{ds} = K(T) \cdot \ln[1 + e^{(V_{gs} - b_1)/c_1}] \cdot \frac{\{K_2 \cdot e^{a_1(V_{gs} - V_{th})} + b_2\} \cdot V_{ds}}{1 + P(T) \{K_3 \cdot e^{a_2(V_{gs} - V_{th})} + b_3\} \cdot V_{ds}}$$ \hspace{1cm} (3.5)$$

where

$$K(T) = K \cdot [1 - h_1 \cdot (T - 25)]$$ \hspace{1cm} (3.6)$$

and

$$P(T) = [1 - h_2 \cdot (T - 25)]$$ \hspace{1cm} (3.7)$$

where $h_1$, and $h_2$ are related fitting parameters of the temperature characteristic.
3.2.4 Dynamic Characteristic Model

The dynamic characteristic of SiC MOSFET is mainly determined by three inherent capacitances. The gate-source capacitance $C_{gs}$ is equivalent to the metal oxide capacitance of SiC MOSFET and is relatively independent of the applied voltage. Hence, a constant capacitance is used in the proposed model.

According to the C-V characteristic curves provided in SiC MOSFET datasheet, the capacitances $C_{gd}$ and $C_{ds}$ are nonlinear voltage dependent capacitances, so constant capacitances may not reflect accurate dynamic characteristic of SiC MOSFET. The proposed model for capacitance $C_{gd}$ is shown in Fig. 3.7. The constant linear capacitance $C_0$ is to generate current $i_{C0}$ which varies with the gate-drain voltage, $V_{gd}$, by means of the voltage-dependent voltage source $Q$. The equivalent current $i_{gd}$ describes the nonlinear capacitance $C_{gd}$ by means of the current-dependent current source [34, 58, 59]. So, the voltage-dependent capacitance $C_{gd}$ is depicted by the voltage-dependent current source. The constant capacitance $C_0$ is to realize the differential characteristic of the capacitance $C_{gd}$ and simplify the simulation [34].

![Figure 3.7: The proposed model of capacitance $C_{gd}$](image)

$$I_{gd} = \frac{i_0}{C_0}$$

current-dependent current source

$V_{gd}$

$+$

$-$

voltage-dependent voltage source

$i_0$

$C_0$
The modeling equations are developed as in:

\[
\begin{aligned}
Q(V) &= f(V_{gd}) \\
i &= \frac{dQ}{dt} \\
i_{gd} &= \frac{1}{C_0} i_0
\end{aligned}
\]

\[\Rightarrow \begin{aligned}
i &= \frac{df}{dV_{gd}} \cdot \frac{dV_{gd}}{dt} \\
i_{gd} &= \frac{1}{C_0} i_0
\end{aligned} \Rightarrow \begin{aligned}
C_{gd} &= \frac{df}{dV_{gd}} \tag{3.8}
\end{aligned}
\]

As shown in equation (3.8), the equation for \( Q \) is needed to develop the capacitance model. The equation of capacitance \( C_{gd} \) can be obtained by data extraction and fitting from the C-V characteristic. According to equation (3.8), it can be found that \( C_{gd} \) and \( Q \) have differential relationship.

\[Q = \int C_{gd} dV_{gd} \tag{3.9}\]

By using equations (3.8) and (3.9), \( C_{gd} \) and \( Q \) can be obtained as:

\[C_{gd} = \frac{p}{1 + e^{(q - V_{gd})/r}} + s \tag{3.10}\]

\[Q = f(V_{gd}) = p.r.ln[1 + e^{(V_{gd} - q)/r}] + s.V_{gd} \tag{3.11}\]

where \( p, q, r \) and \( s \) are the fitted parameters of the C-V characteristic.

The drain-source capacitance \( C_{ds} \) is also a nonlinear capacitance and can be modeled using the same approach described for \( C_{gd} \).

### 3.2.5 Parameter extraction

The parameters in proposed compact model are obtained by data extraction and equation fitting.

The parameter extraction method is shown in Fig. 3.8.

Using data extraction software, GetData, the characteristic curves in datasheet are converted to the required data. Then using MATLAB software, extracted data are fitted by I-V and C-V characteristic equations. The internal gate resistance \( R_g \) is given in datasheet but it is small compared to the external gate resistance which
is typically introduced to dampen transient oscillations during switching transients. Resistances $R_d$ and $R_s$ are assumed to be constant and represent the distributed nature of terminal contact mesh.

Table 3.2 lists the static model parameters valued for SiC MOSFET (C2M0160120D) at 25°C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$a_1$</th>
<th>$a_2$</th>
<th>$b_1$</th>
<th>$b_2$</th>
<th>$b_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>-0.253</td>
<td>0.00594</td>
<td>2.035</td>
<td>61.94</td>
<td>45.56</td>
</tr>
<tr>
<td>Parameter</td>
<td>$c_1$</td>
<td>$K$</td>
<td>$K_1$</td>
<td>$K_2$</td>
<td>$K_3$</td>
</tr>
<tr>
<td>Value</td>
<td>0.134</td>
<td>0.9981</td>
<td>33.7</td>
<td>-5.076</td>
<td>2.054</td>
</tr>
</tbody>
</table>

The fitted parameters in the temperature dependent output characteristic equations 3.6 and 3.7, are $h_1 = 4.474e^{-3}$ and $h_2 = 2.223e^{-3}$.

To extract the capacitance parameters, the datasheet provides input capacitance $C_{iss}$, the transfer capacitance $C_{rss}$, and output capacitance $C_{oss}$ curves, from which
the desired capacitances can be obtained as follow:

\[
\begin{align*}
C_{gs} &= C_{iss} - C_{rss} \\
C_{gd} &= C_{rss} \\
C_{ds} &= C_{oss} - C_{rss}
\end{align*}
\] (3.12)

Using the obtained data from 3.12, the parameters required for nonlinear capacitance model, are extracted using curve fitting and are shown in Table 3.3.

Table 3.3: Non-linear capacitances parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$p$</th>
<th>$q$</th>
<th>$r$</th>
<th>$s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gd}$</td>
<td>3.673e4</td>
<td>-30.96</td>
<td>-5.96</td>
<td>7.026</td>
</tr>
<tr>
<td>$C_{ds}$</td>
<td>387.3</td>
<td>-0.1878</td>
<td>145.8</td>
<td>-0.00402</td>
</tr>
</tbody>
</table>

3.2.6 Model Verification

To validate the proposed compact model, the simulation static characteristic and dynamic characteristic curves are compared with the device datasheet curves. The static characteristic curves in datasheet include the forward transfer characteristic and the forward output characteristic.

According to the parameters presented in Table 3.2, the proposed static model can be built in PSpice, and the curves can be obtained by dc sweep analysis. Fig. 3.9 compares the transfer characteristic between simulation curves (dashed lines) and datasheet curves (solid lines) curves, in forward conduction mode. The SiC MOSFET model used in simulation is from the manufacturer CREE Inc. The simulation curves are in good agreement with datasheet curves.

The comparison of datasheet output characteristic curve and simulation curve is shown in Fig. 3.10. The figure shows that the simulation curves are in good agreement
The temperature dependent static model can be built in PSpice, and the forward output characteristic curves at different temperatures can be obtained. Figs. 3.11 shows the comparisons between simulation (dashed lines) curves and datasheet (solid lines) curves under temperatures -55°C, and 150°C, for forward output characteristic.

The simulation curves are in good agreement with datasheet curves.

The intrinsic nonlinear capacitances determine the dynamic characteristic of a power MOSFET, so the intrinsic capacitance model must be verified by comparing the simulation curves with datasheet curves. The simulation curves can be obtained with the time domain transient in PSpice. Fig. 3.12 shows the gate–drain, drain–source capacitance comparisons between simulation (dashed lines) and datasheet (solid lines). The simulation curves are in good agreement with datasheet curves.
Furthermore, the dynamic characteristic includes the voltage and current changes of the power MOSFET under switching condition. In order to verify whether the dynamic characteristic of the proposed model under switching condition is correct, a double pulse simulation circuit is built as shown in Fig. 3.13.

In order to predict voltage and current transient slopes, overshoot and ringing, some circuit parasitic inductance are also included in simulation. The double pulse circuit parameters are shown in Table 3.4.

Table 3.4: Double pulse simulation circuit parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Input Voltage $V_{in}$ (V)</th>
<th>Load Current (A)</th>
<th>Inductive Load ($\mu H$)</th>
<th>Gate Resistance $R_g$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>500</td>
<td>10</td>
<td>250</td>
<td>20</td>
</tr>
</tbody>
</table>
The voltage and current simulation switching waveforms of the SiC MOSFET are shown in Fig. 3.14. The voltage and current switching waveforms during turn-on and turn-off transient are shown in Fig. 3.15 and Fig. 3.16.

The simulation results show that the proposed compact model can work properly in the double pulse circuit and can reflect the voltage and current changes of SiC MOSFET under switching condition.

3.3 SUMMARY

In this chapter, a simple and accurate circuit-simulator compact model for a SiC power MOSFET is developed. The model parameters can be easily extracted from device static I-V characteristics and C-V characteristics. This model considers the non-linearity of the device internal capacitances, which is a very important feature for circuit designers. A parameter extraction method is provided to allow easy extraction of model parameters using static I-V characteristics and C-V characteristics. A double pulse test-circuit simulation is built to test the switching behavior of SiC MOSFET model. In order to simulate the parasitic ringing during very fast switching transient, gate-source driving loop and drain-source main switching loop parasitic inductances are considered in the simulation. The extracted parameters are used with the SiC MOSFET device model for inductive hard switching simulations in Pspice. The static and dynamic characteristics of the proposed model were well verified based on the datasheet and double pulse simulation. The simulation results show that the proposed compact model can work properly in the double pulse circuit and can reflect the voltage and current changes of SiC MOSFET under switching condition.
Figure 3.11: Comparison between simulation (dashed line) and datasheet (solid line) for output characteristic at Forward transfer characteristic comparison between simulation (dashed line) and datasheet (solid line) at (a)-55°C (b) 150°C
Figure 3.12: Comparison between simulation (dashed line) and datasheet (solid line) (a) Gate–drain capacitance (b) drain–source capacitance as a function of drain-source voltage

Figure 3.13: The double pulse simulation circuit
Figure 3.14: The simulation waveforms of double pulse circuit

Figure 3.15: The simulation waveforms during turn-on transient

Figure 3.16: The simulation waveforms during turn-off transient
Chapter 4

CONCLUSION AND FUTURE WORK

4.1 CONCLUSION

This dissertation discusses the device modeling and loss analysis of wide bandgap power semiconductor devices. SiC power MOSFET is the wide bandgap power semiconductor device studied in this dissertation. The main objective in device modeling is to develop the functional relationship among the electrical and thermal parameters of the devices that are to be modeled. Closed form mathematical equations are used to develop Loss models to accurately describe power loss mechanisms and determine losses as a function of various design parameters.

First, a simple and accurate analytical loss model for SiC power devices is proposed. In order to evaluate the proposed analytical loss in more converter topologies, such as inverter, half bridges, full bridges and so on, the analytical loss model is investigated for a SiC MOSFET in a phase leg configuration.

A novel feature of this loss model is that the nonlinearity of device capacitances and the parasitic inductances in the circuit, such as the source inductance shared by the power stage and gate driver loop, the drain inductance, etc., are considered in the loss model. In addition, the model takes into account the reverse recovery characteristics of the body diode of the SiC MOSFET.

The proposed model identifies the switching waveform into subintervals, and develops the analytical equations for each switching subinterval to calculate the switching loss. Inductive switching for turn-on and turn-off transitions are analyzed in detail.
A double pulse test-bench is built to characterize inductive switching behavior of the SiC devices. The analytical results are compared with experimental results. The comparison results show that the proposed analytical loss model can calculate switching loss more accurately than the conventional loss model and provides reasonably accurate prediction of actual time-domain switching waveforms.

Impact of High Temperature on Reverse Recovery time and current of SiC MOSFET Body Diode is investigated. In order to study the body diode of SiC MOSFET switching behavior at high temperatures, double pulse switching tests are carried out.

Second, a circuit simulator compact model is proposed for SiC MOSFETs. To solve the simulation convergence problem of the SiC MOSFET model, continuous equations are developed to describe the static and dynamic characteristics. Further, the static characteristic of SiC MOSFET obtained by the proposed model is verified by comparing the simulation curves with the static curves provided in datasheet, and the dynamic characteristic is verified by comparing the time domain simulation of the proposed model with the double pulse simulation circuit. The accuracy and good convergence of the model provide a good way to research the power converters with SiC MOSFETs by simulation way.

A novel feature of the proposed model is that it takes into account the nonlinear parasitic capacitances of the device and only device manufacture datasheet is required for the parameter extraction. A curve fitting parameter extraction procedure is proposed. A simulation model is built in PSpice software tool, considering the parasitic elements associated with the PCB interconnections and other components (load resistor, load inductor and current shunt monitor). The PSpice simulation results are compared with datasheet results. The comparison shows good agreement between simulation and datasheet results for both static characterization and dynamic characterization.
4.2 FUTURE WORK

Based on the research results presented in this dissertation, future work can be accomplished as follows:

1) Experimental Resistive and inductive switching validation of the compact SiC power device model.

A PCB double pulse tester circuit will be built to verify the accuracy of the proposed SiC device model under switching conditions. Comparison between simulation results and experimental results will be done to evaluate the performance of the proposed SiC MOSFET compact model. Furthermore, the switching behavior will be correlated with static device characteristics commonly available from datasheet.

2) Resistive and inductive switching experiments at higher temperature.

The experiment temperature is limited by SiC devices package, which has much lower temperature range compared to SiC material and devices.

3) Improve the parasitic non-linear capacitances model of SiC MOSFET, which strongly affects the dynamic characteristics of SiC MOSFET.

4) Design of a SiC DC-DC synchronous buck converter

In order to reveal the SiC MOSFET performance and validate the proposed analytical loss model, a DC-DC synchronous buck converter design using 1200V SiC MOSFETs will be demonstrated. The efficiency of the power converter will be measured, and device temperature will be monitored during steady-state operation. The comparison of experiment, PSpice simulation, analytical loss model calculation will be done, in terms of device losses and converter efficiency.
BIBLIOGRAPHY


