High Quality Low Offcut 4h-Sic Epitaxy and Integrated Growth of Epitaxial Graphene for Hybrid Graphene/Sic Devices

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HIGH QUALITY LOW OFFCUT 4H-SiC EPITAXY AND INTEGRATED GROWTH OF EPITAXIAL GRAPHENE FOR HYBRID GRAPHENE/SiC DEVICES

by

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DEDICATION

To my beloved parents and brother.
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ABSTRACT

Power electronic semiconductor devices are critical components in next-generation power systems such as hybrid electric vehicles and smart grid power controls enabling reduction in system size, weight, and cost. Wide bandgap materials such as SiC, GaN, and diamond have been investigated to replace silicon, due to their superior material properties. Of these, 4H-SiC is considered the most viable candidate beyond 3kV due to its technological maturity, its wide band gap (3.23 eV), high breakdown field ($4 \times 10^6$ V/cm), high thermal conductivity (5 W/cm/K) and, more importantly, its indirect bandgap.

The main contribution of my research relates to the development and investigating the methods for growing high-quality SiC homoepitaxial layers with low defect density, particularly basal plane dislocations (BPDs) which severely affects the SiC bipolar device yield in high scale environments. The first approach of eliminating BPDs was to produce high quality SiC epilayers using a novel Si precursor Tetrafluorosilane (TFS) on nearly on-axis substrates (0.5° offcut) which inherently suppress BPD formation, by identifying a unique growth regime that promotes step flow growth in a nearly on-axis surface which is considered a major challenge in SiC epitaxy. As an alternate solution to BPD elimination in the most common 4º substrates, we developed a composite growth structure to produce 100% BPD free SiC epilayers over a wide range of C/Si ratios (1 to 1.8), introducing a minimal specific on-resistance of <0.5 mΩ-cm².
Final part of this work is integrating the high quality SiC epilayers for fabricating hybrid EG/SiC Schottky structures with epitaxial graphene as an in-situ high temperature metal contact grown using TFS under Argon ambience. The EG/SiC Schottky devices fabricated exhibited an excellent ideality of 1.1 and a barrier height of 0.85 eV. These EG/SiC Schottky devices were tested as photodetectors for sensing UV light owing to graphene’s transparent optical property and 4H-SiC bandgap which is in the range of UV spectrum.

With these contributions made towards increasing the material quality and yield of SiC and SiC-graphene devices, SiC can be envisioned as a versatile and reliable material for power electronics and harsh environment sensor applications in the near future.
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1.1 INTRODUCTION:

Power electronic semiconductor devices are critical components in next-generation energy-efficient power systems such as hybrid electric vehicles, smart grid power controls, and high voltage transmission circuitry enabling reduction in system size, weight, and performance. In the power electronics industry, SiC is setting new standards in high-performance electrical conductivity, high thermal conductivity, and power savings. The SiC market in the power electronics industry has widespread application areas ranging from hybrid vehicles, wind turbines, industrial data centers, medical imaging, renewable energy, oil and gas, and aerospace. Of these, 4H-SiC is considered the most viable candidate beyond 3kV due to its technological maturity, owing to the wide band gap (3.26 eV), high breakdown field (2×10^6 to 4×10^6 V/cm), high thermal conductivity (3 to 5 W/cm/K) and, more importantly, its indirect bandgap. This gives it much longer minority carrier recombination lifetimes of microseconds vs nanoseconds for direct bandgap materials such as GaN, making it the only practical wide bandgap for bipolar devices that require long carrier lifetimes for high current handling.

Despite these promising properties, SiC is not yet a popular material for device fabrication due to challenges in obtaining high quality single crystal materials. The high density of crystal defects especially micropipes, basal plane dislocations (BPDs) present
in bulk growth of SiC severely affect the material yield in high scale environments. Currently SiC wafer technology has shown tremendous improvement for producing high quality SiC single crystals in bulk as well as epitaxial growths with almost no micropipes (www.cree.com).

But the method for eliminating BPDs completely from the bulk material is still under investigation. Identification of the unique and promising properties of SiC have paved way for rapid increase in research to improve the material quality of SiC single crystals in bulk as well as epitaxial growths. The low lattice mismatch between SiC and GaN also makes SiC an excellent substrate for the growth of III-nitrides structures used in fabrication of blue LEDs and lasers (Gurnett & Adams, 2006; Krüger & Grundmüller, 2013). SiC and SiC based electronic devices fabricated from high quality SiC single crystals are expected to excel the performance of Si based power devices in the current market.

1.2 SiC PROPERTIES:

Wide bandgap materials such as SiC, GaN, and diamond have been investigated to replace the industry workhorse, silicon, due to their superior material properties (Table 1.1). The large bandgap (three times greater than Si) and very low intrinsic carrier concentration enables device operation at increased temperature (as high as 600 °C) and at high voltages (~10kV). The electric breakdown field of SiC is 5 times higher than Si, enabling very low specific on-resistance at the same time withstanding high current densities for SiC devices especially used in high power electronics. The large saturation drift velocity of SiC enables high frequency operation of devices under high power
conditions. In addition to the wide bandgap electronic properties, the material strength (chemical stability) of SiC provides a major advantage for devices intended to be used in harsh environments such as radiation detection, UV detectors in aerospace research, ignition system and exhaust sensors in automotive industries. Thus, SiC is one of the promising semiconductor material for fabricating compact high power devices with increased device performance, decreased size and weight.

Table 1.1 Properties of various semiconductor materials (Tolbert, Ozpineci, Islam, & Chinthavali, 2003)

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap, $E_g$ (eV)</td>
<td>1.12</td>
<td>1.43</td>
<td>3.03</td>
<td>3.26</td>
<td>3.45</td>
<td>5.45</td>
</tr>
<tr>
<td>Dielectric Constant, $\varepsilon_r$</td>
<td>11.9</td>
<td>13.1</td>
<td>9.66</td>
<td>10.1</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>Electric Breakdown Field, (kV/cm)</td>
<td>300</td>
<td>400</td>
<td>2500</td>
<td>2200</td>
<td>2000</td>
<td>10000</td>
</tr>
<tr>
<td>Electron Mobility, (cm$^2$/Vs)</td>
<td>1500</td>
<td>8500</td>
<td>⊥: 500</td>
<td>1000</td>
<td>1250</td>
<td>2200</td>
</tr>
<tr>
<td>Hole Mobility, (cm$^2$/Vs)</td>
<td>600</td>
<td>400</td>
<td>101</td>
<td>115</td>
<td>850</td>
<td>850</td>
</tr>
<tr>
<td>Intrinsic Carrier Concentration at 300 K, (cm$^{-3}$)</td>
<td>1.45x10$^{10}$</td>
<td>1.79x10$^{6}$</td>
<td>2.1x10$^{-5}$</td>
<td>1.5x10$^{-8}$</td>
<td>1.9x10$^{-10}$</td>
<td>$\sim$10$^{-27}$</td>
</tr>
<tr>
<td>Thermal conductivity, (W/cm/K)</td>
<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>4.9</td>
<td>1.3</td>
<td>22</td>
</tr>
<tr>
<td>Saturated Electron Drift Velocity, $V_{sat}$ (x10$^{7}$cm/s)</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2.2</td>
<td>2.7</td>
</tr>
</tbody>
</table>

$\varepsilon = \varepsilon_r\varepsilon_0$, where $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
**SiC crystal structure and polytypes:**

Silicon Carbide is a group IV-IV compound naturally occurring in the rare mineral Moissanite. Silicon carbide is useful for commercial and industrial applications due to its hardness, optical properties and thermal conductivity. Efforts to synthesize silicon carbide in a laboratory began in the late 1800s. Each silicon atom in the crystal is mostly covalently bonded (89% covalent and 11% ionic) to four carbon atoms and vice versa in a tetrahedral arrangement (fig.1.1). The strong bonding (4.53 eV) and short bond length (1.89 Å) between Si-C atoms provides SiC its very hard material strength. SiC does not melt but sublimes above 2100°C at atmospheric pressure (Ellison, 1999).

![Figure 1.1](image1.png)  
**Figure 1.1** Tetrahedral basic unit of SiC  

![Figure 1.2](image2.png)  
**Figure 1.2** ABC sites in hexagonal crystal lattice

In the tetrahedron shown in fig.1.1, it is to be noted that the basal plane consisting of three silicon atoms and the next plane of silicon atoms are separated by $d_{\text{plane Si-plane Si}} = 0.252$ nm, which is used for calculating the unit cell height of SiC. The plane containing the carbon atom in the tetrahedral interstitial space is $d_{\text{plane Si-plane C}} = 0.063$ nm from the basal plane. SiC occurs in many different crystal structures called polytypes. Even though all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical properties. The
tetrahedral bilayer orientation (stacking order and rotation) in a SiC crystal controls the lattice arrangement and hence its material properties. Two basic configurations arise from the stacking of successive basic tetrahedral units: either hexagonal (ABAB stacking) or cubic (ABC stacking) (fig.1.2).

While there are over 200 known polytypes of SiC (Fisher & Barnes, 1990), only a few are commonly grown in a reproducible form acceptable for use as an electronic semiconductor. These polytypes are characterized by the stacking sequence of the bilayers of the SiC structure. SiC polytypes are named based on the number of stacks (periodicity) before the sequence is repeated and the crystal symmetry. The most common polytypes of SiC presently being developed for electronics are the cubic 3C-SiC, the hexagonal 4H-SiC and 6H-SiC, and the rhombohedral 15R-SiC (fig.1.3). Change in the stacking sequence has a profound effect on the electrical properties. The band gap changes from 3.23 eV for 4H to 2.36 eV for 3C polytype (Levinshtein, Rumyantsev, & Shur, 2001). 3C-SiC is the only form of SiC with a cubic crystal (zinc blende) lattice structure and referred to as β-SiC. The non-cubic polytypes of SiC are referred to as α-SiC. If the stacking of the bilayer is ABAB ..., then the symmetry is hexagonal (wurtzite) and referred to as 2H-SiC (fig.1.3). All the other SiC polytypes are a mixture of the zinc-blende and wurtzite bonding. 4H-SiC consists of an equal number of cubic and hexagonal bonds with a stacking sequence of ABCB. 6H-SiC is composed of two-third cubic bonds and one-third hexagonal bonds with a stacking sequences of ABCACB. The overall symmetry is hexagonal for both polytypes, despite the cubic bonds which are present in each. Similarly, 15R-SiC is a rhombohedral crystal structure composed of three-fifth cubic bonds and two-fifth hexagonal bonds. In fig.1.3 the silicon atoms labeled "h" or "k"
denote Si-C double layers that reside in quasi-hexagonal or quasi-cubic environments with respect to their immediately neighboring above and below bilayers (Ayalew, 2004). In the 4H stacking sequence of ABCB, all the A sites are the cubic "k" sites and all the B and C sites are the hexagonal "h" sites. Similarly, in the 6H stacking sequence of ABCACB, while all the A sites are the hexagonal "h" sites, there are two kinds of inequivalent quasi-cubic sites for B and C, denoted "k1" and "k2" sites, respectively (Ayalew, 2004). To understand the SiC growth and related challenges it is essential to know its common polytypes in terms of stacking sequences, crystal directions, crystal planes etc. The important SiC polytypes available as substrate material are 4H and 6H-SiC. These polytypes require four and six Si-C bilayers, respectively, to define the unit cell repeat distance along the c-axis [0001] direction arranged in a hexagonal close packed (HCP) lattice.

![Figure 1.3 Stacking arrangements seen along [11\overline{2}0] direction of SiC polytypes (Ayalew, 2004)](image)

The close packed structures of these hexagonal polytypes can simply be described by four Miller-Bravais indexes noted \((h,k,i,l)\) which are referred to the four axes \((a_1, a_2, a_3)\).
a_3, c) shown in figure 1.4. In fig.1.4. the [1100] direction is often referred to as the \( p \) or \( m\)-axis and the [1120] direction is referred to as \( a\)-axis direction. A crystal will behave differently from different crystal directions due to variation in the stacking arrangement.

Since the hexagonal polytypes are made up of stacked double layers, several material properties are different along the c-axis or perpendicular to the c-axis. This is called anisotropy, and the degree of anisotropy is measured by the quotient of a parameter value along and perpendicular to the c-axis. Anisotropy of 1 is analogous to isotropic material. Several of the electrical parameters are anisotropic. As an example, for 6H-SiC, the mobility is different along c-axis and perpendicular to c-axis (Neudeck, 2006). Similarly, the crystal growth is different on different planes for growth rates and polytype replication (homogeneity) due to the variation in atomic packing density along different crystal directions.

Figure 1.4 Hexagonal unit cell of SiC showing different crystal planes

As all the SiC polytypes consists of repeated stacking along the c-axis, the 0001 surfaces have either Si or C atoms terminated layer named as Si face and C face, respectively. The 11% ionic bonding in SiC with Si atoms being positively charged induces polarity differences between C or Si terminated faces, which plays an important
role in the crystal growth process by influencing the polytype stability, the incorporation of dopants and impurities, and the crystal surface morphology.

1.3 SiC EPITAXIAL GROWTH METHODS:

The first successful growth of high purity SiC crystal using sublimation growth was developed by Lely (Lely, 1954). Lely’s initial process used a dense graphite crucible and a porous graphite thin-walled inner cylinder. The SiC powder is loaded between the inner and outer cylinder and heated to temperatures of 2550-2600°C in an argon atmosphere. Spontaneous nucleation of SiC was observed at the inner surface of the thin-walled cylinder (fig.1.5).

![Figure 1.5](image)

Figure 1.5 Lely process for SiC bulk growth (Saddow & Agarwal, 2004, p. 6)

The Lely method had several limitations in SiC growth such as the extremely high growth temperatures above 2000°C and the necessity to have an acceptable growth rate. This resulted in some serious disadvantages such as the concentration of defects being high, the control of platelet thickness, doping, and polytype of the crystal is poor due to the inability of controlling initial nucleation, growth rate, and growth direction.
(Wijesundara & Azevedo, 2011). A breakthrough came around 1980 with the introduction of SiC seed crystal sublimation growth. This method uses a high-quality seed crystal surface to begin the growth process (Tairov & Tsvetkov, 1978). The seeded sublimation growth is often referred to as the physical vapor transport method (PVT) or Modified Lely Method (MLM). The main idea is to sublimate SiC powder at high temperatures \( T > 2000 \, ^\circ \text{C} \) and to re-crystallize the Si- and C-containing gas species at a slightly cooler single crystal seed (fig.1.6).

![Figure 1.6 Schematic of a seeded sublimation (SE) or PVT growth reactor (Chaussende, Wellmann, & Pons, 2007)](image)

PVT is currently used as the standard industrial method for producing high quality SiC wafers owing to the technological improvements and maturity of the process. Currently 150 mm (6") 4H-SiC wafers are commercially produced by standard PVT method by CREE Inc. To make SiC devices superior in comparison to other standard semiconductor devices, high quality material with fewer defects is essential. Therefore, today most SiC electronic devices are fabricated on epitaxial layers grown on bulk SiC instead of directly making them on the wafers sliced from the bulk SiC crystals. Homoepitaxial growth of SiC refers to the growth of SiC films of same polytype as that of the substrates at relatively low temperatures (1500 °C to 1600 °C). Homoepitaxy offers
high structural uniformity, more controllability over the vapor phase composition, growth rate, doping and good reproducibility than the bulk growth (Wijesundara & Azevedo, 2011). Furthermore, since the precursor gas sources are extremely pure, the impurity concentration of the deposited material is up to three orders of magnitude lower than in bulk grown SiC and it is possible to grow n-type and p-type layers with good homogeneity and reproducibility (Ellison, 1999). The nitrogen background doping level can be decreased by increasing the C/Si ratio in the vapor phase by a theory called “site-competition epitaxy” (Larkin, Neudeck, Powell, & Matus, 1994) in which the nitrogen and carbon atoms compete for the carbon vacancies thereby reducing the nitrogen concentration in the epilayers and boron and silicon atoms compete for silicon vacancies thereby forming p-type epilayers. Polytype stability was significantly improved by the concept of step-controlled epitaxy on off-axis oriented (0001) SiC substrates (T. Kimoto, Itoh, & Matsunami, 1997).

Homoepitaxial growth of SiC films can be achieved by various means, each with its own advantages and disadvantages. Selection of a growth technique is determined by the application requirements and the technological maturity of the technique. Homoepitaxial techniques for SiC can be categorized into vapor phase epitaxy (VPE), liquid phase epitaxy (LPE), and vapor-liquid-solid (VLS) epitaxy (Wijesundara & Azevedo, 2011). The latter is a novel epitaxial approach which shares the common fundamentals of VLS nanowire and nanotube growth (Givargizov, 1975; Milewski, Gac, Petrovic, & Skaggs, 1985).

**Vapor phase epitaxy (VPE)** (Wijesundara & Azevedo, 2011): There are three main types of VPE, namely chemical vapor deposition (CVD), sublimation epitaxy, and
high temperature CVD (HTCVD). Among these, CVD is the most matured and researched technique for epitaxial growth of SiC. It is the core technique adapted by the industry for commercial production of epitaxial SiC wafers.

**Chemical Vapor Deposition (CVD)** (Wijesundara & Azevedo, 2011): In CVD growth of SiC, carbon- and silicon-containing gaseous compounds, which are termed as precursor gases are transported to a heated single-crystalline SiC substrate where the homoepitaxial growth occurs through a surface-induced chemical reaction. Depending on the polytype and the reactor configuration (hot wall or cold wall), the growth temperature can be considerably different, but typically, is above 1200°C.

**Cold Wall reactor:** The cold-wall configuration is achieved by using a double-walled quartz tube with water circulated between the walls. The wafer is placed on an inductively heated graphite susceptor. To ensure the cold-wall conditions, the sample is placed on a graphite susceptor (fig.1.7(a)). Cold-wall reactors suffer from shortcomings related to the thermal uniformity of the reactor because the area above the substrate is not actively heated which in turn causes poor precursor dissociation efficiency, which directly translates into the growth rate (Wijesundara & Azevedo, 2011).

**Hot-wall reactor:** The hot-wall reactor concept was first introduced by Kordina et al (Janzén et al., 1994). A graphite (thermally and electrically conductive) tube that runs along the entire length of the reactor is placed inside an air/water cooled quartz tube and the susceptor is placed inside graphite tube (fig.1.7(b)). Thermally conductive graphite helps in reducing the heat loss due to radiation and consequently, hotwall reactors consume less power (20-40 kW) than cold-wall reactors and also helps to
maintain thermal uniformity (Wijesundara & Azevedo, 2011). The advantages of using a hotwall reactor are: They enjoy better thermal uniformity in both lateral and vertical directions. In comparison, the temperature gradient in the vertical direction over the substrate surface can be as large as 220K/mm in a cold-wall reactor and that is nearly ten times higher than what is achievable in a hot wall reactor (Thomas, Bartsch, Stein, Schörner, & Stephani, 2004). At the same time the major disadvantage due to the low thermal gradient in hot-wall reactors is the early decomposition of the growth species causing undesired deposition on the reactor walls (parasitic deposition) and gas phase nucleation of reactant species falling on the sample surface producing particle defects leading to decrease in efficiency of the gaseous precursors during the epitaxial growth. This is a prevailing problem in hot-wall reactors and the key solution to this issue is to shift to a more thermally stable Si or C precursor.

Based on the deposition pressure, CVD can be categorized into atmospheric pressure CVD (APCVD) and low pressure CVD (LPCVD). LPCVD is most commonly used now-a-days as it offers better control of the growth process in terms of gas phase nucleation and impurity levels.

Figure 1.7 Schematic of (a) cold-wall reactor, (b) hot-wall reactor configuration (Wijesundara & Azevedo, 2011)
**Liquid phase epitaxy (LPE):** LPE is a method to grow semiconductor crystal layers from the melt on solid substrates. This happens at temperatures well below the melting point of the deposited semiconductor. In SiC growth, LPE gained interest following the reports indicating that micropipes can be filled or closed with this technique (Filip, Epelbaum, Bickermann, & Winnacker, 2004). The solvent in SiC LPE is silicon and the carbon source is either graphite container or the SiC added to the melt. Addition of metals e.g. Sc to the melt is also used to increase the C solubility. The driving force for the epitaxial growth is provided by applying a temperature gradient across the structure with a higher temperature at the source than at the substrate (Ellison, 1999). Since the growth takes place from the liquid phase, LPE technique has the advantage to provide high growth rates (up to 300 um/h) (Syväjärvi et al., 1999) however the surface morphology is not as good as achieved by the other epitaxial growth techniques.

**Molecular beam epitaxy (MBE)** (Wijesundara & Azevedo, 2011): Molecular beam epitaxy (MBE) is usually applied to grow very thin epitaxial layers. Consequently, the growth rate is in the order of nanometer per hour and normally the growth temperature should be quite low. For the controlled growth of SiC hetero-polytypic structures, consisting of few monolayers each of hexagonal and cubic polytypes, the growth conditions can be changed from low temperatures (1550 K) and an Si-rich Si/C ratio (3C-SiC) to higher temperatures (1600 K) and a more C-rich environment (4H-SiC) (Milewski et al., 1985).
1.4 STEP CONTROLLED SiC EPITAXY:

During the crystal growth process by CVD method, the gas molecules (growth species) in the gas phase approach the sample surface from different directions. Crystal growth on a c-plane (or basal plane) can take any arbitrary polytype when these gas molecules approach the surface as it is impossible to know the polytype (stacking arrangement) from the c-plane. So, growth on a c-plane (0001) is highly unpredictable since it does not expose any template needed for polytype replication during growth. Homogeneous crystal is highly essential for the realization of SiC devices.

As first realized by Frank in 1949, dislocations intersecting the surface of the real crystals provide the source of steps required for continuous growth of a crystal (fig.1.8). In 1951, Burton et al published the first quantitative model referred as BCF theory (Burton, Cabrera, & Frank, 1951) providing a comprehensive understanding of the surface phenomena involved in crystal growth.

Figure.1.8 Crystal growth initiated by a screw dislocation on an ideal on-axis surface (Burton et al., 1951)

In the late 1980s, successful growth of high-quality homoepitaxial 6H-SiC with a smooth morphology without 3C-SiC incorporation at 1400-1500°C using vicinal (which
are at a relatively small angle to the basal plane), or off-axis (off-oriented) substrates was reported (Kong, Glass, & Davis, 1988; Powell et al., 1990) by partially exposing the m-planes or a-planes in SiC crystal to create a template for polytype imitation by cutting the original crystal boule at an angle which is called the offcut angle (fig.1.9). The surface steps existing on the off-oriented substrates serve as a template for replication of the underlying polytype. This technique of growing epilayers on off-axis substrates is known as “step-controlled epitaxy” as described by Matsunami and Kimoto (T. Kimoto et al., 1997).

Figure.1.9 4H-SiC crystal showing offcut plane towards [11\bar{2}0] direction

This method was a significant breakthrough in homoepitaxial growth of SiC as it enabled production of high quality single crystal epilayers with replication of substrate polytype at reduced growth temperature than the bulk growth. This is beneficial in reducing contamination from the reactor wall and minimizing unwanted dopant diffusion. Fig.1.10. schematically illustrates the epitaxial growth process on (a) a well oriented and (b) an off-oriented 6H-SiC substrate (Tsunenobu Kimoto & Matsunami, 1994). The well oriented [0001] face consists of vast terraces and has very low step density. The growth
process proceeds through two-dimensional nucleation on the terraces due to high supersaturation on the surface. The growth process is controlled by surface reactions such as adsorption and desorption. Therefore, the primary factor that determines the polytype is the growth temperature. According to ABC notation, the stacking order of 6H-SiC is ABCACB while 3C-SiC can be either ABCABC or ACBACB. When 3C-SiC grows on a well-oriented face (due to the absence of steps), two adjacent nucleation sites may also lead to double positioned twins (Kong, Jiang, Glass, Rozgonyi, & More, 1988) as shown in Fig.1.10 (a). The off-oriented substrates possess high step density with narrow terrace width. The smaller terrace width allows the adatoms to reach the step through surface diffusion and promotes their lattice incorporation at the step edges. The steps contain dangling bonds which make them highly reactive and in addition to the step edges the growth process is governed by more reactive sites at the steps (kinks) resulting replication of the substrate polytype. The kink sites are very important because molecules that attach there make more bonds to neighboring molecules than the ones that attach to the terraces or to flat step edges (see fig.1.11). Consequently, they are more likely to stick. The initial studies on step-controlled epitaxial were performed on 6H-SiC polytype; however, later studies show its viability to homoepitaxial growth of other polytypes including 4H-SiC (Itoh, Akita, Kimoto, & Matsunami, 1994).
Growth mechanism on a stepped surface:

The remarkable success in step controlled epitaxy led to extensive research to understand the growth mechanism and the factors affecting step-controlled growth. The surface of the substrate is in equilibrium with its vapor pressure, $P_{eq}$, when the flux of adsorbed atoms from the vapor equals the desorption rate from the surface (Ellison, 1999). In the kinetic theory of gas approximation, the equilibrium flux density of incident atoms, $J$ is related to the equilibrium vapor pressure, $P_{eq}$, by:

$$J \text{ (m}^{-2}\text{s}^{-1}) = \sqrt{\frac{N_A}{2\pi R M k T}} P_{eq}$$  \hspace{1cm} (Eq.1.1)

Where $M$ is the molecular weight, $k$ is the Boltzmann constant, $N_A$ is the Avagadro’s number and $T$ is the absolute temperature.
The various surface processes involved at equilibrium on a stepped surface are shown in fig.1.11. The adsorbed species diffuse on terraces toward steps. Some of the adsorbed species can reach steps or kinks and are incorporated into the crystal, and others re-evaporate to vapor. The driving force of crystal growth is the supersaturation ratio of the vapor phase $\alpha$, which for an incident flux $J$ of vapor species supplied to the crystal surface can be defined by: $\alpha = \frac{J}{J_{eq}}$. When $\alpha > 1$ growth is promoted, whereas $\alpha < 1$ results in evaporation. In the BCF theory, the steps are assumed as uniform and perfect sinks for the incoming species, that is, the capture probability of adsorbed species at steps is unity, independent of the direction from which adsorbed species approach the steps. The adsorbed atoms migrate randomly on the terrace before they get incorporated in the crystal lattice or desorb. The mean distance $\lambda_s$ for adsorbed species to migrate on a ‘step-free’ surface before desorption is given by:

$$\lambda_s = \sqrt{D_s \tau_s} = a \exp\left(\frac{E_{des} - E_{diff}}{2kT}\right)$$  \hspace{1cm} (Eq.1.2)
where $\tau_s$ is the mean residence time of adsorbed species, and $D_s$ is the surface diffusion coefficient, $a$, $k$, and $T$ are the jump distance (interatomic distance of the impinging molecule), Boltzmann constant, and absolute temperature respectively. $E_{\text{des}}$ and $E_{\text{diff}}$ are the activation energies for desorption and surface diffusion. The growth takes place by the resulting lateral propagation of surface steps. At a supersaturation $\alpha > 1$, the net flux of growth species reaching the surface is the difference between the adsorption ($J$) and desorption ($n_s \tau_0$) fluxes:

$$J_{\text{net}} = J - \frac{n_s}{\tau_0}$$  \hspace{1cm} (Eq.1.3)

The net vertical growth rate $R$ can then be expressed by the velocity of lateral advancement of the steps, $v_{\text{step}}$, determined by the adatom diffusion and the step height, $h$ and is given by the product of the step velocity and $\tan \theta$ ($\tan \theta = h / \lambda_0$) (Tsunenobu Kimoto & Matsunami, 1994),

$$R = v_{\text{step}} \tan \theta = \frac{2h\lambda_0}{n_{s0}\lambda_0} \left( J - \frac{n_{s0}}{\tau_s} \right) \tanh\left( \frac{\lambda_0}{2\lambda_s} \right)$$  \hspace{1cm} (Eq.1.4)

where $\theta$ is the substrate off-angle and $n_{s0}$ is the density of surface adatom sites (C and Si) at equilibrium conditions. Thus, the growth rate equation above shows that a surface controlled growth rate presents an exponential temperature dependence due the adatom diffusion ($\lambda_s$). When the growth is on well oriented surfaces (misorientation from the basal plane is less than a degree), the growth rate is surface kinetics limited i.e., strongly dependent on the temperature resulting in high sensitivity to surface temperature which needs high activation energy and thus leading to growth rate non-uniformity. In the off oriented surfaces the presence of steps greatly influences the surface processes and under
sufficient temperature the growth rate becomes mass transport controlled and increases with increase in the offcut angle (increased density of steps).

**Step bunching in stepped surfaces:**

The formation of multiple-height steps (step bunching) has been an attractive but unresolved subject in crystal growth and surface science. During prolonged growth times step bunching is generally observed on the epilayer surface, because of coalescence of elementary steps into macrosteps with larger step height (fig.1.12). The surface is quite similar to the so-called ‘hill-and-valley (or faceted)’ structure, which often appears on grown surfaces which are off-oriented (Tsunenobu Kimoto, Itoh, Matsunami, & Okano, 1997; Syväjärvi, Yakimova, & Janzén, 2002). The off-oriented surfaces will rearrange spontaneously to minimize their total surface energies, even if this involves an increase in surface area.

![Figure 1.12 Schematic of a stepped surface showing regular array of steps and step bunching (Degawa, Minoda, Tanishiro, & Yagi, 1999)](image)

The surface free energies of SiC were calculated to be 2220 erg cm\(^{-2}\) for the Si face and 300 erg cm\(^{-2}\) for the C face (Tsunenobu Kimoto et al., 1997). Thus, in order to reduce
the overall surface energy, the Si face which is normally the growth face of SiC epitaxy forms ‘hill-and-valley’ structures (step bunching) on the off-oriented surfaces.

**Impurity incorporation or Site competition in step controlled epitaxy:**

The success of silicon carbide (SiC) for high temperature and high power electronic applications is dependent upon the ability to produce high quality SiC epilayers of both n-type and p-type in-situ doping with doping profiles ranging from extremely low doped epilayers for high voltage devices to degenerately doped layers for minimizing parasitic resistances (Larkin et al., 1994). Larkin et al, 1994, reported for the first time that the Si/C ratio within the growth reactor has a strong influence on intentional and unintentional dopant incorporation of the growing 6H, 3C, and 4H SiC (0001) epilayers. Specifically, the active n-type (nitrogen) carrier concentration was found to be directly proportional to the Si/C ratio, whereas, the active p-type (aluminum) concentration was found to be inversely proportional to the Si/C ratio for epilayer growth on the SiC (0001) basal plane. Dopants in SiC are believed to occupy specific sites, specifically nitrogen occupies the carbon site while aluminum occupies the silicon site of the SiC lattice (Choyke, 1990; Davis & Glass, 1991). The relative increase in carbon concentration in the precursor gas species “outcompetes” the nitrogen for the C-sites of the growing SiC lattice. The analogous situation exists for an increased Si/C ratio, in which the relative increase in silicon concentration “outcompetes” the Al for the Si sites of the growing SiC lattice. This model is referred as “site-competition” epitaxy and is used to rationalize the experimental results of active dopant dependence on the Si/C ratio.

Site-competition epitaxy was also successfully used to obtain very abrupt changes in dopant concentrations in SiC epilayers. In conventional CVD systems, the abruptness
of the dopant profile is limited by the purging of the dopant-source from the growth reactor. One advantage of epilayer growth using site-competition epitaxy is that more abrupt dopant profiles can be obtained by excluding the remaining unwanted dopant by changing the Si/C ratio along with the dopant-source gas (Larkin et al., 1994). Conversely, very abrupt, enhanced dopant incorporation can be accomplished for production of highly degenerately doped epilayers. One highly useful example of this is the ability to form very thin degenerately doped p-type and n-type contact layers by stopping the source-flow of Si or C, respectively, during the last minutes of epilayer growth. Subsequently deposited metal contacts are “ohmic as deposited” for a wide variety of metals on both p-type and n-type epilayers (Larkin et al., 1994).

1.5 STRUCTURAL DEFECTS IN SiC:

The structural defects nucleated in SiC epilayers as well as in the substrates attract interest because some of them have been demonstrated to be detrimental to device performance. The main dislocations that are discussed in SiC epitaxy are the micropipes (MP), threading screw dislocations (TSD), threading edge dislocations (TED), the basal plane dislocations (BPD) and stacking faults (SF) (N. Zhang, 2011). These common defects are shown after KOH etching in fig.1.13. Circular, or oval shapes are indicative of their directions in the crystal related to off cut.
Koga et al. in 1992 reported for the first time that a p-n junction presented a very low breakdown voltage when a micropipe was present (Koga, Fujikawa, Ueda, & Yamaguchi, 1992). Elementary screw dislocations (TSDs), although not as detrimental as micropipes, could adversely affect the breakdown voltage of SiC devices and deteriorate the performance and reliability of SiC power devices (Wahab et al., 2000). The basal plane dislocations and stacking faults are additional defects that were found to degrade the SiC device performance (Agarwal, Fatima, Haney, & Ryu, 2007; Sumakeris et al., 2006).

**Screw dislocations (SDs)** have both burgers vector and line direction along c-axis. The screw dislocations observed in SiC are divided as closed-core screw dislocations (threading screw dislocations, TSDs) and hollow-core screw dislocations (micropipes, MPs). In hexagonal SiC (4H and 6H) screw dislocations with Burgers vectors of magnitude two multiples of the c-lattice parameter or less are close-core SDs (Huang et al., 1999). The origin of the screw dislocations are related to nucleation faults.
due to the large energy needed for screw dislocation formation (Ohtani, Katsuno, Fujimoto, Aigo, & Yashiro, 2001).

**Micropipe (MP)** is the defect that has been discussed the most in SiC. The first topographic observation of the presence of MPs in SiC was done by Dudley et al. (Huang et al., 1999). MP is a pure screw dislocation with giant Burgers vector along the c direction. The critical Burgers vectors for a hollow core screw dislocation are 2c and 3c for 6H and 4H SiC, respectively (Heindl et al., 1998). Micropipe is the most detrimental defect for high power and high voltage devices because they increase the leakage current and reduce the breakdown voltage drastically (N. Zhang, 2011). Inheritance of MPs from the seed is commonly seen in growth of SiC. Also, they may come from the relaxation of stresses from handling damage on the seed surface. Another possible reason to nucleate MPs is the relaxation of stresses arising from the incorporation of inclusions of solvent or impurity which can occur on the seed surface. Filip et al. (Filip et al., 2004) reported the closure of 80% of the MPs with the diameter less than 5 µm using LPE process. Owing to the tremendous maturity in SiC bulk growth and wafer processing technology, at present the MPs density has been reduced to zero for a 3” wafer (www.cree.com).

**Threading edge dislocations (TEDs)** are pure edge type dislocations with Burgers vectors (1/3<1120 >) perpendicular to their line directions (along c-axis). Threading edge dislocation is introduced by extra half (1100) habit plane. Ha et al reported that the TEDs are mostly inherited from the substrate or converted from bent BPDs due to image force (Ha, Mieszkowski, Skowronski, & Rowland, 2002). Ha et al. also proposed the formation of TEDs due to prismatic plane slip. No detrimental effects
of TEDs has been reported in SiC devices except for a minor influence in reducing the minority carrier diffusion lengths (S. Maximenko et al., 2010).

**Basal plane dislocations (BPDs)** are the defects that lie in the basal plane (c-plane) of the crystal. The basal plane [0001] is the primary slip plane for 4H and 6H due to its largest inter-plane distance. These BPDs are screw or mixed (edge and screw) type depending on the angle between line direction and Burgers vector $\frac{1}{3}[11\bar{2}0]$. BPDs are formed mostly during the relaxation stress caused by temperature gradients introduced during cooling down from growth temperature to room temperature (Gao & Kakimoto, 2014).

Both screw and threading edge dislocations propagate perfectly to the epilayer from substrate, though basal plane dislocation mostly converts into threading edge dislocation (Ha et al., 2002; Ohno et al., 2004). Lower elastic energy of threading edge dislocation per unit length along the growth thickness is preferable to form during the growth than forming the basal plane dislocation of higher elastic energy (Ha et al., 2002). That is why it is assumed that most of the BPDs convert in to TED during epitaxial growth. The method of converting all the BPDs in the epilayer into TEDs is of paramount interest in the field of SiC epitaxy.

**Stacking faults (SFs)** are planar defects and they mostly exist in the primary slip plane, which, for SiC, is [0001]. They are formed due to the misalignment in the stacking order deviating from that of the parent polytype (fig.1.14). Extra energy is needed to generate the SF and this is called the SF energy. It differs greatly for different polytypes. The stacking fault is bounded by two Shockley partials. There are two different types of
SF namely, intrinsic SF (caused due to missing (vacancy agglomeration) of lattice atoms) and extrinsic SF (formed due to the insertion of extra interstitial layer of lattice atoms). Hong et al (Hong, Samant, & Pirouz, 2000) reported the stacking fault energy of 4H-SiC is 14.7±2.5mJ/m2 and that of 6H-SiC is 2.9±0.6mJ/m2. When forward voltage is loaded, basal plane dislocations with Burgers vector 1/3<1120> were observed to dissociate into two Shockley partial dislocations of Burgers vectors 1/3<1010> and 1/3<0110>. The Burgers vector is conserved by reaction 1/3<1120> = 1/3<1010>+1/3<0110> with a ribbon of stacking fault between the two Shockley partials (N. Zhang, 2011).

The existed stacking faults were also found to expand through the motion of Si-co cored partials under forward bias. These Formation and expansion of basal plane stacking faults bounded by partial dislocations were interpreted as the reason for the degradation of forward voltage (S. I. Maximenko, Pirouz, & Sudarshan, 2005)

Figure 1.14 Schematic of a stacking fault seen in 4H-SiC due to the slip in basal plane (0001)
1.6 STATE OF THE ART SiC WAFER AND DEVICE TECHNOLOGY:

Due to the persistent research in improving the quality of SiC bulk growth and processing technology, SiC wafers currently exhibit tremendous increase in quality. At present, a 4H-SiC 3” highly conducting wafer is obtained for ~$550 (CREE Inc., 2016). SiC 3” wafers with zero micropipe density and a BPD density of 500 to 800 cm⁻² [II-VI epiworks, Dow Corning and CREE Inc]. SiC power MOSFETs, Schottky diodes and IGBTs are commercially available with a temperature withstanding capability of 225°C [ROHM semiconductor]. SiC sensor market has also shown an increase in demand for its applications in harsh environments such as radiation detectors, UV detectors, exhaust gas sensing in automobiles and industries. Epitaxial Graphene on Silicon Carbide is a newly maturing technology owing to the versatile properties of graphene especially in the solar energy, fuel cells and other sensory applications. With the raising popularity and demand for SiC devices, the necessity to improve the quality of SiC epitaxy is the need of the hour to envision a SiC dominating market especially in the power electronics industry.
CHAPTER 2

HOMOEPITAXIAL GROWTH OF 4H-SiC USING HALOGENATED PRECURSORS

2.1 INTRODUCTION:

Homoepitaxial growth of SiC is one of the key processes in the fabrication of SiC devices. As mentioned in the previous chapter, though various methods are attempted in SiC epitaxial growth, chemical vapor deposition (CVD) is still the leading and the most attractive technique to grow thick and high quality epitaxial SiC layers for high power devices. One of the significant challenges in obtaining high quality thick SiC epitaxial films is to restrict/eliminate the Si gas-phase nucleation or aerosol formation during growth which is caused by the early decomposition of the growth species before reaching the surface of the substrate. The generated aerosol particles adversely influence growth by reducing the growth rate due to precursor losses, and affect crystal quality (Segal et al., 2000), since the Si droplets are carried to the crystal growth surface. Moreover, liquid aerosol particles adhere to the various reactor parts (parasitic deposition), and contribute to their severe degradation during epitaxial growth. These parasitic depositions are generally loosely bound, and can be carried to the growth surface during growth as particulates, resulting in degradation of crystal quality by introducing defects in the growing epitaxial layers (T Rana, Chandrashekhkar, & Sudarshan, 2012).
The conventional SiC-CVD process uses silane (SiH₄) as the Si-precursor, light hydrocarbons e.g. propane (C₃H₈) or ethylene (C₂H₄) as the C-precursor, and hydrogen as the carrier gas. Using Silane precursor, the gas decomposition starts early in the gas delivery system and leads to severe parasitic deposition in the reactor system and degradation of epilayer morphology due to particulates deposition on the growth surface (T Rana et al., 2012).

In recent years, chloride precursors such as CH₃Cl₃Si (Methyltrichlorosilane, MTS), SiH₂Cl₂ (Dichlorosilane, DCS), SiCl₄ (Tetrachlorosilane, TCS) and/or HCl addition are induced to achieve high growth rate and to reduce Si-droplet formation in 4H and 6H SiC-CVD process (Chowdhury, Chandrasekhar, Klein, Caldwell, & Sudarshan, 2011; Dhanaraj et al., 2006; La Via et al., 2006; Lu, Cheng, Zhao, Zhang, & Xu, 2009).

Recently, tetrafluorosilane (TFS, SiF₄), a fluorine based gas having the strongest Si-halogen bond (Si-F bond energy 565kJ/mol vs. Si-Cl bonding energy 381kJ/mol) (Kolditz, 1967), has been introduced as a novel Si-precursor in SiC epitaxial growth (Sudarshan, Rana, Song, & Chandrashekhar, 2013). As a thermodynamically stable compound, TFS breaks to elemental compounds only at a very high temperature above 2000°C (Collins, 2000). Interestingly, it reacts with C-containing species at a temperature less than 2000°C to facilitate the epi-growth of SiC. This deposition possible with presence of a hydrocarbon gas indicates that the hydrocarbons plays an important role in SiC growth by SiF₄. This temperature stability of TFS makes it a potential Si-precursor in SiC epitaxial growth by inhibiting parasitic deposition by 80% and eliminating Si droplet formation during SiC epitaxial growth (T Rana, Chandrashekhar, & Sudarshan, 2013; Sudarshan et al., 2013).
2.2 COMPARATIVE STUDY BETWEEN DCS AND TFS PRECURSORS:

A systematic study of parasitic deposition and its influence on the precursor efficiency for various precursors in the reactor is essential to improve the epitaxial growth. In this chapter, we report the results and discussion of a comparative study on 4° offcut SiC substrates between the halogenated Si precursors SiH₂Cl₂ (DCS) and SiF₄ (TFS) used in the author’s group for SiC homoepitaxy.

EXPERIMENTAL SETUP:

Epitaxial growth of SiC is carried out using an inverted chimney type vertical hot-wall CVD reactor (fig.2.1). This arrangement consists of a hot-wall, a gas injector and a substrate holding susceptor. TFS / DCS and propane are used as precursor gases. DCS or TFS was used as the Si-precursor with standard flow rates at 5.6 sccm and 10 sccm, respectively. Propane was used as the C precursor. Hydrogen was the carrier gas with a flow rate of 10 slm. Growths were performed for different C/Si ratios (from 0.3 to 2) keeping constant Si and varying the C flow rates. The growth temperature and pressure were 1600°C and 300 torr. The growth recipe is shown in fig.2.2. Commercially available 4H-SiC wafers (4° off cut towards [11-20], optically polished) cut into 8 mm × 8 mm pieces were used as the substrate for all the growth experiments in this study. The gas delivery system in the CVD reactor contains an injector tube and a funnel as shown in fig. 2.3 (a&b). The injector tube is axially split into two half parts (fig. 2.3a). This split tube can be assembled to form a complete tube before growth and can be observed after the growth by separating them. The parasitic deposition generated during the growth run can be directly observed on the inner wall of the injector tube, and can be quantitatively analyzed by weighing their difference before and after growth.
The epilayer thickness was measured using the fourier transform infrared reflectance (FTIR) spectroscopy and mercury probe C-V analysis technique was used for measuring the net unintentional doping concentration of the epilayers. The epilayer surface morphology was studied using an atomic force microscope (AFM) and Nomarski optical microscope (NOM), KOH etching was performed to determine the defect density in the epilayer.
2.3 PARASITIC DEPOSITION AND GROWTH RATE COMPARISON:

As explained previously, parasitic deposition is one of the major reasons that limits epilayer quality and causes high fabrication cost (T Rana et al., 2012). It occurs because of the decomposition/reaction of the precursors on the surface of the reactor wall, before reaching the substrate. The parasitic deposition is severe for high growth rate and/or long duration growth for thick epilayers. Fig.2.4 shows the CVD furnace geometry
and temperature distribution obtained by simulation using Virtual Reactor. Fig. 2.5 shows the split injector tube and bottom view of the injector funnel (cap) before and after growths using DCS and TFS for the same C/Si ratio = 1.8 and Si flow rate (10 sccm).

The parasitic deposition could be found as yellowish depositions on the walls.

Figure 2.4. CVD furnace geometry and temperature distribution simulated using Virtual Reactor (T Rana et al., 2012)

For DCS-growth, the parasitic deposition starts at ~900°C, reaches the maximum at ~1250°C on the injector tube (Fig. 2.5b), and then reduces on the injector cap (Fig. 2.5e), whereas for TFS-growth, the parasitic deposition occurs at ~1400°C mostly on the injector cap (Fig. 2.5f). By weighing the injector tube and cap before and after epigrowth, the overall parasitic deposition in TFS-growth is much less (~80%) than that in DCS-growth.
Figure 2.5 Deposition on injector tube (split) and Injector cap (funnel) (bottom view) for 1 hour growth with 10 sccm DCS or TFS. (a) and (d): before growth; (b) and (e): after DCS-growth; (c) and (f): after TFS-growth (Balachandran, Song, Sudarshan, Shetu, & Chandrashekhar, 2015)

Ideally TFS should not exhibit parasitic deposition at a temperature below 2000°C due to its high temperature stability (fig.2.6). Experimentally, deposition of 3C-SiC is observed (confirmed by Raman spectroscopy) in TFS growth on the injector funnel where the temperature is ~1400°C. It has been shown that the decomposition and reaction of TFS in the gas-phase is mediated by C-containing species. There are several potential reaction pathways that have been proposed (T Rana et al., 2013) as shown by Table 2.1. These reactions are all possible below the 2000 °C decomposition temperature for TFS. But it is evident that the presence of hydrocarbons makes TFS decompose (dissociate) at a temperature below 2000°C resulting in parasitic deposition on the injector cap portion (T Rana et al., 2013). Surface reaction kinetics also play an important role on TFS decomposition in the presence of C-containing species. This also suggests that the epitaxial growth of SiC using TFS is carbon mediated. Optimization of the reactor geometry (e.g., increasing the temperature gradient above the susceptor) can further reduce the parasitic deposition, especially in TFS-growth. In depth research on the influence of DCS and TFS
in the SiC epilayer properties such as growth rate, unintentional doping, surface morphology and defects is necessary for identifying the superiority of the precursors to obtain high quality SiC epilayers, which is one of the main objectives of the research presented in this chapter.

![Figure 2.6 Temperature versus Gibbs free energy of thermal decomposition reactions of SiH₄, SiH₂Cl₂ and SiF₄ (Sudarshan et al., 2013)](image)

2.4 GROWTH RATE VS. C/Si RATIO:

The growth rates at various C/Si ratios are shown in Fig.2.7. It can be seen that for DCS, the growth rate increases with C/Si ratio when C/Si<1 and saturates for C/Si >1. This indicates that the growth is C supply limited for C/Si<1 and Si-supply limited for C/Si>1. However, for TFS-growth, the growth rate continually increases with C/Si ratio up to C/Si=2. This suggests a strong C supply dependent growth mechanism for TFS growth. It should be noted that for TFS-growth, even at high Si flow rate (10 sccm), the growth is C- supply limited and epilayer has no particle defects. Epilayer surface of DCS
growth at 10 sccm (C/Si ratio =1.8, growth rate 21.5 um/hr) has more particle defects (~5/cm²) than DCS at 5.6 sccm (no particles). This is due to the increase in parasitic deposition and Si droplet formation on the injector with increase in DCS flow rate.

Figure 2.7 Growth rate vs. C/Si ratio for DCS and TFS-growth at different flow rates (Trend lines shown are guide to eyes) (Balachandran et al., 2015).

In step-controlled epitaxy, at typical temperatures, the growth is mainly limited by the diffusion of growth species into the boundary layer (the region near the surface of the substrate where the gas flow velocity, concentration of growth vapor species and temperature changes from the bulk gas flow region) (Tsunenobu Kimoto, Nishino, Yoo, & Matsunami, 1993). Increased growth rate at increased temperatures is shown to be due to the increased diffusivity of the gas molecules in the boundary layer at elevated temperatures. The non-saturating growth rates seen in TFS at high flow rate (10 sccm) is attributed to the mass transport limited growth with increase in precursor efficiency by minimizing parasitic deposition.
Table 2.1 Free formation energy (kcal/mol) for various SiC etching reactions calculated from JANAF thermochemical data (T Rana et al., 2013)

<table>
<thead>
<tr>
<th>Reaction</th>
<th>1800K</th>
<th>1900K</th>
<th>2000K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dissociation and evaporation reactions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SiC(s) → Si(s) + C(s)</td>
<td>13.72</td>
<td>13.53</td>
</tr>
<tr>
<td>2</td>
<td>SiC(s) → Si(l) + C(s)</td>
<td>12.90</td>
<td>12.00</td>
</tr>
<tr>
<td>3</td>
<td>SiC(s) → Si(g) + C(s)</td>
<td>58.19</td>
<td>54.60</td>
</tr>
<tr>
<td>4</td>
<td>SiC(s) → 1/2Si_2C(g) + 1/2C(s)</td>
<td>36.99</td>
<td>34.69</td>
</tr>
<tr>
<td>5</td>
<td>Si(l) → Si (g)</td>
<td>45.29</td>
<td>42.59</td>
</tr>
<tr>
<td>Hydrogen reactions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SiC(s) + 1/2H_2(g) → Si(g) + 1/2C_2H_6(g)</td>
<td>73.44</td>
<td>69.23</td>
</tr>
<tr>
<td>7</td>
<td>Si(l) + 1/2H_2 → SiH(g)</td>
<td>44.81</td>
<td>43.12</td>
</tr>
<tr>
<td>8</td>
<td>SiH(g) + H_2(g) → SiH_4(g)</td>
<td>48.96</td>
<td>52.02</td>
</tr>
<tr>
<td>9</td>
<td>C(s) + 3/2H_2(g) → CH_3(g)</td>
<td>42.86</td>
<td>43.47</td>
</tr>
<tr>
<td>10</td>
<td>C(s) + 2H_2(g) → CH_4(g)</td>
<td>25.94</td>
<td>28.62</td>
</tr>
<tr>
<td>11</td>
<td>2C(s) + H_2(g) → C_2H_2 (g)</td>
<td>30.50</td>
<td>29.26</td>
</tr>
<tr>
<td>12</td>
<td>2C(s) + 2H_2(g) → C_2H_4(g)</td>
<td>44.34</td>
<td>46.34</td>
</tr>
<tr>
<td>Halogen reactions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>SiF_4 → Si (g) + 2F_2</td>
<td>368.90</td>
<td>362.20</td>
</tr>
<tr>
<td>14</td>
<td>Si (l) + SiF_4 → 2SiF_2 (g)</td>
<td>19.69</td>
<td>15.93</td>
</tr>
<tr>
<td>15</td>
<td>SiHCl_2 → Si (g) + 2HCl</td>
<td>30.17</td>
<td>24.21</td>
</tr>
<tr>
<td>16</td>
<td>Si(l) +2HCl → SiCl_2 + H_2</td>
<td>-4.06</td>
<td>-3.79</td>
</tr>
<tr>
<td>17</td>
<td>C(s) + 1/4SiF_4 → CF + 1/4Si(g)</td>
<td>107.83</td>
<td>103.65</td>
</tr>
<tr>
<td>18</td>
<td>C(s) + 1/2SiF_4 → CF_2 + 1/2Si(g)</td>
<td>128.23</td>
<td>124.16</td>
</tr>
<tr>
<td>19</td>
<td>4C(s) + 3SiF_4 → 4CF_3 + 3Si(g)</td>
<td>184.63</td>
<td>180.62</td>
</tr>
<tr>
<td>20</td>
<td>C(s) + SiF_4 → CF_4 + Si (g)</td>
<td>211.04</td>
<td>206.36</td>
</tr>
<tr>
<td>21</td>
<td>2C(s) + 1/2SiF_4 → C_2F_2 + 1/2Si (g)</td>
<td>175.24</td>
<td>171.05</td>
</tr>
</tbody>
</table>

2.5 UNINTENTIONAL NET DOPING CONTROL VS. C/Si RATIO:

Grown SiC epilayers were examined using mercury-probe C-V technique to determine the net doping concentrations. Fig. 2.8 shows the unintentional doping concentration at various C/Si ratios for both DCS and TFS. Both the curves show doping dependence behavior agreeing with the “site competition” theory (Larkin et al., 1994). TFS-growth produces doping concentration by an order of magnitude lower than for DCS-growth at the same C/Si ratio. It should be noted that in TFS growth the precursor flow rates are higher and hence are the growth rates. The semi-insulating region for DCS
is of narrow range (C/Si ratio 1.6 to 1.8) compared to TFS (C/Si ratio 1.5 to 2) (Balachandran et al., 2015).

Figure 2.8. (a) Net doping concentration vs. C/Si ratio for (a) TFS (at 10 sccm), (b) TFS (at 5 sccm) and (c) DCS (at 5.6 sccm) growths.

The weak site competition in TFS growth is attributed to the strong Si-F bond and affinity. The high bond strength between F and Si increases the surface resident time of Si-F molecules impinging the growth surface. This increases the probability of elemental F to get incorporated in the crystal and C atoms being less mobile also stay on the surface, giving less chance for nitrogen or boron impurities to enter into the crystal lattice. It is demonstrated that substitutional F, Cl and Br behave like shallow single
donors in Si crystal (T. A. Rana, 2013). On the other hand, due to their strong electronegativity, these group VII elements can also behave like acceptors when they are tetrahedral interstitials. However, only F can be stable in interstitials due to their smaller size and hence F will have more tendency to behave like an acceptor unlike Cl. This phenomenon is believed to be responsible for reduced doping concentration and weak site competition in the TFS growth (for both high and low flow rates). A detailed SIMS analysis is required to quantitatively analyse to investigate F incorporation (if any) in the epilayers grown using SiF₄.

2.6 STEP BUNCHING AND SURFACE MORPHOLOGY:

The 4° epilayers grown using TFS and DCS showed some interesting morphological features (step bunching) in the AFM images with varying C/Si ratio. Step bunching was explained by the Schwoebel effect and it is a process through which the surface energy is lowered during the growth by which the fast growing steps on a surface catch up with the slower steps to form “hill and valley” like structures. The crystal surface has a varying elastic potential and the surface of a certain off cut substrate has a certain periodic elastic potential on the surface present prior to the growth. This potential changes dynamically during the growth based on various growth conditions (e.g. C/Si ratio) which results in varying step bunching. Micro steps are essentially related to the steps created due to the off cut of the wafers. The height of these micro steps is ~1nm for 4H SiC which is the height of the 4H-SiC unit cell. On the other hand, macrosteps are generated due to step flows with different velocity, where steps coalesce or merge with each other rendering a larger step with a collective height of multiple microsteps in the range of ~5nm or above, which is termed as step bunching.
The epilayer surface roughness was measured using AFM (Fig. 2.10) and the surface morphology was examined using NOM (Fig. 2.9). All the epilayers show step-bunching. It was observed that for DCS-growth (5.6 sccm), better epilayer surface morphology (less step-bunching) was obtained at low C/Si ratios (~0.6) as shown in Fig. 2.9a, and the surface roughness increases with C/Si ratio and growth rates (see fig.2.10). Severe step bunching was found at C/Si=1.8 (Fig. 2.9b). This tendency is consistent with the interpretation that step bunching is enhanced under a C rich condition (Tsunenobu Kimoto et al., 1997). For TFS (10sccm) growth, the RMS surface roughness does not show significant difference for increase in growth rates (fig.2.10) over a wide range of C/Si ratios from 1.0 to 2.0. But at C/Si=0.6, there are many triangular defects and growth
pits generated on the epilayer surface (fig. 2.9c). This may be attributed to TFS etching properties on the Si surface which is enhanced at low C/Si ratio due to less availability of C.

![Graph showing Epilayer RMS roughness vs. C/Si for DCS, TFS growths](image)

Figure 2.10 Epilayer RMS roughness vs. C/Si for DCS, TFS growths (Trend lines shown are guide to eyes)

**2.7 DEFECTS STUDY IN 4° EPILAYERS USING KOH ETCHING:**

Defects including basal plane dislocations (BPD) and in-grown stacking faults (IGSF) are studied on selected epilayers after molten KOH etching, as shown in Table 2.2. Although in DCS-growth at a low C/Si ratio of 0.6 the epilayer is of best morphology, the BPD and IGSF densities are high. This trend is also observed in growth using silane (Chen & Capano, 2005a). The BPD and IGSF densities also increase when DCS flow rate increases from 5.6 sccm (growth rate ~11.8 µm/h at C/Si =1.6) to 10 sccm (C/Si =1.8, growth rate ~21.5 µm/h). However, for TFS-growth at high flow rate of 10 sccm for C/Si =1.8 (growth rate ~28 µm/h), both low BPD and IGSF densities are preserved whereas at low C/Si ratio (C/Si = 0.6), there is increase in densities of both BPDs (~14 cm²) and IGSFs (~108 cm²) which is attributed to TFS etching that occurs during the growth at low C supply.
Table 2.2 Defect densities on epilayers grown using DCS or TFS

<table>
<thead>
<tr>
<th>Precursor</th>
<th>C/Si</th>
<th>BPD (cm$^{-2}$)</th>
<th>IGSF (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCS 5.6 sccm</td>
<td>0.6</td>
<td>114</td>
<td>25</td>
</tr>
<tr>
<td>DCS 5.6 sccm</td>
<td>1.6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>DCS 10 sccm</td>
<td>1.8</td>
<td>19</td>
<td>25</td>
</tr>
<tr>
<td>TFS 10 sccm</td>
<td>0.6</td>
<td>14</td>
<td>108</td>
</tr>
<tr>
<td>TFS 10 sccm</td>
<td>1.8</td>
<td>6</td>
<td>8</td>
</tr>
</tbody>
</table>

From this comparative study of halogenated precursors in SiC epitaxial growths using DCS and TFS, TFS exhibits great ability in suppressing Si gas phase nucleation even at high flow rates and considerably reduces the parasitic deposition compared to DCS growth. Controlled doping (low doping concentration) of epilayer with high growth rates and reduced surface roughness produced by TFS growth is suitable for high quality CVD growth to achieve SiC devices with excellent performance characteristics. DCS has proved to be an efficient precursor for SiC epigrowth, but the results produced by TFS show that it is a potential competitor to DCS with several improved properties more ideal for SiC epitaxial growth.
CHAPTER 3

EPITAXIAL GROWTH ON NEARLY ON-AXIS (0.5°) 4H-SiC

SUBSTRATES USING TFS\textsuperscript{1}

3.1 INTRODUCTION:

4H-SiC is a wide band gap semiconductor for producing high power (>3kV) and high temperature electronic devices (Casady & Johnson, 1996), which require thick high quality epitaxial layers, >30um. Homoepitaxial growth of 4H-SiC by Chemical Vapor Deposition (CVD) is the key enabling technology for improving the quality of these thick SiC films. These films often suffer from polytype inclusions, with SiC displaying >200 polytypes, with bandgaps varying from 2.3eV for the thermodynamically favorable 3C cubic polytype to 3.4eV for the 2H hexagonal polytype. The difference among the various SiC polytypes is the stacking sequence of double layers of Si and C atoms. The stacking sequence in the (0001) direction for the hexagonal polytype (also known as α-SiC) 4H is ABCB..., where A, B, and C represent the three possible positions of the double layers. The stacking sequence for the cubic 3C polytype, also known as β-SiC, in (111) direction is ABC. Change in the stacking sequence has a profound effect on the electrical properties (Levinshtein et al., 2001). The most important polytype for electronic devices is 4H-SiC (bandgap 3.23eV) owing to its wide bandgap and high thermal conductivity (Qteish, Heine, & Needs, 1992).

\textsuperscript{1}A Balachandran, H Song, TS Sudarshan, MVS Chandrashekar. Journal of Crystal Growth 448, 97-104. Reprinted here with permission of publisher.
Replicating polytype without extraneous polytypes (e.g. 3C) is critical to ensure high quality epitaxial layers for device fabrication and is typically done on off-axis substrates. The high surface density steps found on off-axis substrates provides the template for growth species to stick to the surface and replicate the substrate polytype structure. This mechanism is termed step-flow growth (Matsunami & Kimoto, 1997). Epilayers with high polytype uniformity and specular surfaces are generally possible with off-oriented substrates.

However homoepitaxy on off-axis substrates has several disadvantages such as: slicing the wafer from an on-axis growth boule resulting in greater material losses >50% as substrate diameter increases especially for 8° offcut, 4” and 6” wafers, with corresponding increase in cost (Treu, Rupp, Brunner, Dahlquist, & Hecht, 2004). Growth on off-axis substrates results in a greater likelihood of propagation of basal plane dislocations (BPDs) from the substrate into the epilayer (Bergman, Lendenmann, Nilsson, Lindefelt, & Skytt, 2001; Lendenmann et al., 2001). BPDs are defects that nucleate stacking faults under electrical stress that result in increased forward voltage drop and thus degradation/failure in bipolar devices/circuits (Skowronski & Ha, 2006). Eliminating BPDs completely from SiC epitaxial growth is of prime interest to increase the SiC material quality in the commercial scale.

A majority of BPD’s ~70-80% spontaneously convert to relatively benign threading edge dislocations (TEDs) during epitaxial growth(Z. Zhang & T. S. Sudarshan, 2005; Z. H. Zhang, Shrivastava, & Sudarshan, 2006). Processes for successful elimination of BPDs (~99%) have been demonstrated for off-oriented substrates by the method of BPD-TED conversion(Song & Sudarshan, 2013) that relies on the exposure of
the <0001> 4H-SiC basal plane near the BPD by either KOH/Eutectic, or H₂ etching (Myers-Ward et al., 2009). While these techniques are effective, they require multiple growths, etching and cleaning steps, adding complexity and cost to the epitaxial growth process.

A simpler solution to produce BPD free epilayers would be to directly use nearly on-axis or low offcut (tilt angle ≤1°) substrates for epi-growth. These substrates (offcut ≤ 1°) have very low BPD concentration to begin with due to the very small tilt in the basal plane (0001 plane) resulting in high conversion rate of substrate BPDs into energetically favorable TEDs on the epilayer.

**Conversion mechanism of BPDs to TEDs:**

As mentioned earlier, BPDs are device killing defects in epitaxial growth which are found to propagate in higher number from substrate to the epilayer for higher off cut angle. They are screw or mixed (edge & screw) dislocations formed on the (0001) basal plane (primary slip plane) of the SiC crystal (fig.3.1) due to the thermal relaxation stress experienced during the cooling process of bulk growth process.

![Dislocation Diagram](image)

Figure 3.1 Basal Plane Dislocation (screw and mixed (60°) dislocation) showing their burgers vector along {11 \( \overline{2} \)0} directions in the crystal lattice
As SiC homoepitaxial growth is dominated by off-oriented substrates (step controlled epitaxy), a wafer is cut from an on-axis boule at 4° or 8° offcut angle typically towards the [11̅20] crystal direction. Due to this offcut, BPD lines intersect and emerge on the surface of the wafer. BPDs are propagated to the epilayers from these intersection points during the epilayer growth. It was found that for 8° off axis samples, ~70 to 80% of the BPDs convert into TEDs and the rest of them propagate through the epilayer and emerge on the surface. For a lower off cut angle, it is energetically more favorable for BPDs to convert into TEDs (Ha et al., 2002).

As explained by Klapper and Küppers (Klapper & Küppers, 1973), BPD to TED conversion happens according to the following equation:

\[ W_{\text{BPD or TED}} = \frac{E_{\text{BPD or TED}}}{\cos \alpha} \]  
(Eq.3.1)

Where, \( W \) is the elastic energy of the dislocation per unit growth length, \( E \) is the elastic energies per unit length of dislocation line, \( \alpha \) is the angle between the dislocation line and the growth direction i.e., \( \alpha = 90\text{-offcut angle} \) (Z. Zhang & T. S. Sudarshan, 2005). With a reduction in the offcut angle, \( W_{\text{BPD}} \) increases while \( W_{\text{TED}} \) reduces. The elastic energies per unit length of dislocation line for BPDs and TEDs were found to be almost the same, i.e., \( E_{\text{BPD}} \sim E_{\text{TED}} \) and we get \( W_{\text{BPD}} \gg W_{\text{TED}} \). Hence it is energetically favorable for a BPD to get converted into a TED during epitaxial growth on a low offcut substrate as shown in fig.3.2 (Z. Zhang & T. S. Sudarshan, 2005).
Figure 3.2 a) BPD conversion and propagation and b) Quasi on-axis surface showing BPD to TED conversion due to increase in $W_{BPD}$

For a higher off cut angle (4° or 8°) more BPDs can propagate into the surface as $W_{BPD}$ and $W_{TED}$ become comparable. So, lower off cut angle very close to the basal plane is preferable over higher off cut angle in many ways. However, higher density of some other defects such as 3C inclusions, triangular defects, inverted pyramid and step bunching are observed on the epilayer grown on lower off cut angle substrate. So, there might be two ways to eliminate BPD in SiC epitaxial growth. One approach is to move to lower off cut angles; this will solve both material wastage and BPD issues. The other solution might be to find an effective method to convert all the BPDs to TEDs during the epitaxial growth on higher off cut substrate. However, material wastage cannot be prevented by the second.

But the challenge in growing homoepitaxial layers on ideally on-axis or low vicinality (basal) surfaces is the difficulty to maintain 4H-SiC polytype uniformity due to the inclusion of thermodynamically favored cubic 3C-SiC polytype in the growth process (Hallin, Wahab, Ivanov, Bergman, & Janzén, 2004; Hassan, Bergman, Henry, & Janzén, 2008; S. Nakamura, T. Kimoto, & H. Matsunami, 2003). This is due to the lower density of steps on the surface, so that the adatoms on the surface only see the $<0001>$ basal
plane template, which reveals no stacking sequence, thereby initiating the terrace nucleation of the thermodynamically favorable 3C polytype. This is opposed to the \(<1120>\) or \(<1100>\) faces at the step edges, which do reveal the stacking structure described above, enabling homoepitaxy. Thus, good homoepitaxial growth is achieved by the minimization of terrace nucleation of 3C-SiC, and maximizing step-flow growth.

Good 4H-SiC homoepitaxial growth can be achieved by i) increasing temperature to encourage desorption of growth species from the terrace surfaces, although this can also reduce growth rate by increasing desorption from step-sites; ii) by using off-cut substrates as discussed above and iii) by changing the chemistry of the CVD process, which in turn affects the surface kinetics, thereby breaking certain inherent tradeoffs in the growth(Sudarshan et al., 2013). Previous studies have used this method to varying degrees of success(Song, Rana, Chandrashekhar, Omar, & Sudarshan, 2013), particularly with the addition of halogens to the growth to increase the volatility of growth species on the terrace surfaces. Previous studies have focused on the use of Cl-based chemistries (see below). While F-based chemistries are expected to offer improvements(T Rana et al., 2012), a systematic study of on-axis growth has not been performed.

Qualitative studies in understanding the mechanism of 4H-SiC homoepitaxial growth on Si-face of ideally on-axis (step-free surfaces) and vicinal surfaces have been conducted previously. In-situ surface preparation techniques, growth parameters and growth temperature play a vital role in maintaining the polytype uniformity in on axis epilayers free of BPDs (Hassan et al., 2008). Hassan et al (Hassan et al., 2008), Leone et al (Stefano Leone, Henrik Pedersen, Anne Henry, Olof Kordina, & Erik Janzén, 2009a) demonstrated that high quality 4H-SiC homoepitaxial layers could be grown using Cl-
based CVD. However, in their process, the dominant growth mode was spiral growth, rather than step-flow growth, leading to degradation of morphology, and potentially increasing the likelihood of 3C nucleation and rough surfaces. For ideally on-axis substrates the growth mode is dominated by the spiral growth provided by the screw dislocations intersecting the surface (S.-i. Nakamura, T. Kimoto, & H. Matsunami, 2003). Earlier studies showed that the spiral growth mode of on-axis epilayers has a strong dependence on C/Si ratio, with lower C/Si ratios favoring step-flow growth, and higher C/Si ratios favoring spiral growth that degrades the surface morphology, and can eventually lead to 3C nucleation (Stefano Leone, Henrik Pedersen, Anne Henry, Olle Kordina, & Erik Janzén, 2009b). There can also be terrace 3C nucleation at low temperatures, and nucleation at spiral growth sites. This is mitigated by using higher temperature growth to encourage desorption of growth species from the terraces, although this also can lead to lower growth rates. Studies on hetero epitaxial growth of high quality 3C-SiC intentionally grown on 4H-SiC/6H-SiC on-axis (step free) surface (Neudeck et al., 2006) show that 3C-SiC nucleation is favored at temperatures significantly lower (~1300°C) than the typical homoepitaxy temperature ~1600°C. Kimoto et al. (S. Nakamura et al., 2003) showed that judicious preparation of the SiC surface with HCl etching encouraged homoepitaxy, although polytype uniformity was still an issue. Clearly, there is a need for investigating the key growth parameters that govern homoepitaxy on on-axis substrates, and this study provides some additional understanding. In this chapter, a novel method to grow high quality step flow mediated homoepitaxial layers on Si face of nominally on-axis (±0.5°) 4H-SiC substrates with high polytype uniformity using TetraFluoroSilane (TFS) as the Si precursor is discussed.
3.2 EXPERIMENTAL SETUP:

Highly N-type doped (~10^{19} cm^{-3}) 4H-SiC (0001) on-axis substrates diced into 8 x 8 mm² samples from a 3” wafer from Cree Research Inc. was used in this work. Tilt angle ranged between ±0.5°. The substrates were degreased with organic solvents, de-oxidized with HF and rinsed with de-ionized water before being blown dry with Argon for growth. A Graphite susceptor with TaC coating was used as the sample holder (Landini, 2000). TaC coating on graphite susceptor reduces the residual acceptor impurity (Boron) concentration present in graphite by serving as a getter (Spencer, 1998) by providing thermal stability to graphite at high temperatures. In-situ etching was carried at 1600°C with only H₂ at 10 slm for 5 min and at 300 torr pressure (T. Rana et al., 2012).

Growths were performed in a home-built vertical inverted chimney hotwall reactor for different C/Si ratios keeping the Si precursor (TFS) flow rate constant at 5 sccm and varying the C precursor (propane) flow rate. Previously, good epilayer growth on on-axis substrates was shown using TFS (10 sccm) only at a C/Si ratio of 0.3 (T. Rana, 2013). The polytype uniformity degraded dramatically above a C/Si ratio of 0.3 due to the combined effects of reduced etching and higher growth rates at higher C/Si ratios. The growth results reported in this work were carried at a low TFS flow rate of 5 sccm and the temperature was maintained at 1600°C at 300 Torr pressure for 1 hour. H₂ (10 slm) was used as the carrier gas. The thickness of the epilayers were measured using the Fourier transform infrared reflectance (FTIR) (Sunkari, Mazzola, Mazzola, Das, & Wyatt, 2005). Surface morphology of the epilayers was analyzed using Nomarski Optical Microscope (NOM) and tapping mode Atomic Force Microscope (AFM). Net doping
concentrations of the epilayers were measured by mercury probe Capacitance-Voltage method (Kim & Davis, 1986). Polytype uniformity ensures the quality of SiC homoepitaxial growth. To check the crystalline quality and polytype inclusions Raman analysis was performed (Nakashima & Harima, 1997). The Raman spectra were obtained using a Jobin-Yvon Raman spectrometer equipped with a charge-coupled-detector array for emission at room temperature. The excitation was carried out at room temperature using a 632 nm He-Ne laser excitation source with 2 μm spot size with 500x objective.

3.3 HIGH QUALITY NEARLY ON-AXIS EPITAXIAL GROWTH USING TFS:

**Growth rate and net doping concentration vs. C/si ratio:**

The growth experiments were carried out at different C/Si ratios which were varied by keeping Si precursor (TFS) flow constant and varying the C precursor (Propane) flow during each growth. As shown in fig.3.3(a), the growth rate gradually increases with the increase in C/Si ratio, as opposed to the C-independence often seen with silane-based growth (Chen & Capano, 2005b). With Cl-based growth, some C-dependence is seen, which saturates at higher C/Si ratios (Song et al., 2013). However, in this study, we observe two distinct growth regimes, one at C/Si<1.8, which shows growth rate, $R_g \approx 6\text{um/hr}$, relatively independent of C/Si ratio, and a second at C/Si>1.8, which shows an approximately linear dependence on C/Si ratio up to $\sim 14\text{um/hr}$. Thick epilayers (> 20 um) can be achieved by increasing the duration of growth. All layers were specular, with varying degrees of polytype uniformity, which will be discussed in the following section.
These two growth regimes are also reflected in the C/Si dependence of the unintentional doping of these homoepitaxial layers (Fig. 3.3 (b)). Site-competition (Larkin et al., 1994) is clearly observed, with N-type net doping concentration, $N_d$ ranging from $\sim 5 \times 10^{18} \text{ cm}^{-3}$ to $\sim 7.2 \times 10^{14} \text{ cm}^{-3}$ for C/Si~0.6 to 2.5. In SiC epitaxy, C and N compete for the same site. Therefore, at low C/Si ratio, there is an undersupply of C, providing more sites for N-impurities in the ambient to enter the growing SiC crystal. At high C/Si, these sites are filled, minimizing N-incorporation, and eventually transitioning to p-type doping. Typically, the C/Si trend is monotonic, unlike the regime-2 behavior seen here for the growth rate. At C/Si ratio<1.8 (regime 1), typical site-competition is seen (fig.3.3(b)). However, at C/Si>1.8 (regime 2), a significant weakening of this behavior is observed; i.e. at high C/Si ratio, there is no transition to p-type. This behavior indicates that there is additional supply of Si-species competing with the B thus enabling n-type growth at high C/Si ratios. This is despite the fact that the SiF$_4$ silicon precursor supply
has been constant, thus creating a virtuous positive feedback loop at C/Si ≥ 2.0. The inference of additional Si-supply is supported by the faster growth rate (Rg), linear in C/Si, seen at C/Si ≥ 2.0 (fig.3.3(a)). This observation is consistent with previous observations that without the addition of carbon, SiF₄ does not decompose to liberate silicon species for growth (T Rana et al., 2013), attributed to the extremely large Gibbs free energy change (ΔG) of ~360kcal/mol required for the direct decomposition of SiF₄ to elemental Si (Table 2.1 (chapter 2), equation 13). However, with the addition of carbon, pathways for elemental-Si liberation, with significantly smaller ΔG~100-200kcal/mol (Table 2.1, equations 17-21) are activated, providing additional Si to the growth which is explained visually in fig.3.4.

In regime 1(fig.3.4), it is shown that the boundary layer (region formed just above the surface of the epilayer) near the growth surface is predominantly controlled by the etching reaction of TF₃S with the surface Si (table 2.1, equation 14) at low C/Si ratios (≤1.8). The removal of Si by reaction with SiF₄ (etching process) does not contribute to SiC growth due to the low C/Si ratio resulting in a suppressed growth at regime-1. In regime 2 (fig.3.4), a Si liberation reaction (table 2.1, equation 17) happening at high C/Si ratios (>1.8) in the boundary layer is shown. This additional elemental Si will drive the spontaneous decomposition of SiC (Table 2.1 Equation 2, ΔG~13kcal/mol) backward (leading to deposition or growth) which also slows down the etching of SiC by SiF₄ (Table 2.1, equation 14).
Figure 3.4 Schematic of important growth reactions responsible for two different growth regimes (Balachandran, Song, Sudarshan, & Chandrashekhar, 2016)

At high C/Si ratio, without free Si on the SiC surface, the etching reaction (Table 2.1, equation 14) \( \text{SiF}_4 (g) + \text{Si (l)} \rightarrow \text{SiF}_2 (g) \) is suppressed. Therefore, the combination of reduced etching, and liberation of additional Si species by the additional reactions at higher C/Si both lead to the transition from regime 1 to regime 2 (Fig 3.3(a)). While this analysis has been done for the liberation of elemental Si, there will certainly be additional more complex reaction pathways at high C/Si leading to the liberation of additional SiF\(_2\), which will also drive the etching reaction 14 backward (towards deposition), again giving rise to linear growth rates (as shown in regime-2 of fig.3.3(a)). Further numerical simulations of the growth process are required to establish the key controlling reactions, although the morphological and polytype observations in the following suggest that elemental Si might be responsible.
Raman analysis:

Characteristic Raman spectra of 4H and 3C-SiC polytypes are shown in fig. 3.5(a) and (b) respectively. As reported by Nakashima and Haima (Nakashima & Harima, 1997), the phonon modes of interest in 4H-SiC include planar folded transverse optic (FTO) modes at 776 and 796 cm\(^{-1}\), respectively and an axial folded longitudinal optic (FLO) mode at 964 cm\(^{-1}\). For cubic SiC (3C-SiC) a dominant TO mode is at 796 cm\(^{-1}\) and an axial LO mode at 972 cm\(^{-1}\) (fig. 3.5(b)). For all the samples, the 4H-SiC characteristic (FTO and FLO) peaks were visible at 776 to 780 cm\(^{-1}\) and ~ 979 to 967 cm\(^{-1}\) (fig. 3.5(a)). The red shift (decrease in wavenumber) observed for FLO peaks with increasing C/Si ratio is as reported by Yugami et al (Yugami et al., 1987) and is attributed to the impurity (doping) incorporation which decreases as the C/Si ratio increases (fig. 3.5(c)).

The large difference in the wave number values between C/Si = 0.6 (~978.5 cm\(^{-1}\)) and C/Si = 1.0 (~970.5 cm\(^{-1}\)) is due to the large difference in doping concentration between those ratios. As reported by Yugami et al, the frequency of FLO band increases rapidly for carrier concentration above 5x10\(^{17}\) cm\(^{-3}\) and show less variation for carrier concentration below 1x10\(^{17}\) cm\(^{-3}\). As the net doping concentration decreases with increase in the C/Si ratio the Full Width Half Maximum (FWHM) of the 4H-FLO peaks also decreases (fig.3.5(d)). This is due to the collective excitation of the free carriers (plasmons) interacting with the longitudinal optical phonons to form LO phonon-plasmon coupled modes (LOPC) which is termed as FLO peak. The FWHM of 4H-FLO peak is sensitive to the change in free carrier density (doping concentration) as the Raman scattering process is governed by the electro-optic (EO), deformation potential (DP) and charge density fluctuation (CDF) at LOPC mode (Nakashima & Harima, 1997).
Figure 3.5 Raman spectra showing characteristic peaks of 4H and 3C-SiC taken on (a) C/Si = 2.5 and (b) 3C part of C/Si = 1.0, (c) 4H-FLO peak wave number vs. epilayer net doping concentration, (d) 4H-FLO peak linewidth (FWHM) vs. epilayer net doping concentration.

The intensity ratio values of 4H-FTO peak to 3C-FTO peak which is a measure to evaluate polytype uniformity is given in fig.3.6. Varying degrees of polytype uniformity were observed for epilayers grown at different C/Si ratios. From the ratio of peaks, it can be observed that the epilayer regions with negligible 3C inclusion have 4H/3C ratio >15 and for regions with significant 3C inclusions the intensity ratio was found to be < 5. For C/Si ratios <1 and ≥2 the Raman 4H/3C peak ratio >15 was found for entire epilayer surface suggesting a better polytype uniformity of epilayer. For C/Si ratios 1.0 to 1.8, the
4H/3C ratio varied throughout the surface of the epilayer indicating a poor polytype uniformity of the epilayer.

**Surface morphology:**

From fig. 3.6, it is evident that the morphology of the epilayers shifts from a wavy step-flow at low C/Si ~ 0.6, to a combination of island/spiral growth with step-flow growth at 1< C/Si <1.8, then back to pure step flow at high C/Si >1.8. These regimes correspond with the Rs and doping regimes outlined above, further strengthening the argument that new chemical pathways have been activated at C/Si>1.8.

For the epilayers grown using TFS at 5 sccm, at low C/Si~0.6, the epilayer shows wavy step flow growth throughout the surface with few small spirals (fig.3.6 (a)). Very few screw dislocations emerging from the substrate are seen on the epilayer. At low C/Si conditions, step-flow growth is observed due to the suppressed nucleation process on the terrace enabling flow of steps. This happens due to enhanced surface etching at Si rich conditions (Table 2.1, equations 1, 14). Increased surface etching minimizes the probability of nuclei attaching to the terrace making it energetically less favorable and thus suppressing the spiral growth (S.-i. Nakamura et al., 2003). Waviness on the surface steps (fig.3.6(a)) is attributed to the presence of step bunching often observed on substrates with smaller offcuts (i.e. 4°)(T Rana et al., 2013).

With the increase in C/Si (Fig.3.6(b-d)), increase in the 3C inclusions (spiral and island growth) on the epilayer surface is observed. As the C/Si ratio increases, availability of C in the boundary layer (formed just above the surface of the epilayer) increases. This mitigates the surface etching reaction rate of SiF₄ on Si (Table 2.1,
equation 14) due to the hindrance offered by the cluster of C atoms present near the surface for the reaction between SiF₄ and Si atoms on the surface resulting in slow etching (Fissel, 2000). Thus, 2D nucleation rate for 3C polytype inclusion becomes more than the surface adatoms desorption rate. It has been calculated that at high carbon partial pressure (elemental C availability) and at lower growth temperature the thermodynamic stability of the 3C polytype is higher than any other SiC polytypes (Danielsson, Henry, & Janzén, 2002). It is also speculated that carbon species adhere better on a flat surface (on-axis or low vicinality substrates) and Silicon species diffuse in the gas phase more slowly than carbon species due to their larger molecular weight (Danielsson et al., 2002), especially through the boundary layer. Increase in C/Si reduces the desorption capacity of C atoms (on flat surfaces) from the surface thereby increasing carbon supersaturation near the surface favoring 3C inclusions (Leone et al., 2009b). The evidence for lower off-angle substrate epitaxial layers being “carbon rich” is reported both by Huh et al. (Huh et al., 2006) and Yamamoto et al. (Yamamoto, Kimoto, & Matsunami, 1997). The experimental data for doping (fig.3.3 (b)) agrees with the above statement where doping concentration (Nitrogen incorporation) decreases at these C/Si ratios (1, 1.5, 1.8), which is in accordance with the site-competition-epitaxy theory (Larkin et al., 1994).

An interesting feature is observed at very high C/Si (>1.8) (fig.3.3(a) –Regime 2) with the surface morphology shifting back to uniform step flow growth without any 3C inclusions (fig. 3.6 (e), (f)). As discussed earlier, abundant supply of Carbon at ratios ≥ 2.0 liberates additional Si in the gas phase (Table 2.1, equations 17-21). Non-saturating increase in Rg (fig.3.3 (a)) and low n-type doping concentration (suppressing the transition to p-type) (fig.3.3 (b)) serves as a strong evidence of elemental Si liberation at
C/Si ≥2. It is found that 4H-SiC is more stable at high C/Si as hexagonal polytype is favored at C rich conditions (Fissel, 2000) whereas 3C-SiC is more stable at low temperature and occur at high supersaturation conditions as observed and explained for 1 ≤ C/Si ≤ 1.8. Thus the suppression of 3C inclusions in growth regime 2 (C/Si ≥ 2) happens due to the combined effects of C-rich condition additionally liberating gas phase Si that lowers C supersaturation near the growth surface favoring 4H-SiC formation (Fissel, 2000).

Typically, nearly on-axis epilayers with no 3C inclusions show uniform spiral growth (Leone et al., 2009b; S.-i. Nakamura et al., 2003). But the epilayers grown at C/Si ≥ 2 reported in this paper exhibit uniform step flow growth (fig.3.3 (a) –Regime 2). The reason for this prominent change in surface morphology is due to several C-reactions that liberate elemental Si (fig.3.4 and Table 2.1, equations 17 to 21) at the high growth temperature (1600 °C) as discussed earlier in this paper. On a nearly on-axis substrate, a regular array of steps is present. Spirals are formed as a result of revolution of pinned steps created by dislocations merging at a surface (Burton et al., 1951). Due to the step line tension, there is a critical curvature (ρc) above which a spiral grows (S.-i. Nakamura et al., 2003). If the growth velocity of a straight step is $V_{step}$, the angular velocity of spiral $\omega$ is given by (Budevski, Staikov, & Bostanov, 1975)

$$\omega \approx 0.33 \frac{V_{step}}{\rho_c}$$

(Eq.3.2)

Accordingly, the time required for one turn of spiral is,

$$T = \frac{2\pi}{\omega} \approx \frac{19\rho_c}{V_{step}}$$

(Eq.3.3)
If the time taken for straight steps (t) is faster than the time taken by spiral steps (T), i.e., when \( t < T \), a spiral will not form. Using the simple surface diffusion model proposed by Kimoto et al (Tsunenobu Kimoto & Matsunami, 1994), step-flow growth rate is given by,

\[
R_g = V_{\text{step}} \tan \theta
\]  
(Eq.3.4)

Where \( V_{\text{step}} \) is the step velocity and \( \theta \) is the off-angle of a substrate (~0.5°). Since \( R_g \) increases almost linearly for \( C/\text{Si} \geq 2 \) (fig.3.2 (a) regime 2) compared to that of \( C/\text{Si} < 2 \) (fig.3.2 (a) regime 1), the straight step velocity with increasing \( R_g \) overcomes the spiral step velocity suppressing the spiral growth at \( C/\text{Si} \geq 2 \). Thus, increase in \( R_g \) due to extra Si that is liberated during the growth reactions at \( C/\text{Si} \geq 2 \) influences step flow growth and suppresses spiral growth.

\[
\frac{4H - FTO}{3C - FTO} = 32
\]

(a)

\[
\frac{4H - FTO}{3C - FTO} = 2.3
\]

(b)

\[
\frac{4H - FTO}{3C - FTO} = 18.5
\]
Figure 3.6 NOM images (100x magnification) and AFM images (5x5 μm²) of nearly on-axis epilayers grown using TFS (5 sccm). (a) C/Si = 0.6, Rg = 5.6 μm/h, (b) C/Si = 1.0, Rg = 5.8 μm/h, (c) C/Si = 1.5, Rg = 7.2 μm/h, (d) C/Si = 1.8, Rg = 6.3 μm/h, (e) C/Si = 2.0, Rg = 9.2 μm/h, (f) C/Si = 2.5, Rg = 14.4 μm/h
Homoepitaxial growth on nearly on-axis 4H-SiC using the novel fluorinated Si precursor at low flow rates (5 sccm) has been studied in detail. The grown epilayers exhibit good polytype uniformity at low and high C/Si ratios. A two-regime growth model is reported. A novel growth regime is identified at C rich conditions and new reaction pathways are highlighted to obtain uniform step flow growth of on-axis epilayers with low surface roughness (~1nm). This study demonstrated the possibility of achieving BPD free nearly on-axis epilayers with C/Si ratio dependent high 4H polytype uniformity (regime 2) without any additional pretreatment process for the substrates. Epilayers with growth rate ranging from low (5um/hr) to a maximum of ~15 um/hr (step flow) is reported which can be extensively used for fabricating high power devices free of BPDs.
CHAPTER 4

BASAL PLANE DISLOCATIONS (BPD) FREE 4° 4H-SiC EPILAYERS USING DCS¹

4.1 INTRODUCTION:

4H-SiC homoepitaxy on off-oriented substrates is the key to fabricating reliable SiC bipolar power devices. High gain 4H-SiC bipolar junction transistor (BJT) devices have potential applications in high power switching (Ryu, Agarwal, Singh, & Palmour, 2001). However, off-oriented substrates suffer from a major drawback of producing device killing crystal defects such as Basal Plane Dislocations (BPDs) on the grown epilayers which nucleate into Shockley-type stacking faults (SF) under bipolar forward bias conditions and deteriorate the device performance characteristics by limiting minority carrier concentration and causing forward voltage drifts (Wheeler et al., 2011). As mentioned in the previous chapter, off –oriented substrates promote the propagation of Basal Plane Dislocations on the epilayers due to the tilt in their basal plane (0001, c-axis). BPDs are Shockley type dislocations that can glide along the basal (0001) plane of the growing crystal. About 70 -90% of BPDs in the off oriented substrate spontaneously convert to threading edge dislocations (TEDs) at the epilayer/substrate interface (Z. Zhang & T. Sudarshan, 2005a) or during the growth throughout the epilayer thickness (Myers-Ward et al., 2009) with the conversion efficiency depending upon growth conditions (Ohno et al., 2004).

However, a fraction of the substrate BPDs propagates into the active layers of devices where they are detrimental to device performance, and are currently considered the yield-limiting killer defect in SiC power devices (Wheeler et al., 2011).

Figure 4.1 BPD with dislocation line parallel to the [11-20] off-cut direction (Z. Zhang & T. Sudarshan, 2005b).

With a reduction in the offcut angle, $W_{BPD}$ increases while $W_{TED}$ reduces by the equation,

$$\frac{W_{BPD}}{W_{TED}} = \frac{E_{BPD}}{E_{TED}} \frac{1}{\tan \theta}$$

Eq.4.1

Where, $W$ is the elastic energy of the dislocation per unit growth length, $E$ is the elastic energy per unit length of dislocation line, $\theta$ is the offcut angle. The elastic energy per unit length of dislocation line for BPDs and TEDs was found to be almost the same, i.e., $E_{BPD} \sim E_{TED}$ and we get $W_{BPD} \gg W_{TED}$. As observed from the equation, $W_{BPD}$ energy increases with the decrease in offcut angle ($\theta$). Hence it is energetically favorable for a BPD to get converted into a TED during epitaxial growth on a low offcut substrate (fig.4.1). It has been shown that growing on low-offcut substrates significantly enhances BPD conversion (Tsuchida, Kamata, Izumi, Tawara, & Izumi, 2004). However, as one approaches close to on-axis < 1°, the possibility of 3C inclusions increases, along with
the possibility of step flow from the <1100> unintentional miscut direction leading to degradation of surface morphology (Tsuchida et al., 2004).

Various successful approaches to increasing the conversion efficiency have been reported including the modification of growth conditions such as:

i) Substrate pretreatment (etching) using molten potassium hydroxide (KOH) (Myers-Ward et al., 2009; Sumakeris et al., 2006), or using molten eutectic mixture (NaOH+KOH) (Song & Sudarshan, 2013)

ii) High temperature annealing of the substrates before growth (Mahadik et al., 2016; X. Zhang & Tsuchida, 2012)

iii) In situ hydrogen etching before epitaxy (Y. Sun, Feng, Zhang, Qian, & Kang, 2016)

iv) In situ growth interrupts (VanMil et al., 2008)

One common factor in all the above-mentioned processes is pretreatment of the substrates before epitaxial growth. Since the BPD density ranges from 500 cm$^{-2}$ to 800 cm$^{-2}$ in a 100mm (4”) substrate (Dow Corning®), it is difficult to produce 100% conversion at the substrate/epilayer interface. BPD conversion at the substrate/epilayer interface is very important for high reliability of SiC power devices as the BPDs buried in the epilayer can still be converted to SFs under current stress and these SFs will extend to the device active layer and degrade the device performance (Mahadik et al., 2012). Considering that ~500 BPDs/cm$^2$ are on the substrate surface and 99% of them are converted in to TEDs (Song & Sudarshan, 2013; Stahlbush et al., 2009; VanMil et al., 2009) producing ~5 BPDs/cm$^2$ on the epilayer surface, which is still a significant value adversely affecting the epitaxial wafer yield for device fabrication. Thus, 100%
conversion at the substrate/epilayer interface for 4° off oriented substrates is essential to achieve high yield and performance characteristics of SiC devices at the commercial level.

Earlier studies conducted by V.D.Wheeler et al. (Wheeler et al., 2011) have shown that BPD conversion on the epilayer show abrupt increase on low doped nitrogen films (< $10^{16}$ cm$^{-3}$) while high doped films show minimal BPD conversion. Recently, Song and Sudarshan (Song & Sudarshan, 2013) developed a “growth-etch-regrowth” technique which employs a well-controlled eutectic etching method to achieve a BPD-free epilayer with almost no surface degradation for 8° 4H-SiC epilayers. The etch pits are created when the eutectic chemical etchants (KOH-NaOH-MgO salt mixture) react with the SiC epilayer and selectively (anisotropically) etch the areas where the crystal defects are present (Sakwe, Müller, & Wellmann, 2006). Large etch pits are easier to obtain on low doped epilayers than on the high doped epilayers for the same etching conditions. This is due to the influence of high nitrogen concentration on the high-doped epilayers hindering the etching process (Sakwe et al., 2006). Zhang and Sudarshan (Z. Zhang & T. Sudarshan, 2005a) demonstrated that the lateral growth on the etch pits forces the BPDs to convert into TEDs, which implies the narrower the BPD etch pit, the easier it is for the lateral growth to force BPD conversion into TEDs within a thinner layer. This makes eutectic etching on low-doped epilayers a highly preferable method for BPD conversion and growing the active device epilayer on a low-doped buffer layer (fig. 4.2) is a prospective way to mitigate BPDs in the device layer.

Typically, high-doped epilayers (~$10^{18}$ cm$^{-3}$) are used as buffer layers due to their low on-resistance, and suitability as effective recombination layers. However, they are
not conducive for 100% BPD conversion (Wheeler et al., 2011). On the other hand, using a low-doped buffer layer, while good for BPD conversion, was thought to introduce unacceptably high on-resistance, since >10µm thick buffer layers are required (Wheeler et al., 2011). However, with improvements in buffer layer growth, layers as thin as 1.5µm (Song & Sudarshan, 2013), are possible to achieve 100% BPD conversion, giving a 10x improvement in on–resistance.

However, recombination rates, R, in low-doped buffer layers are much smaller than in high-doped buffer layers, since $R \propto N_d$ (Sze, 2008). The low doping density in the buffer layer, with corresponding diffusion lengths >10µm (Hatayama, Yano, Uraoka, & Fuyuki, 2006) means that for low-doped buffer layers, even if they are >10µm thick, recombination can still occur at the buffer layer/ SiC substrate interface, where BPDs are still present, causing stacking fault nucleation under bipolar current injection. These stacking faults can expand into the buffer layer, and eventually into the active device layer, rendering the original BPD-free buffer layer ineffective. Thus, low-doped buffer layers, even if they are grown thicker may not prevent stacking fault nucleation. This led us to growing a thin buffer layer (3 to 5µm) which reduces the total device series on-resistance significantly and then growing the $BPD$-$free$ recombination (high-doped) layer of considerably greater thickness ($\geq 10\mu m$) for all the minority carrier recombination to occur within the high-doped layer.
4.2. NOVEL COMPOSITE GROWTH STRUCTURE FOR BPD FREE ACTIVE DEVICE LAYERS:

In this chapter, we discuss about the BPD free 4°, 4H-SiC epitaxial growth method using the chlorinated Si precursor, DCS. We developed a composite approach to buffer layer growth, where we start with a thin low-doped buffer layer to achieve 100% BPD conversion, followed by a moderately thick higher doped recombination layer to ensure that all recombination occurs in a BPD-free region. If the thicknesses and doping of these two layers are carefully engineered, they will not introduce a significant addition to the on-resistance of the device, and will enable translation of BPD conversion technology into real devices. In other words, growing the active device epilayer on a low doped buffer layer is not detrimental to the device specific on-resistance while greatly advantageous for enhancing 100% BPD conversion (fig. 4.2).

Figure 4.2 Schematic of a 4H-SiC device template for fabricating P-i-N diodes or BJTs with specific on-resistance, $R_{\text{on-sp (total)}}$ (recombination+ buffer epilayers) = 0.47 mΩ-cm²

For example, a 4H-SiC BJT power device reported by Cree Inc.³ has a series on-resistance of 10.8 mΩ-cm². Since the 4H-SiC mobility is highly dependent on the free carrier concentration (~815 cm²V⁻¹s⁻¹ for ~10¹⁶ cm⁻³ and drops to ~250 cm²V⁻¹s⁻¹ for 10¹⁸ cm⁻³) (Schaffer, Negley, Irvine, & Palmour, 1994), low-doped buffer layers (n= 1x10¹⁶ cm⁻³, mobility $\mu$ ~815 cm²V⁻¹s⁻¹) with epilayer thickness (L) as low as 1.5 μm will add a
specific on-resistance of only 0.12 mΩ-cm² to the device, or ~1%. This was calculated using the formula:

\[ R_{on-sp} = \frac{\rho L}{nq\mu} \text{ per unit area (Ω-cm}^2\text{)} \]  (Eq.4.2)

For the buffer/recombination layer demonstrated by this method (fig.4.2), the total addition was <0.5 mΩ-cm², or <5%. This may be further reduced with optimization of the growth process, although 5% is within reasonable engineering tolerances for the thickness and doping, which will eventually determine the device variability. Moreover, the fact that for a typical recombination layer doping at 2x10¹⁷ cm⁻³, the mobility has already decreased from ~900cm²/Vs to < 250cm²/Vs shows that the recombination I has been greatly enhanced by the larger number of dopants through impurity scattering. In addition, R is enhanced, by the larger number of carriers. (n), as expected from the continuity equations:

\[ R = \beta np \]  (Eq.4.3)

Where, \( R \) = recombination rate (cm⁻³ s⁻¹), \( n \) and \( p \) are the carrier densities of electrons and holes (cm⁻³), \( \beta \) = proportionality constant.

With this in mind, for the first time 100% conversion of basal plane dislocations (BPDs) is reported on higher doped (recombination) epilayers (5x 10¹⁶ cm⁻³ to 1.6x10¹⁷ cm⁻³) by first growing a low n-doped (5x10¹⁵ cm⁻³ to 1x10¹⁶ cm⁻³) buffer epilayer on the 4° off 4H-SiC n+ substrate, and then mildly etching it by a modified eutectic mixture (MgO+NaOH+KOH). The etched epilayer with exposed etch pits (~5 µm to 7 µm) are subjected to regrowth (second epilayer) to serve as the recombination layer at high doping concentration under different C/Si ratios (0.6 to 1.8), and the underlying BPD to
TED conversion mechanism from the buffer epilayer to the recombination layer are studied in detail. The ideal growth condition to produce BPD free epilayers with minimum in-grown stacking fault (IGSF) density is reported.

4.3 EXPERIMENTAL DETAILS:

Epitaxial growth was carried out in a vertical hot-wall chimney reactor using Dichlorosilane (SiH\textsubscript{2}Cl\textsubscript{2}, DCS) and propane (C\textsubscript{3}H\textsubscript{8}) as precursors and H\textsubscript{2} as the carrier gas. The substrates were commercial 4H-SiC wafer with 4° offcut towards [11\bar{2}0]. The growth temperature and pressure were 1600°C and 80 Torr, respectively, with a C/Si ratio = 1.42. The growth rate was 20 µm/hr and the doping concentrations were found to be from 5x10\textsuperscript{15} cm\textsuperscript{-3} to 1x10\textsuperscript{16} cm\textsuperscript{-3} n-type for all the samples. After the above first buffer layer growth, the sample was etched by the modified (MgO-KOH–NaOH) eutectic mixture. Etch pits of 5-7 µm in length measured along the [11\bar{2}0] (step flow) direction were revealed at a temperature of 515°C for 13-17 min etching time with good controllability and reproducibility. The recombination layers at different C/Si ratios (0.6 to 1.8) were subsequently grown on the eutectic etched samples. After the above regrowth, the recombination layer was etched again by KOH etching at 550°C to obtain etch pits of ~10 µm size to examine the defect evolution. Since the recombination layer was used only to observe the defect conversion and not to preserve surface roughness, it was etched by traditional KOH etching method. Fig.4.3. shows the schematic of the steps involved for obtaining BPD free epilayers by growth-etch-regrowth method. The defects were observed using Nomarski optical microscopy (NOM) at the same surface locations on both epilayers. Atomic force microscopy (AFM, Digital Instruments Dimension 3100, tapping mode) was employed to study the surface morphology and shape of the BPD etch
pits. The thickness of the epilayers were measured using the Fourier transform infrared reflectance (FTIR) (Sunkari et al., 2005). Net doping concentrations of the epilayers were measured by mercury probe Capacitance-Voltage method (Kim & Davis, 1986).

Figure 4.3 Steps to produce 100% BPD conversion on high doped epilayers (Balachandran, Sudarshan, & Chandrashekhar, 2017)

4.4 BUFFER EPILAYER GROWTH AND EUTECTIC ETCHING:

Fig. 4.4(a) shows the specific on-resistance and fig. 4.4(b) shows the BPD and IGSF densities calculated after the first epilayer growth for a growth duration of 15 min at a fixed C/Si ratio =1.42 with 0.1 sccm intentional N₂ flow to obtain n-doping concentration in the epilayers. All the epilayers in fig.4.5 (a) to (d) showed a similar thickness of ~5 µm. C/Si ratio of 1.42 was chosen for the first buffer epilayer growth as it is the best condition to obtain specular surface morphology with minimum BPD propagation by maximum spontaneous BPD conversion during the buffer layer growth at a reasonable growth rate 20 µm/hr (Song, Chandrashekhar, & Sudarshan, 2015). By intentionally adding less N₂ (0.1 sccm) at this condition gives a net doping concentration ranging between (5x10¹⁵ cm⁻³ to 1x10¹⁶ cm⁻³) with a specific on-resistance <0.9 mΩ/cm²
(fig.4.4 (a)) for all the samples and also helps in the eutectic etching to etch the epilayer faster (< 15 min) due to the low doping concentration compared to the substrate.

![Figure 4.4](image-url) Buffer epilayer (a) Theoretical series on resistance w.r.t doping concentration and (b) BPD and IGSF densities vs. net doping concentration

Fig.4.5 shows typical etch pits on the first buffer epilayers from eutectic etching. The threading screw dislocations (TSDs) have large hexagonal etch pits with a tip (lowest position within the etch pit) at the down-step side; TEDs have smaller hexagonal pits with a tip at the down-step side, and BPDs are shell-like shaped with a tip at the up-step side (see Fig.4.6a). All the epilayers (fig.4.5 (a) to (d)) were etched for a duration ranging from 10 min to 13 min. The surface roughness of the first buffer epilayers had nearly no change before and after the eutectic etching (~0.5 nm RMS change observed from AFM), thus preserving the epilayer surface morphology for the subsequent growth.
Figure 4.5 (a) to (d) Nomarski images of the defects seen after eutectic etching of first buffer epilayers grown at same C/Si ratio for 15 min growth duration.

AFM scanning was done on the BPD etch pits seen on the eutectically etched epilayers. All the epilayers showed similar BPD structures with very narrow sector angle (4.5°~5°) calculated from the sector shaped (AOB in fig.4.6 (a)) basal plane (0001) exposed after the controlled and anisotropic eutectic etching. The narrow opening of the sector plane enables lateral growth in the BPD and converts it into a TED at the interface during the subsequent recombination layer growth (Song & Sudarshan, 2013).
Figure 4.6 (a) Typical AFM image of the BPDs seen on the buffer epilayers, (b) Schematic showing influence of large sector and narrow sector opening of BPD etch pits for propagation and conversion.

4.5 RECOMBINATION LAYER GROWTH:

The etched buffer layers, after mapping of the delineated defects, were subjected to regrowth at different C/Si ratios from 0.6 to 1.8 by changing the flow rate of propane while keeping the flow of DCS constant. N$_2$ flow was increased to 15 sccm for the recombination layer growth in order to obtain higher doping concentration of the epilayers as well as to examine the influence of intentional doping on BPD conversion. The growth duration was increased to 30 min to produce thicker recombination layers. From fig.4.7 (a) it is observed that the growth rate increases and the net doping concentration reduces with the increase in C/Si ratio due to the site competition epitaxy, which is in accordance to previously reported results with DCS.$^{29}$
Figure 4.7 Recombination layer (a) thickness and net doping concentration w.r.t C/Si ratio, (b) BPD and IGSF density w.r.t net doping concentration (trend lines shown are guide to the eyes)

The recombination layers were KOH etched to reveal the defects on the epilayer surface, as shown in fig. 4.8(a) to (d). The Nomarski images shown in fig.4.8 (a) to (d) were taken at positions where there were previously BPDs on the buffer epilayers (shown in fig. 4.5(a) to (d)) and indicate the location of the converted TEDs on the corresponding recombination layers after regrowth. All the epilayers showed 100% BPD to TED conversion rate from the buffer layer with the only exception at C/Si = 0.6.

At C/Si = 0.6, although all the BPDs from the buffer epilayer got converted into TEDs at the buffer-recombination layer interface, a new BPD was generated during the recombination layer growth thus reducing the net BPD conversion ratio rate (fig.4.9). This is similar to the observations of V.D.Wheeler et al. (Wheeler et al., 2011) in which it is reported that an abrupt increase in BPDs is reported at high nitrogen concentrations.
Figure 4.8 (a) to (d) NOM images of converted BPDs to TEDs seen on the recombination layer at the corresponding buffer epilayer positions (fig.4.5 (a) to (d)) at different C/Si ratios after KOH etching.

Figure 4.9 Net BPD to TED conversion ratio from buffer to recombination layer w.r.t. C/Si ratios (Balachandran et al., 2017)
The reason for the formation of a new BPD on the recombination layer at C/Si = 0.6 is explained below. The difference in the doping between the buffer layer and recombination layer is maximum at C/Si = 0.6. This high N doping concentration of the second layer compared to the low doping in the buffer layer induces strain in the recombination layer. A threading dislocation segment in the buffer epilayer experiences a force due to the lattice misfit which is balanced by dislocation line tension. If the misfit induced force exceeds the force due to dislocation line tension, formation of a misfit dislocation is favorable (Kallinger et al., 2012). Ohtani et al. (Ohtani, Katsuno, Takahashi, Yashiro, & Kanaya, 1999) have reported that nitrogen doping in the epilayer at high concentrations causes the epilayer step trains to become unstable: the equidistant step trains are transformed into meandering macrosteps by nitrogen adsorption on the growing crystal surface. The step flow growth balance between micro (vertical) and macrosteps (lateral growth) become unstable and this phenomenon is said to exert more force on the dislocation line leading to the formation of a new BPD in the high-doped (~5.8x10^{17} cm^{-3}) recombination layer.

Another interesting result was observed at C/S ratio 1.0, where the BPD intersecting the etched buffer epilayer surface converts into a TED in the recombination layer, but the conversion point is not at the buffer-recombination layer interface. The BPD-TED conversion point is shifted by a certain distance along the up-step direction (Fig. 4.8(b)) which is referred to as a ‘TED glide’ (Abadier, Song, Sudarshan, Picard, & Skowrons, 2015). This TED glide indicates that the BPD to TED conversion point is located beneath the buffer-recombination layer interface. The glide distance (~50 µm measured from NOM) which when multiplied with the offcut (50 µm x tan (4°)) comes to
~3.5 µm. This implies that the BPD conversion point is shifted 3.5 µm below the buffer epilayer interface along the dislocation line (fig.4.10) (USC Technology ID: 1252). The TED glide also indicates a decrease in the total dislocation energy by decreasing the dislocation line length.

As reported by Abadier et al. (Abadier et al., 2015), the above TED glide mechanism occurs in steps as follows; the BPD glides along the basal plane and its dislocation line aligns with the [11̅20] direction. This causes the BPD partials to constrict and the constricted BPD gets converted into a local screw dislocation (Chung et al., 2011). Consequently, the local screw dislocation emerges as a TED which is pulled by its line tension and glides towards the up-step direction. The shift due to this TED glide is always towards the up-step direction (Abadier et al., 2015). The TED glide is observed for BPDs that are screw dislocations, for the mixed type BPDs the conversion point will be at the epilayer/substrate interface (Chung et al., 2011). For all other recombination layers grown at different C/Si ratios the conversion point was at the interface of the buffer-recombination layer. This is identified by the location of the BPD depression on the buffer epilayer overlapping with the TED conversion point seen on recombination layer after KOH etching.
The ideal growth condition for 100% BPD conversion and minimum IGSF density was observed when the C/Si ratio was maintained the same for both the first buffer and the second recombination layers (fig.4.7(b)). The doping difference between two epilayers at this condition is found to be the minimum (Brillson et al., 2002). This plays an important role in minimizing the IGSF formation on the recombination layer as doping induced lattice misfits are the common reason for the formation of stacking faults in the epilayer due to their low energy of formation (Huh et al., 2004; Kallinger et al., 2012).

Since the doping difference was less and C/Si ratio was maintained the same (C/Si =1.42) on both epilayers, the surface step morphology was able to be preserved on both the epilayers. The effect of the growth morphology on the BPD conversion efficiency implies that the step structure around the emergence point of the BPD plays an important role in the conversion (Jacobson et al., 2003). By maintaining same C/Si =1.42 for the buffer and recombination layers, the step roughness and step bunching is preserved for both the epilayers and the ideal condition for growing BPD free epilayer with minimum IGSF density is achieved at this C/Si ratio.

In-grown stacking faults (IGSFs) observed on the buffer epilayer and the recombination layer show typical inverse relationship with the BPD density (fig. 4.4(b) & 4.7(b). In the results reported in this chapter, the low doped buffer epilayer on high doped substrate experiences compressive strain and the high doped recombination layer on the low doped buffer layer experiences tensile strain in the crystal lattice. Though the origin of IGSFs are not exactly known, doping concentration induced lattice misfit (strain) also can be a reason for some of these stacking faults (Kallinger et al., 2012). The
experimental reports (Huh et al., 2004; Jacobson et al., 2003) suggest that the relaxation of homoepitaxial layers is linked to the formation of stacking faults. This is very likely due to the low stacking fault energy in 4H-SiC of 3–15 mJ/m² (Hong et al., 2000). Jacobson et al. (Jacobson et al., 2003) have shown that stacking faults occur in low N-doped epilayers (~3x10^{15} cm^{-3}) grown on highly N-doped substrates and they propagate up to 30µm thickness. These results are consistent with results presented in this study.

In summary, a unique composite approach to grow BPD-free active device layers with doping concentration as high as $1.6 \times 10^{17}$ cm$^{-3}$ on low-doped buffer layers ($1 \times 10^{16}$ cm$^{-3}$) is reported. The innovative concept of growing the active device epilayer on a low doped buffer epilayer to achieve 100% BPD conversion rate and thereby improving the epitaxial wafer yield is introduced and demonstrated. A C/Si ratio dependence on BPD conversion rate is demonstrated on intentionally doped recombination layers and the BPD-TED conversion point was maintained at or below the growth interface for a wide range of C/Si = 1 to 1.8. The ideal condition to obtain 100% BPD conversion with minimum IGSF density has been found when both buffer and recombination layer growths are carried at the same C/Si ratio (1.42), exhibiting minimum doping difference (minimum lattice strain) between the two epilayers. The study showed that the strain related to the difference in doping concentration between the buffer and recombination layers strongly influence the net BPD conversion rate and also the BPD-TED conversion point between the two epilayers. The creation of BPD-free recombination layer with high doping is a significant technological improvement in the field of SiC epitaxy for producing robust, forward voltage drift free bipolar devices.
CHAPTER 5

INTEGRATED EPITAXIAL GRAPHENE GROWTH ON 4H-SiC USING TFS

5.1 INTRODUCTION:

Graphene is a 2-dimensional nano material consisting of a single layer of carbon atoms, bonded together in a hexagonal honeycomb lattice (sp$^2$ bonding), that has been isolated from graphite (sp$^3$ bonding). The carbon-carbon distance is 1.42 Å and the lattice constant is 2.46 Å (Fig.5.0 (a) and (b)). The definition “graphene” is not only used for single layers, but also for bilayer, few-layer (three to <10 layers) and multi-layer graphene (>10 mono layers) (Geim & Novoselov, 2007). Graphene has an extremely high optical transparency, high electric and thermal conductivity, single-molecule gas detection sensitivity, mechanical toughness (high Young’s modulus), and high electron mobility (Yazdi, Iakimov, & Yakimova, 2016). It is a semi-metal with linear energy dispersion around the Dirac point dispersion (Figure 5.0 (c)) due to its two-dimensional honeycomb structure (Novoselov et al., 2005). This makes the material behave differently from the conventional semiconductors and provides opportunity in revolutionary applications, such as RF devices, sensors and high precision metrology (Yazdi et al., 2016).

1 Balachandran, A, Chava, V N, Letton, J, Chandrashekhar MVS. To be submitted to Journal of Applied Physics.
The earliest ways to synthesize graphene, an emerging nanomaterial, were crude (e.g. exfoliation of bulk graphite), and could only produce single layers of small area <100um in size (Geim & Novoselov, 2007). Subsequently, several other techniques have been perfected for graphene synthesis by reduction of graphite oxide, chemical vapor deposition on transition metal/metal carbide substrates (Reina et al., 2008) and Si sublimation of SiC (Daas et al., 2012). The best quality material for nano-electronics has been obtained systematically through the solid-state decomposition of the surface of commercial SiC substrates (Lee et al., 2014).

Figure.5.1 (a) Bravais lattice of the graphene; (b) \(\sigma\) and \(\pi\) bonds in graphene; (c) graphene \(\pi\)- and \(\pi^*\)-band structure (Neto, Guinea, Peres, Novoselov, & Geim, 2009)

Growth of graphene by the sublimation method is nowadays typically performed in a furnace with an Ar overpressure to improve the uniformity of the epitaxial graphene (EG) layer (Yazdi et al., 2016). The main advantages of epitaxial graphene on SiC are that no transfer is needed for device processing and size of the graphene sheet can be as
large as the substrate, which is another benefit for device processing. SiC as a polar material has two terminations, called the Si-face (polar), corresponding to the (0001) polar surface, and the C face (000\bar{1}). For both the Si face and C face, the growth mechanism of graphene layers is driven by the same physical process: sublimation of Si at elevated temperatures at a rate much faster than C due to its higher vapor pressure (Lilov, 1993). The remaining C forms a graphene film on the surface. The surface reconstructions and growth kinetics for Si and C faces are different, resulting in different graphene growth rates, growth morphologies and electronic properties (Jernigan et al., 2009; Van Bommel, Crombeen, & Van Tooren, 1975). The underlying SiC substrate, having the space group \(P6_3mc\) with a hexagonal lattice, provides excellent symmetry matching for graphene epitaxy. Graphene grown in this manner is referred to as “epitaxial graphene” (Jernigan et al., 2009). Sublimation method is a promising technique for quality graphene growth and shows interesting physical characteristics such as ballistic transport in nanoribbons (Baringhaus et al., 2013), high frequency transistors (Lin et al., 2010), quantum Hall resistance standard for metrology (Tzalenchuk et al., 2010).

In this technique, the substrate is heated to high temperatures \(~1300-1650^\circ C\), either in a vacuum, or in an inert environment such as Argon. The Si vapor pressure at the surface, being higher than that of carbon, leads to the loss of Si from the surface, and the formation of a C-rich layer on the SiC surface according to reaction 1 in table 5.1:

\[
\text{SiC(s)} \rightarrow \text{Si(g)} + \text{C(s)}
\]

The C-rich layer produced according to reaction 1 in table 5.1 then rearrange itself into a perfect graphene crystal, if enough time is available for the bonds to form. The thickness is controlled by changing the temperature and time, as well as the choice of SiC
substrate orientation (Dresselhaus & Dresselhaus, 1981). It was then shown that the best quality material could be obtained by slowing down the growth rate (Drowart, De Maria, & Inghram, 1958), allowing the C-rich layer to form complete C-C bonds leading to a good quality graphene crystal. If the formation rate of the C-rich layer is too fast, a good quality crystal cannot be formed due to random and uncorrelated nucleation of graphene layers (Hupalo, Conrad, & Tringides, 2009).

While this conventional graphene growth has focused mainly on producing 1–2 atomic monolayers (ML) of epitaxial graphene, thicker layers (>100 ML) may also find interest in energy applications such as engineered carbon electrodes, emission sensing (Wentrcek, Wood, & Wise, 1976), hydrogen storage and fuel cells (Bessel, Laubernds, Rodriguez, & Baker, 2001), etc., where a greater accessible surface area is needed. Graphene/SiC heterojunctions are used and have potential applications in field effect transistors (FET), radio frequency (RF) transistors, integrated circuits (IC), sensors and UV detectors.

Previous work from our group has reported that the growth of multilayer graphene films MUST be mediated by the defects (Daas et al., 2012) in the growing epitaxial graphene film (Figure 5.2), as a perfect graphene crystal cannot allow further Si-atoms to diffuse through it and out of the growth region, a necessary step for the formation of a subsequent C-rich layer. In other words, to grow thick layers, defects must be present, and therefore, thicker layers contain a greater density of defects (Daas et al., 2012).
Figure 5.2 (a) The silicon atom has a much larger diameter than the atomic gap in a graphene layer. Si-loss can only occur through defects (Daas et al., 2012). (b) Schematic of defects in graphene, and how they mediate molecular in-diffusion for doping and Si-adatom out-diffusion for growth of EG (Shetu et al., 2013)

Table 5.1 Free formation energy (kcal/mol) for SiC dissociation and SiF₄ reactions (TRana et al., 2013)

<table>
<thead>
<tr>
<th>Reaction</th>
<th>1800K</th>
<th>1900K</th>
<th>2000K</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dissociation and evaporation reactions</strong></td>
<td>Gibbs Free Energy (kcal/mol)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SiC(s) → Si(g) + C(s)</td>
<td>58.19</td>
<td>54.60</td>
</tr>
<tr>
<td>1a</td>
<td>SiC(s) → Si(l) + C(s)</td>
<td>12.90</td>
<td>12.00</td>
</tr>
<tr>
<td>1b</td>
<td>Si(l) → Si (g)</td>
<td>45.29</td>
<td>42.59</td>
</tr>
<tr>
<td><strong>SiF₄ reactions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Si (l) + SiF₄(g) → 2SiF₂ (g)</td>
<td>19.69</td>
<td>15.93</td>
</tr>
<tr>
<td>3</td>
<td>C(s)+1/4 SiF₄→CF+1/4 Si(g)</td>
<td>107.83</td>
<td>103.65</td>
</tr>
<tr>
<td>4</td>
<td>C(s)+1/2 SiF₄→CF₂+1/2 Si(g)</td>
<td>128.23</td>
<td>124.16</td>
</tr>
<tr>
<td>5</td>
<td>4C(s) + 3SiF₄ → 4CF₃ + 3Si(g)</td>
<td>184.63</td>
<td>180.62</td>
</tr>
<tr>
<td>6</td>
<td>C(s) + SiF₄ → CF₄ + Si(g)</td>
<td>211.04</td>
<td>206.36</td>
</tr>
<tr>
<td>7</td>
<td>2C(s)+1/2SiF₄→C₂F₂+1/2Si(g)</td>
<td>175.24</td>
<td>171.05</td>
</tr>
</tbody>
</table>

We demonstrate in this chapter that by changing the Si loss mechanism from reaction (1) to reaction (2) (Table 5.1) we can obtain high quality multilayer EG.
This technique relies on a fluoride enhanced chemically accelerated Si removal mechanism from the SiC surface, which also changes the stacking/defect profile of graphene grown on Si-face of 4H-SiC.

5.2 PREVIOUS WORK ON EPITAXIAL GRAPHENE (EG) GROWTH USING TFS:

In the previous research, our group demonstrated that SiF₄ (tetrafluorosilane, TFS) can be used as a Si precursor to grow high quality SiC epitaxial films (T Rana et al., 2012; T. A. Rana, 2013). It was also demonstrated that SiF₄ can be used as a SiC etchant when it is used in a H₂ ambient (T Rana et al., 2013). It was reported that in a SiF₄+H₂ environment, H₂ removes C and SiF₄ removes Si from the surface and performs SiC etching by removing both components (C and Si). It was also demonstrated that this technique of etching can be exploited to grow graphene by replacing H₂ with an inert (Argon) carrier gas to selectively etch Si from the SiC surface (Tawhid Rana, Chandrashekhar, Daniels, & Sudarshan, 2015). The novel growth mechanism of epitaxial graphene formation on SiC using TFS is explained below:

When SiC is heated above 1410°C in any inert environment (e.g., Ar, He or vacuum), Si dissociates (reaction 1 in Table 5.1), forms liquid/gas (reaction 1a,1b in Table 5.1) and eventually evaporates leaving carbon layer(s) on the surface (Kumagawa, Kuwabara, & Yamada, 1969). The conventional sublimation process is dependent on the removal of Si from the surface by thermal evaporation reactions. This is a slow process since liquid Si on the surface must be removed as Si gas by the slow self-evaporation process, without any control over removing Si from the surface efficiently.

To grow graphene in a more predictable manner with greater controllability, a controllable Si removal process by some precursor gas is essential. SiF₄ has a very strong
Si–F bond, making thermal decomposition difficult below 2000 °C (Collins, 2000). However, SiF$_4$ is also known for forming SiF$_2$(g) by reacting with solid Si above 1150°C (Timms, Kent, Ehlert, & Margrave, 1965) by the following chemical reaction (reaction 2 in table 5.1):

$$\text{Si (l)} + \text{SiF}_4(g) \rightarrow 2\text{SiF}_2(g)$$

SiF$_4$ removes Si(l) from the SiC surface at a temperature of ~1400 °C forming SiF$_2$ gas. Si removal from the surface is more favorable ($\Delta G = 15.9$ kcal=mol, reaction 2 in Table 5.1) by using SiF$_4$ compared to the thermal evaporation reaction ($\Delta G = 42.6$ kcal=mol, reaction 1b in Table 5.1). On the other hand, C removal by SiF$_4$ gas is considerably difficult due to much higher free energy for the carbon removal reactions ($\Delta G > 100$ kcal/mol, reactions 3–7 in Table 5.1). Ar alone does not remove Si from the surface as it is not reactive with Si or SiC. Hence, treatment of SiC at higher temperatures with SiF$_4$ in an inert environment (e.g., Ar) is essentially a silicon selective etching process which can be exploited to enhance the epitaxial growth of graphene. The chemical process of Si removal by SiF$_4$ and formation of graphene is shown in Fig.5.3 (Tawhid Rana et al., 2015).

To perform a qualitative and quantitative analysis on the TFS grown graphene samples, a micro-Raman setup with laser excitation wavelength at 632nm and a spot size of ~2µm was used. The Raman system was calibrated using the known Si peak at 520.7cm$^{-1}$. Reference blank substrate spectra were scaled appropriately and subtracted from the graphene spectra to show only the graphene peaks (Tawhid Rana et al., 2015).
Figure 5.3 Mechanism of epitaxial graphene growth using SiF$_4$. In this process, Si is removed from the surface (steps I–IV). I) Dissociation and Si(l) formation at temperatures $>1400^\circ$C. II), III) Si is removed efficiently by SiF$_4$ as SiF$_2$ gas. IV) Residual C on the surface forms graphene layers at temperatures 1400 °C or above (Tawhid Rana et al., 2015)

The Raman spectrum of graphene has three peaks, the disorder induced D-peak at $\sim 1350 \text{cm}^{-1}$, the G-peak intrinsic to graphene/graphite at $\sim 1580 \text{cm}^{-1}$, and the second order 2D peak, which is present in ideal graphene. At 1300°C, no 2D peak was observed, showing no graphene growth (Tawhid Rana et al., 2015). For all other conditions, the presence of the above-mentioned peaks was observed, an indication of the presence of graphene. Raman analysis of SiC samples treated at 1600°C are shown for 5.4 a) treated substrate with only Ar (10 slm) for 60 min, and b) SiF$_4$ treated substrates- Ar (10 slm) + SiF$_4$ (10 sccm) (Tawhid Rana et al., 2015) with similar growth conditions (temperature: 1600 °C, pressure: 300 Torr). Surface pretreatment using only Ar (1600 °C, 60 min) did not show any obvious graphene G-peak and no obvious difference was found from the original substrate (fig. 5.4(a)). On the other hand, for the samples where 10 sccm of SiF$_4$
is added to the Ar gas stream during the growth process, a sharp G-peak emerged (fig. 5.4(b)).

Figure 5.4 Comparison of as-taken Raman spectra (without substrate subtraction) of on-axis 4H-SiC substrates treated at 1600°C. a) For 1 hour at 10 slm of Ar flow rates without SiF4 and b) for 1 hour at 10 slm of Ar with a 10 sccm of SiF4 (Tawhid Rana et al., 2015).

Growth temperatures were varied from 1300 to 1600 °C at 100 °C intervals while keeping the Ar and SiF4 flow rates at 10 slm and 10 sccm respectively. No observable G-peak was found for the graphene growth at 1300°C. A clear G-peak was observed when temperature was increased to 1400°C. High D/G ratio (~1.1) at this temperature indicates higher disorder in graphene layers (fig. 5.5(a)). However, a lower D/G ratio of ~0.2 was found for the grown layers at a temperature of 1600 °C indicating higher quality of the graphene material with higher sp2 content (fig. 5.5(a)) (Tawhid Rana et al., 2015). It is generally known that higher temperature leads to higher C–C bond formation and minimizes the grain boundaries (i.e., ordered graphitic phase) (Dresselhaus & Dresselhaus, 1981).
Figure 5.5 (a) Temperature dependence of Raman ratio of integrated peak intensities of the D peak to the G peak ($I_D/I_G$) indicative of defect density reduction in higher temperature growth, (b) As temperature increases, the Raman 2D FWHM reduces towards higher carrier mobility for these samples.

The 2D peak in EG Raman spectrum is an indicator of the stacking order of the material. All graphene samples exhibit a symmetric 2D peak that could fit well with a single Lorentzian instead of split-peak seen for Bernal stacked graphene/graphite (Terrones et al., 2010). Ideal Bernal stacked graphite has a split asymmetric 2D peak, with each sub-peak corresponding AB stacking responsible for graphene’s linear electron dispersion. This shows that these films are not AB Bernal-stacked as seen usually with Si-face epitaxial graphene, but instead have turbostratic, or mixed stacking.

As a continuation of the previous work, in this chapter, we have proven the novel concept of EG/n-SiC hybrid Schottky device structures by epitaxial graphene growth using TFS. Epitaxial graphene growth process optimization and characterization, device fabrication, and characterization results as a diode and UV-photodiode are also discussed in detail.
5.3 TEMPERATURE RAMP DOWN STUDY OF EG GROWTH USING TFS:

As explained above, previous work on epitaxial graphene growth using TFS mainly focused on optimizing the growth conditions to obtain high quality epitaxial graphene. The effect of stepped surfaces (4° or 8° substrates/epilayers) on the epitaxial graphene morphology, which is important for integrating graphene with SiC epi-growth was yet to be investigated. In this work, a temperature ramp down study on the EG growth was performed for three different ramp down times such as 15 min (~56°C/min), 30 min (~28°C/min) and 60 min (~14°C/min) to understand the cooling effect (thermal stress) on the growth morphology of epitaxial graphene grown on different offcut 4H-SiC substrates and epilayers.

**Experimental details:**

Nitrogen doped (~10^{19} cm^{-3}), chemical-mechanical polished (CMP), commercial 4H-SiC substrates with various off cuts (~0°, 4° and 8°) and 8° epilayers were used in this study. Samples were cleaned by standard RCA cleaning method. All the graphene epitaxial growths were performed on the Si-face of the substrates/epilayers in a home built vertical hot-wall CVD reactor. Ultra high purity (99.9999%) Ar gas was used as the carrier gas. The substrate was first baked at 750°C in vacuum. Then 6 slm Ar carrier gas flow was initiated to attain the growth pressure (300 torr). The growth temperature (1600°C) was reached in ~20 minutes, at which point 0.1% SiF_4 flow (Tetrafluorosilane or TFS) was initiated for the graphene growth for a duration of 10 min. Finally, the temperature was ramped down from the growth temperature to 750°C. Three different experiments with three ramp down times such as 15 min (~56°C/min), 30 min (~28°C/min) and 60 min (~14°C/min) were performed. No pre-growth hydrogen etch was
performed. The surface morphology of these films was characterized by atomic force microscopy (AFM) after each growth. Tapping mode was used to scan 5µm × 5µm window at several positions on a sample.

After each growth, X-ray photoelectron spectroscopy (XPS) measurements were conducted using a Kratos AXIS Ultra DLD XPS system equipped with a monochromatic Al Kα source in the XPS facility at USC. The energy scale system was calibrated using an Au foil with Au(4f) scanned Al radiation and a Cu foil with Cu(2p) scanned for Mg radiation resulting in a difference of 1081.70 ± 0.025eV between these two peaks. The binding energy is calibrated using an Ag foil with Ag(3d5/2) set at 368.21 ± 0.025eV monochromatic Al X-ray source. The monochromatic Al Kα source was operated at 15 keV and 150 W. The pass energy was fixed at 40 eV detailed scans. A charge neutralizer was used to compensate the surface charge. The graphene film thickness was extracted from the XPS spectrum (Cumpson, 2000). For films <~10ML thick, the C(1s) peak for graphene was referenced to the C(1s) peak for the SiC substrate, whereas for films >10ML, the C(1s) peak was referenced to the Si(2p) peak for the SiC substrate. FTIR reflectivity measurements were performed using a Galaxy Series FTIR-5000 spectrometer in an incidence angle of 40° over the wavelength 2.5µm to 25µm using a blank SiC substrate as the reference.
Characterization results of epitaxial graphene/4H-SiC:

The characterization results of EG/SiC samples grown at different ramp down rates are discussed below:

**Atomic force microscopy (AFM):**

The surface morphology of the EG samples are analyzed using AFM. Fig.5.6 and 5.7 show the AFM height and phase images of EG grown on different offcuts of 4H-SiC at the respective ramp down rates. The surface roughness values for EG grown on different offcuts is found to vary for different cooling rates (Fig. 5.6). Surface roughness for EG grown on on-axis substrates does not show obvious dependence on the cooling rates. Whereas for EG on 8° substrates the best surface morphology is seen for the slowest cooling rate (14°C/min). On the other hand, the phase images show interesting features on the EG surfaces grown on different offcuts for different cooling rates. It is seen that the EG growth on on-axis substrates exhibit uniform phase images (thick graphene growth seen only at the step edges) irrespective of the cooling rates. For EG grown on 4° and 8° offcuts, the phase images shown thick graphene nucleation, termed as ‘cracking’ at random areas on the surface at different ramp down rates. The cracking is observed to be uniform at the step edges for the slowest ramp down rate (14°C/min) for both 4° and 8° substrates and 8° epilayers.
Figure 5.6 AFM height images (5 x 5 μm²) of epitaxial graphene films grown on different offcuts of 4H-SiC substrates

Figure 5.7 AFM phase images (5 x 5 μm²) of epitaxial graphene films grown on different offcuts of 4H-SiC substrates
The cracking phenomenon observed on the EG grown on off-oriented surfaces is due to the increased kink density on the stepped surfaces (J. Robinson et al., 2009) which also contributes to the increase in EG surface roughness. The crack densities seen for different ramp down rates is found to affect the EG-SiC interface properties which in turn may have a strong influence on the barrier height inhomogeneity on the EG/n-SiC Schottky junction.

**X-ray Photoelectron Spectroscopy (XPS):**

The XPS results for EG grown on 4° offcut substrates at different ramp down rates are presented here. The thickness calculations of the EG layers estimated using XPS are described as follows. Using XPS, we measured the C(1s) and Si(2p) peaks both on the EG samples, in the normal (10°) beam incidence angle. For EG on Si face, the C (1s) XPS spectra consists of three components, one SiC bulk component located at 283.7 ± 0.08 eV, one is from the graphene over layer at 284.4eV, while the other is broad and weak at 285.5 eV arising from C-C bonding in a $6\sqrt{3} \times 6\sqrt{3}$ interfacial buffer layer (fig.5.8) (D. Sun et al., 2010). Thus, to estimate the EG thickness after the interfacial buffer layer, graphene overlayer peak intensity was normalized to the peak intensity arising from SiC bulk component. For thicker layers, the peak due to SiC bulk component disappears from the EG C (1s) spectra, while the Si(2p) peak is still present.
Figure 5.8 XPS C(1s) spectrum of ~14 ML EG showing C(1s) graphene component and Si(2p) SiC bulk component (not obvious because of the thickness > 10 ML)

The C(1s) peak was normalized to the Si(2p) peak for thicker layers, from which the thickness was determined using the formula given below (Eq.5.1):

\[
\ln \left( \frac{I_G}{S_G} \right) = \frac{-d}{\lambda \cos \theta}
\]

(Eq.5.1)

where, \(I_G\) and \(I_S\) are the peak area intensities of C(1s) and Si(2p) peaks of the graphene over layer component for the EG/SiC samples, \(S_G\) and \(S_S\) are the relative sensitivity factors corresponding to the graphene sample and SiC substrate, \(\lambda\) is the inelastic mean free path at that kinetic energy when the intensity is in peak (here K.E is 1202 eV and hence \(\lambda\) is 2.1 nm), \(\theta\) is the emission angle (measured with respect to the surface normal) and \(d\) is the thickness of the graphene layer, a monolayer graphene thickness of 0.33 nm is used for the thickness calculation (Ohta, Bartelt, Nie, Thürmer, & Kellogg, 2010).
Figure 5.9 XPS data (Gaussian curve fitted) and thicknesses of EG grown on 4° offcuts for ramp down rates (a) 14°C/min, (b) 28°C/min and (c) 56°C/min

From the XPS thickness analysis (fig.5.9), it is observed that the thickness of EG layers increased with slow cooling rates implying a slow reconstruction of EG layers with increased nucleation site (crack) densities. The thickness values also agree with the surface roughness values seen in fig.5.6.

**Fourier Transform Infrared Spectroscopy (FTIR):**

The XPS measurement is a reliable technique to measure thickness up to ~30 to 40 ML. For EG thicker than 40 ML, it is difficult to differentiate the C(1s) and Si (2p) peaks from the data. In order to extract the thickness of the EG layers (>35 ML) Fourier Transform Infrared Spectroscopy (FTIR) can be used. This relies on the fact that more conductive graphene layers are more reflective in the infrared (Daas, Daniels, Sudarshan, & Chandrashekhar, 2011). Also, thicker layers are more reflective in the infrared spectrum (fig.5.10). Thus, from a reflectance spectrum, the conductivity can be determined (Daas et al., 2011). For thick films, which are electrically neutral (far from the substrate>>1ML screening length in graphene (Y. Sun et al., 2016), the carrier concentration, n, is known. Thus, if the carrier mobility, μ, can be estimated using Raman/ Hall measurements (J. A. Robinson et al., 2009) and the carrier concentration in the EG layers can be estimated from Hall measurements, the total thickness in ML, N, can be estimated from the relationship:
Therefore, the lone fitting parameter is $N$, enabling reasonable confidence in the measurements. Furthermore, for layers $<30$ML, XPS can be used to correlate the results obtained from FTIR, with excellent agreement.

![FTIR spectra of EG grown on 4° substrates at different ramp down rates](image)

Figure 5.10 FTIR spectra of EG grown on 4° substrates at different ramp down rates

We considered the reflectance at a low value of $500\text{cm}^{-1}$ to minimize apparent decrease in reflectance for non-specular reflections, damping from carrier scattering, and increase in conductivity from interband transitions at higher frequencies (Daas et al., 2011).

Thus, we estimated the differential reflectance of graphene as we vary the no of layers with this approach for a $\mu \approx 700\text{cm}^2/\text{Vs}$ (from Hall measurements) using the reflectance equation:
\[
R = \frac{\left(\sqrt{\frac{\varepsilon_1 \varepsilon_2 \varepsilon_0}{\alpha}} + \sqrt{\varepsilon_1 N \sigma(\omega) x \cos \phi} \frac{-\varepsilon_1 \varepsilon_0}{c} \right)^2}{\left(\sqrt{\frac{\varepsilon_1 \varepsilon_2 \varepsilon_0}{\alpha}} + \sqrt{\varepsilon_1 N \sigma(\omega) x \cos \phi} \frac{+\varepsilon_1 \varepsilon_0}{c} \right)^2} 
\]

(Eq. 5.3)

where, \(\alpha = \sqrt{\frac{1 - (n_1 \sin \theta)^2}{\cos \theta}}\), \(\theta\) is the angle of incidence of the IR beam = 40°, \(n_1\) and \(n_2\) are the refractive index of air and SiC, respectively, \(\sigma(\omega)\) is the total conductivity, and \(\varepsilon_0\) is the free-space permittivity (\(~8.854 \times 10^{-12} \text{ F/m}\)). For EG on SiC substrates, \(\varepsilon_1\) is the permittivity of air (\(~1\)) and \(\varepsilon_2\) is the permittivity of SiC, which is a function of wavelength, given by:

\[
\varepsilon_2 = \varepsilon_2(\omega) = \varepsilon_\infty \frac{\omega^2 - \omega_{LO}^2 + i \Gamma_1 \omega}{\omega^2 - \omega_{TO}^2 + i \Gamma_2 \omega} 
\]

(Eq. 5.4)

Here, \(\varepsilon_\infty = 6.5\) is the positive ion core background dielectric constant, \(\omega_{LO}\) is the longitudinal optical phonon frequency (\(\omega_{LO} = 972 \text{ cm}^{-1}\)), and \(\omega_{TO}\) is the transverse optical phonon frequency (\(\omega_{TO} = 796 \text{ cm}^{-1}\)). \(\Gamma_1,2\) describes the broadening of the phonon resonances, typically 5–60 \text{ cm}^{-1}, where the higher values are caused by free-carrier absorption. By measuring the IR reflectivity of N+ 4H–SiC substrates, we found \(\Gamma_1 = 60 \text{ cm}^{-1}\), whereas \(\Gamma_2 = 10 \text{ cm}^{-1}\). \(\Gamma_1,2\) were used as free fitting parameters in the measurement of the EG/SiC interface, with these nominal values for \(\Gamma_1,2\) as the starting point (Daas et al., 2011).

Finally, the graphene film thickness was extracted while matching the experimental FTIR values. We found good agreement in EG thickness values grown at 1600°C estimated from XPS and FTIR which also validates the method to extract EG thickness for values >30 MLs which can not be done using XPS.

**EG/n-SiC Schottky diode fabrication and characterization results:**
Epitaxial graphene was grown on three different 8° 4H-SiC epilayers of thicknesses 26 µm, 6.2 µm and 12 µm at three ramp down rates 14°C/min, 28°C/min and 56°C/min, respectively. The doping concentration of the three corresponding epilayers were 1.6x10^{14} cm^{-3}, 2x10^{15} cm^{-3} and 4.5x10^{14} cm^{-3}. For the first time, we report these single step Schottky diode growth structures of epitaxial graphene on SiC grown using TFS. One of the major advantages of these EG/SiC structures is the reduction in the metal contact deposition and annealing steps in the diode fabrication process which is known to add some significant contact resistances to the final device structure. In our case, the EG is the Schottky metal contact which is deposited and annealed at high temperature in a single step during the growth process. The fabrication process flow is schematically given in fig.5.11.

Figure.5.11 Fabrication process flow for EG/SiC vertical schottky diodes

The fabrication process involves only two simple steps which are: 1. Patterning the devices by photolithography, 2. Isolating the patterns of devices on the sample by O₂ plasma etching of epitaxial graphene using Reactive Ion Etching method.

Current – Voltage characteristics of EG/n-SiC Schottky diodes:
From the I-V characteristic results (fig.5.12), we extracted the ideality $\eta$, leakage current ($I_0$) and resistances (series and shunt) of all the devices throughout the samples for each ramp down rate. It is evident from the results that the devices show better quality for the graphene grown at both low (~14 °C/min) /medium (~28 °C/min) ramp down rates with $\eta = 1.1$ whereas it is poor for the fast ramp down (~56 °C/min) growth ($\eta =1.3$) (fig.5.13). The thermal stress which is more pronounced in the fast ramp down growth causes the graphene layers to crack severely which increases the non-uniformity in the EG-SiC interface causing inhomogeneity in the Schottky barrier height (fig.5.14) and thereby degrading the device quality.

Figure.5.12. Forward I-V characteristics of EG/SiC Schottky diodes grown at different ramp down rates
Figure. 5.13 Average ideality values for EG/SiC Schottky diodes at different ramp down rates with three different areas (each data point represents an average of 28 devices for the respective areas of the device)

The Schottky barrier heights for the EG/SiC junction were derived from the leakage current densities of the diodes for different ramp down rates (fig.5.14) from thermionic emission equation given below:

\[
\Phi_B = \frac{kT}{q} \ln \left( \frac{J_0}{A^* T^2} \right) \quad \text{(Eq. 5.5)}
\]

where, Richardson's constant, \( A^* = 143 \, \text{A/cm}^2\text{K}^2 \) for 4H-SiC, \( T = 300\,\text{K} \), \( J_0 = \) leakage current density \( \text{(Acm}^{-2}) \) and \( \frac{kT}{q} \) is the thermal voltage at 300K = 0.0259eV.

From fig.5.14 it is evident that the \( \Phi_B \) values of the EG/SiC devices grown at the fastest ramp down rate (56 °C/min) exhibits huge variation in throughout the sample surface, the variation reduces for medium ramp down rate devices (28 °C/min) and follows a uniform trend for the slowest ramp down rate (14 °C/min). This gives additional evidence that a uniform EG/SiC junction is formed by slow cooling of the graphene layers during growth.
Figure 5.14. Schottky barrier height ($\Phi_B$) of EG/SiC Schottky junctions obtained for an average of 28 devices for different P/A of the devices (trend lines shown are guide to the eyes)

**EG/SiC Schottky diodes as UV-Photodetectors:**

In the application point of view, the EG/SiC Schottky diodes fabricated and tested above were used as ultra-violet (UV)-photo detectors due to the optical transparency of the metal electrode (EG) which reduces any losses due to reflection/absorption. Ultra-violet (UV) detectors are important for their applications in remote sensing, flame detection, UV dose monitoring etc. The UV spectrum is classified into three regions, UV-A (310-400 nm), which is relatively benign to human health, and the cancer-causing UV-B (280-315 nm) and UV-C (200-280nm) bands. 4H-SiC is suitable for detecting all 3 UV bands due to its favorable bandgap of ~3.26eV or 380nm.

Of the three different Schottky diodes discussed above, the best quality diode (slowest ramp down rate at 14 °C/min) was chosen to test the device performance as a UV detector. The epilayer thickness was 12µm and doping was $4.5 \times 10^{14}$ cm$^{-3}$ for this vertical Schottky diode structure with the epitaxial graphene thickness of ~14 ML (~4.6 nm).
From fig. 5.15 it can be clearly seen that there is a generation of small photocurrent (~ 3nA at 0V) and very small open-circuit voltage (~ 0.14V) under the UV-exposed conditions compared to the dark (unexposed) condition. The responsivity of the EG/SiC diodes for different wavelengths and power of UV spectra are shown in fig. 5.16. Responsivity (A/W) is calculated as the ratio of the photocurrent and the measured power at each wavelength. For a minimum power of 2.5 nW, the UV detectors could measure and exhibit a significant increase in the photocurrent (an order of magnitude increase) for almost the entire UV spectra of 250 nm to 400 nm. As the power of the UV source is increased, the responsivity is also increased as expected.
In summary, this growth method exploits the thermodynamic advantages of SiF$_4$ to increase the graphene growth rate (1.5 ML/min) and opens a new domain for producing in-situ large area, high temperature, high quality metal contact (graphene) for high temperature EG/SiC electronics. The thickness controllability offered by this method can be exploited for variety of applications where thick graphene (e.g. energy storage, fuel cells, etc.) and moderate to thin graphene (e.g. graphene-gated RF transistors, sensors, etc.) are needed. This growth method can serve as a template for fabricating in-situ high quality metal (EG) contacts for all graphene/SiC device structures (BJTs, MESFETs, Schottky diodes). Though the technique of hybrid EG/SiC devices has been demonstrated successfully for low power applications, in future, due to the increasing demand of SiC in high power electronics, it is necessary to improve the quality of both EG/SiC junction and underlying SiC epitaxial layer (without BPDs or In-grown SFs) for exploring the high-power domain of EG/SiC devices.
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