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Fault Protection In DC Microgrids Based On Autonomous Operation Of All Components

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DEDICATION

To my loving parents, Xin Deng and Xiaoling Dun

&

To all who have supported me through this process

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ABSTRACT

DC power distribution systems (or so called DC microgrids) are of wide interest for various power applications due to their advantages over traditional AC power distribution systems with respect to power density and power distribution efficiency. On the other hand, short-circuit faults present formidable hazards in these systems. It is difficult to extinguish these arc faults via conventional circuit breakers due to the lack of natural zero-crossing of DC current. Also the DC breakers are usually more bulky and costly. Today, fault protection in these systems – to the extent that it exists – relies on over-current time-out limits in power converters or on special circuit breakers that are tripped via over-current or distance relays and that therefore depend critically on a data network. More-robust communication-independent, fully-distributed schemes are needed.

In this dissertation, we address the problems for fault protection in DC microgrids, and define an approach Local Information Based Fault Protection (LIFP) for robust protection against short-circuit faults that does not rely on microgrid-wide communications. Builds on work of Pietro Cairoli, we show how each entity connected to the dc bus, including current-limiting power converters and non-load-breaking disconnect switches, can autonomously detect, identify, and appropriately react to the presence of a short-circuit arcing fault based only on its own local observations of voltage and current. Successful implementation of such an approach can eliminate the need for dc breakers or fuses. Such an approach can rapidly detect a fault, shut down power injection to the bus, isolate the

fault, then re-energize and return the bus to service. The entire process can occur in milliseconds and thus can be transparent to load systems that contain small energy buffers.

For MVDC power systems, we extend the coverage of LIFP to arc faults (with arc impedance up to 4 Ω) under varying load conditions (1 pu to 2 pu). The effective resistance of an arc can sometimes be large compared to that of the bus cables, and the arc resistance can vary randomly in time with large bandwidth; these characteristics complicate implementation of the LIFP method. Therefore, the characteristics of arc faults in DC systems are investigated, and the time-average resistance of DC arcs was represented via the Paukert equations, with the coefficients fitted to experimental data from DC converter-fed arcs. We describe the system design constraints and how moving average filters and dynamically-coordinated tripping thresholds can overcome these problems, and then we report the effectiveness of applying the method for a reference system over a wide range of system parameters (e.g. cable size and length), operating conditions (e.g. system current), and fault conditions (arc location, arc length).

In order to validate LIFP, the MATLAB-SIMULINK model of a representative multi-terminal MVDC system was developed. The effectiveness of the method was evaluated by applying arc faults, one at a time, to many locations. The apparent resistance parameter (V/I ratio) was computed for each controllable entity, for each fault occurrence, and evaluated to determine whether appropriate protection action was taken. Also due to the assumption that the current ramping rate (di/dt) of power converters during any load change is limited to be less than 110A/ms, it is used for differentiating load variations ($di/dt < k_{limit}$) from faults ($di/dt > k_{limit}$). Results demonstrate that there are no cases where a fault was not disconnected from the system and only a few cases where loads lost

power when they optimally should not have. For load variation events with a ramping rate up to 50A/ms, LIFP can successfully identify the incident and initiate adjustment of tripping thresholds within 4.5ms.

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V_n	voltage value at the terminal of switch ‘n’;
I_n	current value at the terminal of switch ‘n’;
R_n	apparent resistance at switch ‘n’ calculated from V_n / I_n;
V_r	voltage value at current limiting mode;
P_{r+}	heaviest power flow at the direction by default;
P_{r-}	heaviest power flow at the reverse direction by default;
R_{th+}	positive threshold for fault detection;
R_{th-}	negative threshold for fault detection;
V_{arc}	arc voltage;
I_{arc}	arc current;
R_{arc}	arc resistance;
μ	mean value;
σ	standard deviation;
+	impedance drops to a lower positive value due to the fault event;
-	impedance shifts to a negative value due to the fault event;
N	impedance stays at the same level during the fault event;
Y	bus admittance matrix;
V_i , V_j	voltage of adjacent nodes;
R_{CABij}	cable resistance between the two nodes i and j;
p, q	nodes that are connected to power sources;

I_{limit_q} , I_{limit_p} output target of the MMCs during current limiting mode;

$R_n^{F\_x}$ apparent impedance at the terminals of Switch n after fault event happens at location x;

$V_n^{F\_x}$ voltage at either terminal of Switch n after fault event happens at location x;

$I_n^{F\_x}$ current through Switch n after fault event happens at location x;

ΔR initial resistance margin;

ΔI initial current margin;

List of Abbreviations

DC ..... Direct Current

AC ..... Alternating Current

LIFP ..... Local Information Based Fault Protection

MVDC ..... Medium Voltage Direct Current

CFP ..... Centralized Fault Protection

LFC ..... Local Fault Controller

CFC ..... Central Fault Controller

ESRDC ..... Electric Ship Research and Development Consortium

MW ..... Megawatts

HVDC ..... High Voltage Direct Current

UHVDC ..... Ultra-High Voltage Direct Current

LVDC ..... Low Voltage Direct Current

SES ..... Shipboard Electrical System

SiC ..... Silicon Carbide

SSPD ..... Solid State Protective Device

PDM ..... Power Distribution Module

VSC ..... Voltage Source Converter

SSCB ..... Solid State Circuit Breaker

CFM ..... Centralized Fault Management

VSM ..... Voltage Source Mode

CSM ..... Current Source Mode

CHAPTER 1

INTRODUCTION

This Chapter aims to describe and discuss the challenges in this research, whereas all of the background material with most references has been put in Chapter 2.

The goal of this research is to develop a "breakerless" method of protecting DC microgrids against short-circuit arc faults based on shut-down and reconfigure. This method is expected to detect and locate a wide range of faults, including low impedance (<0.02pu) bolted faults as well as high impedance (>0.08pu) arc faults, only via local information without wide area communication. This research is important as interest in dc microgrids is rapidly increasing, especially for applications such as data centers, smart houses, power collection in wind or solar farms, or integrated power and propulsion systems for ships, electric vehicles or offshore oil and gas drilling platforms [1]-[9]. Due to the absence of natural zero-crossings for dc current, it is difficult to clear short circuits in dc systems with traditional mechanical circuit breakers, even if electrically-tripped. This difficulty has led us to investigate a different approach which relies on coordinated control of power converters and non-load-breaking disconnect switches, so that the fault can be cleared by completely de-energizing the entire affected portion of the system, reconfiguring (i.e. isolating the faulty section) via disconnect switches while de-energized, and finally re-energizing the entire system [60]-[62].

The objective for the fault protection algorithm is to ensure that the closest switch/switches (either two closest switches at both ends of the cable on a ring bus, or one closest switch at one end of the cable at the branch circuit) are assigned to isolate the faulted segment while the remaining parts of the system stay fully functional. It is obvious that this fault protection scheme needs to be integrated with fault localization approaches in order to guarantee selectivity just like all the other fault protection schemes. There are always tradeoff decisions to be made when designing the fault protection scheme for a Medium Voltage DC (MVDC) system. The adoption of differential protection, so called Centralized Fault Protection (CFP) [22], can be a viable solution for achieving fast and accurate protection for short-circuit faults. But it can also put the whole system at great risk in the event of failure in the wide area communication system. In contrast, the Local Information Based Fault Protection (LIFP), which has adopted the concept of "distance protection" that is common in ac systems, chooses a different strategy by relying only on local observations of voltage and current. Apparently this method brings huge benefits because a system that does not rely on communications is not susceptible to failure based on failure of the communications. Also the distributed decision making capability (decision can be made directly at local fault controllers (LFC) instead of through central fault controllers (CFC)) provides additional protection to the system in dealing with undesirable operating conditions.

When it comes to multi-terminal microgrids, "communication dependent" fault protection schemes are widely used because there are not yet any known methods for avoiding dependence on communication especially considering the difficulty of coordinating tripping settings. Very few studies have been carried out to develop

impedance based communication-independent fault protection methods in such systems until the rapid advancing of dc microgrids applications in recent years. One of the driving forces is led by the Electric Ship Research and Development Consortium (ESRDC), which is of special interest to develop a communication-independent fault protection scheme for the next generation of "all-electric" naval ship [15]-[16].

The major challenges with the LIFP method are often associated with its communication-independent feature. On one hand, it requires more efforts to coordinate tripping settings at each LFC to guarantee reliability and selectivity for fault protection. Also, it may be difficult for a device "here" to determine that a fault has occurred "there" (far away), and that it should shut down in order to clear the fault. In order to overcome these challenges, a novel algorithm needs to be developed and integrated with the LIFP method. This algorithm should be able to differentiate whether the system is experiencing normal load variations or a short circuit fault by evaluating the changing rate of the local measurements. Also it should be able to automatically determine and adjust the tripping settings for each switch with the presence of severe system noise. This approach is expected to largely increase the applicability of LIFP to the MVDC shipboard power systems, and has great potential to facilitate the application of LIFP in other dc microgrids.

Therefore, this work aims to address and solve challenges that are summarized as follows:

- Limited fault coverage (only response to low impedance fault (<0.02pu) with constant value) of existing communication-independent fault location technique.
- Difficulty of existing fault identification technique for differentiating normal load variations from short circuit faults.

- Coordination of tripping settings for all switches in the system still needs human intervention and is time consuming.

1.1 PROTECTION FOR HIGH IMPEDANCE ARC FAULTS

One of the most common challenges for impedance-based fault protection method is protecting against high impedance short circuit faults. It is difficult to locate a fault when the fault impedance is nearly the same as the system cable impedance – which can be very small in a high power dc system. Thus, it will be interesting to investigate how the fault impedance can affect the effectiveness of the LIFP method, and how the tradeoff decision can be made between the coverage range of the LIFP for fault and the effectiveness of the LIFP in application. On one hand, it is important to define the range of fault impedance that the existing fault protection scheme can cover without losing its reliability and selectivity for a given system configuration. On the other hand, it is valuable to test the response of the fault protection scheme for different system configurations (such as cable resistance), so as to provide possible optimization for the system level design.

Also it should be noticed that most of the previous studies assumed that faults could be modeled as pure resistances. However for applications like the shipboard systems, arc faults have very high probability to occur in the short circuit events. The current of arc can vary randomly in a wide range, and the impedance can be unpredictable due to its nonlinear and time varying behavior. Hence, it is worthwhile to analyze the characteristic of arc impedance for various fault conditions (current level, operating mode, arc length and etc.) in order to establish a practical arc model [51]-[55]. Furthermore, it is of great importance to validate the LIFP method in correspondence with these high impedance arc

faults, so as to find out whether LIFP still works as it should, or under what condition this method will work.

1.2 AUTOMATIC CALCULATION OF TRIPPING THRESHOLDS

It has been illustrated in previous studies [48] that both the power converters and the dc disconnect switches need to be aware of the fault events under current fault protection scheme. However the difference is, the power converters only need to know if there is a fault in the system, because all of them will eventually operate to de-energize the whole system through the fault clearing sequence, whereas the switches need to estimate the fault location, because only the corresponding switches should open to isolate the faulted segment while the others should remain closed. The power converters adopt overcurrent protection. The current through the converters are measured and compared to the tripping thresholds to determine whether the converters should go into current limiting mode. Similar ideas are applied to the switches which adopt impedance protection. The impedance tripping thresholds defines the tripping zone and non-tripping zone of each switch, and further determines the operation status of each switch during fault scenarios. Therefore, it is of great importance to optimize the settings of tripping thresholds, otherwise the switches may operate incorrectly under certain circumstances.

The setting of tripping thresholds can vary switch by switch, and is strongly affected by the topology and the parameters of the system. Former study assumes the MVDC system is always operating with the same system configuration, so as fixed tripping thresholds are assigned for switches based on simple estimation. However for a practical MVDC systems, each generation unit or zonal load can either be connected to or disconnected from the whole system or experience significant shifting of power demand regarding

various operating conditions (take the shipboard system for example, the pulse load can be active at certain conditions, and the propulsion load demand can vary dramatically). Even the system topology can change by changing switch settings. Therefore, it is necessary to develop an algorithm that can automatically calculate the tripping thresholds for all the switches during the interval between each system reconfiguration.

1.3 DIFFERENTIATING ARC FAULTS VERSUS NORMAL SYSTEM VARIATIONS

The existing LIFP method evaluates current at converter terminals and apparent resistance at switch terminals to determine the status of the system: whether in fault condition or normal operating condition. And this method assumes that tripping thresholds for switches remain fixed between each system reconfiguration. However the power demand of system loads will be time varying, and these events may look similar to arc faults in terms of current or apparent resistance. This characteristic complicates implementation of the LIFP method. For example, assume that the rated value of some load is 4 Ω and that the apparent resistance of this load can drop to 0.8 Ω under certain load ramping up conditions. Comparatively, if an arc fault with 1 Ω resistance occurs near the load, the apparent resistance of the arc plus load will also be equal to 0.8 Ω. Therefore, it is difficult to tell a fault event apart from normal system variation events by only referring to the apparent resistance value.

It will have merit if some extra information can be extracted from the apparent resistance for fault identification purpose. According to the IEEE standard 1709, a connected load cannot draw more power from the dc bus than is allowed by the load di/dt rating. Hence the current derivative is of special interest for further investigation. It is expected to be an effective indicator to differentiate whether the system is experiencing a

fault or just a load variation. It would be a very interesting challenge to develop a local information based algorithm which automatically adjusts the tripping thresholds under various load variation scenarios without compromising the reliability and accuracy of arc fault detection.

1.4 NOISE TOLERANCE OF LOCALIZED FAULT PROTECTION

There can be considerable amount of noise on the dc bus even when the system is operating at steady state, such as that caused by the operation of switching power converters or that caused by short-circuit arc faults. While these noises may be insignificant in terms of power distribution, but can cause big problems for the LIFP method, as explained next.

One major concern is false triggering when noise causes a parameter to exceed the detection threshold. The tripping signal can be generated by the local controller once the apparent resistance is calculated and monitored through measurement falls into the preset tripping zone. However, it can be possible that the peak values of the apparent resistance go beyond the threshold while the average value of the apparent resistance remains below the threshold. Thus, in order to increase the noise tolerance and guarantee the reliability of the LIFP scheme, it is important to overcome this mistripping challenge by analyzing how the noise will affect the protection scheme, and further propose a noise-compatible solution.

Another major concern regards the undesirable influence noise may impose on the current derivative based fault identification method. The current derivative can vary dramatically even when the system is in normal operating condition due to the unpredictable feature of system noise. If low pass filter is adopted to reduce bandwidth,

considerable time delay will be introduced to the whole fault clearing process. Thus, it is of great importance to propose a noise-immune solution for this current derivative based algorithm.

CHAPTER 2

LITERATURE REVIEW AND BACKGROUND

Interest in MW-scale microgrids is rapidly increasing. Microgrids are electrical distribution systems containing loads and distributed energy resources that can be operated either connected to the main power network or islanded [1]. It is a promising technology that fits in with the Smart Grid concept. Compared to traditional large-scale power systems, microgrids bring more flexibility and efficiency to power generation and power distribution, so as such they are being widely adopted in both industrial and residential applications.

According to a tracker report from Navigant Research, more than 480 microgrid projects are proposed, planned, under construction, or operating worldwide, representing nearly 3800 magawatts (MW) of capacity [2]. Microgrids are beginning to move into the mainstream, and have caught the attention of many research groups in industry and academe. Recent literatures show interest in microgrid technologies such as system dynamic and fault protection, intelligent management and control, renewable generation, power quality, power flow, load forecasting, and system integration.

2.1 MVDC MICROGRIDS

The benefit of dc over ac in microgrids generally lies in three facts: First, the rapid advance of power electronic techniques make transformer free power systems applicable at the distribution level. Second, dc systems require fewer stages of power conversion for

various ac and dc loads connected to the common bus [5] [6]. Third, ac current only flows through the outer surface of cable due to the skin effect, whereas dc current can flow through the entire cable. Thus dc systems can deliver times more power than ac systems for power cables of the same size [4].

However, when it comes to fault protection, ac microgrids still have a clear advantage over dc microgirds. The existing IEEE/IEC standards for fault protection within ac systems can be easily applied to an ac microgrid. But the same rule doesn't apply for dc microgrids, because the standards on the protection of dc systems currently do not exist [4]. Additionally, ac circuit breakers are very common and well developed equipment in ac systems (from medium voltage level to high voltage level) for fault isolating purpose, whereas the application of such circuit breakers in dc systems is largely constrained to voltage ratings under 1-10 kV, because there are no natural zero crossings of the dc current [7]-[10]. There are dc circuit breakers available as products in industry by manufacturers like ABB and EATON, for voltage rating up to 1 kV. But still they are costly and bulky in size [11]-[13].

DC power systems can be categorized by means of voltage rating: at transmission level, high voltage dc (HVDC) is rated above 65 kV, while ultra-high voltage dc (UHVDC) is typically rated above 800 kV; at distribution level, medium voltage dc (MVDC) is rated from 1500 V to 22 kV, while low voltage dc (LVDC) is rated below 1500 V [3]. Although there have been significant research on HVDC transmission systems, the dc distribution (MVDC & LVDC) systems are becoming more and more popular especially in recent years [4].

2.1.1 MVDC SHIPBOARD POWER SYSTEM.

MVDC power systems are of wide interest for the next generation of "all-electric" naval ships because MVDC appears to be the only technology that will be able to meet the stringent demands on power and energy density [14][15]. One general topology of an MVDC shipboard power system is displayed in Figure 2.1 [16][17].

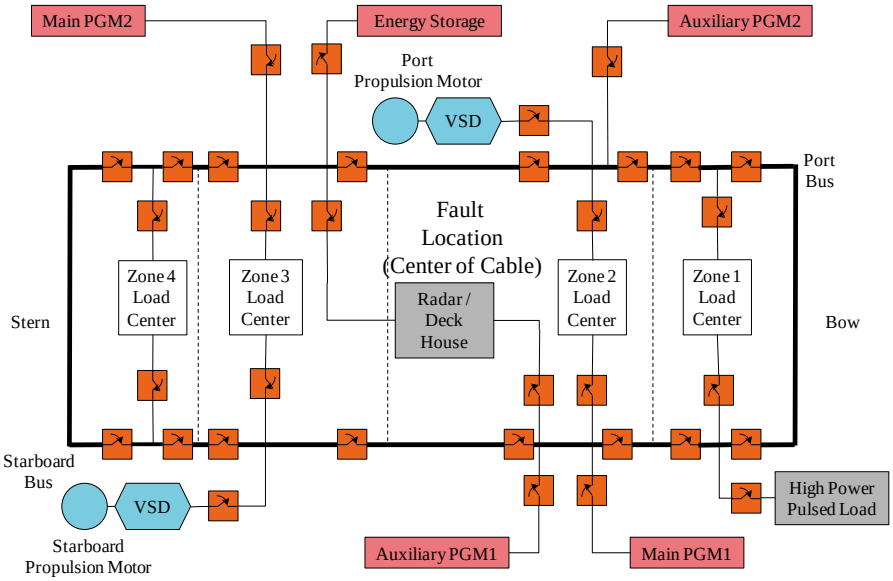


Figure 2.1 Concept diagram of the MVDC shipboard power system [16]

This system is an implementation of a generic multi-terminal dc Shipboard Electrical System (SES) derived from [18]-[20]. It has several ac generators feeding the dc ring bus through rectifier converters. The dc ring bus is rated at 5 kV, the two main generators are rated at 47 MVA each, and the two auxiliaries are rated at 5 MVA each. The voltage-controlled rectifiers are rated at 5 MVA each, and they convert the 4.16 kV, three-phase ac voltage to 5 kV dc [21]. These rectifiers are assumed to have a built-in fault protection mode that will limit current or shut off completely when a fault is detected. In this MVDC

system, sectionalizers (dc disconnect switches) are placed at each end of each cable section on the ring bus, and at the connecting end of the cables on branches connected to the ring bus, so that a faulted section can be isolated from the rest of the system. Loads within zones are supplied through dc-dc converters [22].

The Office of Naval Research and the University of Pittsburgh also proposed a generic MVDC-based electric ship architecture shown in Figure 2.2 [23]. It applies similar concept of integrated power system (IPS) as in [16] which enables all the energy generated by the ac generators to be converted to dc power at the MVDC ring bus, and further delivered to various dc and ac loads in the ship system through dc/dc and dc/ac converters. There are also dc disconnects at both the ring bus and the load branches for fault protection purpose.

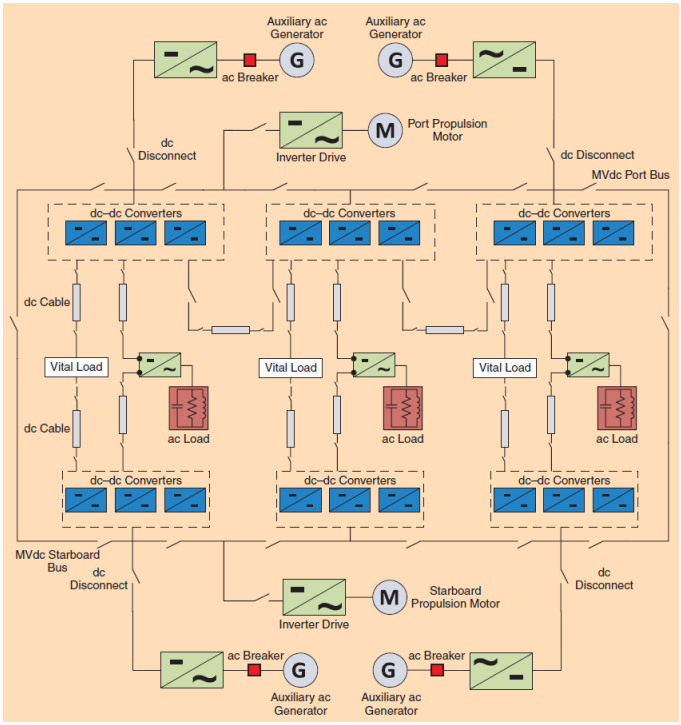


Figure 2.2 A generic layout of the MVDC shipboard power system [23]

2.1.2 OTHER DC MICROGRIDS

The dc microgrids are not only of interest in dc zonal systems for ships, but also attract great attention in other industrial applications such as offshore oil and gas drilling platforms, remote area mine site, renewable energy systems, and data centers [7][24][25]. There are three main reasons for the popularity of MVDC/LVDC microgrids in these applications: First, for certain industrial operations in remote areas (such as offshore oil and gas drilling, and remote area mining), it is hard or even impossible to obtain electric power from the national grid through power transmission. As a result, using the power generated and distributed locally seems to be the only viable solution. Second, it has been well recognized worldwide that using renewable energy such as solar power can achieve long-term environmental and economic benefits. The dc microgrids provide a flexible platform for conveniently integrating the maximum possible renewable energy sources which predominantly generate dc into these localized power systems [26]. Third, comparing to ac microgrids, the dc microgrids have improved power quality, increased conversion efficiency and simpler power electronic interfaces.

Reference [23][27][28] introduced a MVDC power system for offshore oil and gas drilling platforms. The system architecture is shown in Figure 2.3. Up to 20MW power is generated locally by off-shore wind farms to serve the offshore drilling platform through the MVDC system. It can be noticed that breakers are placed at each branch for fault protection. However, there is no breaker at the MVDC collection platform, so if short circuit fault occurs at the dc bus, the whole collection platform will need to be disconnected, and the drilling platform can only use its secondary dc bus which fed by its local diesel generator.

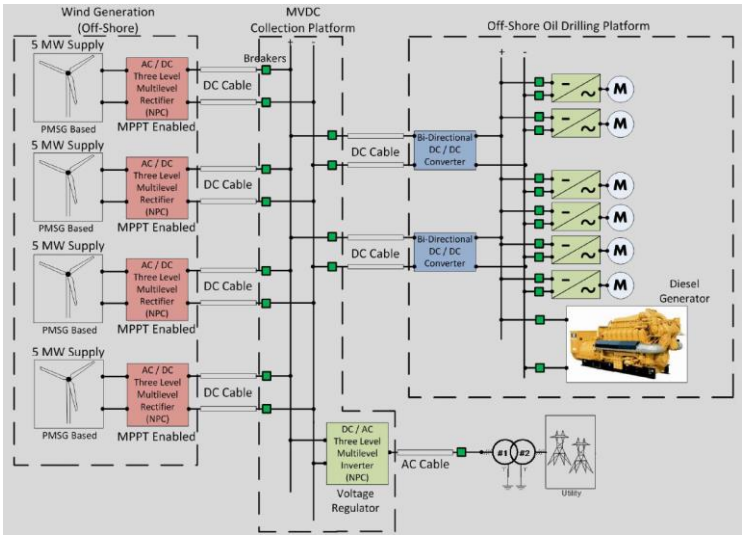


Figure 2.3 MVDC power system for offshore oil and gas drilling platforms [23]

Reference [32] indicates Mitsubishi Electric is planning to build a development and demonstration facility for MVDC distribution at its power distribution system center. Also, companies and institutes like Intel, HP, Emerson Network Power, The Green Grid, Lawrence Berkeley National Laboratory and Universal Electric are in favor of 400 V dc systems for their data centers [33]-[37]. A study conducted by these companies concluded that energy savings of approximately 7 to 8 percent could be achieved over high efficiency, best practices 480-280 Vac – with a 15 percent electrical facility capital cost savings, as well as a 33 percent space savings and 200 percent reliability improvement [34].

2.1.3 Protection Strategies For Dc Microgrids

Reference [29][30] investigated the protection and control strategies for an MVDC microgrid within a remote area mine site. A communication based differential protection scheme is adopted as primary protection, whereas the overcurrent protection scheme is set

as backup. Reference [31] introduced a multi-terminal MVDC distribution system with renewable energy sources. The fault current is extinguished by dc circuit breakers, and then the faulty part is isolated by dc switches. However, this protection scheme needs communication between over current relays for fault location and coordination.

As the advance of wide bandgap power semiconductor technology such as the enabling of Silicon Carbide (SiC) with voltage rating from 1.2kV to 10kV in power electronics [38], the solid state protective devices (SSPDs) are presently being considered for fault mitigation in "Breaker-Based" future shipboard power system shown in Figure 2.4. These SSPDs are deployed at the Power Distribution Modules (PDMs) both at the main dc ring bus and LVDC distribution bus. There are communications among these SSPDs for the coordination of fault protection. The location of the fault is ascertained by capturing fault current snapshots at every fault isolation point and then communicating this information up to a higher level in order to determine which no-load switch to open [39]. Apparently, this approach is still communication-dependent comparing to LIFP.

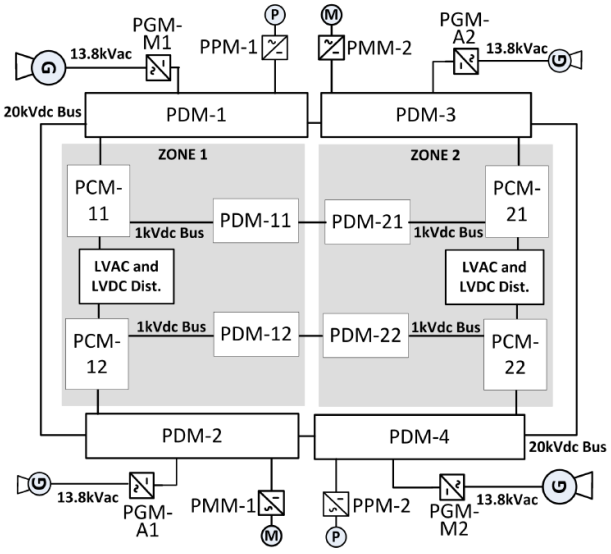


Figure 2.4 An MVDC shipboard system architecture using SSPD [39]

Figure 2.5 illustrates the layout of a unidirectional interrupting SSPD at the system shown in Figure 2.5. Compared to direct interruption of fault current (along with arc extinguishing) via conventional mechanical breakers, these SSPDs use power electronics to drive fault current to zero so that the fault can be galvanically isolated from the rest of the system by no-load mechanical switches. When a fault occurs at the MVDC side, the energy stored in the output capacitors of the VSC will discharge into the fault and induce large fault current going through the SSPD. The rate of rise in this fault current (di/dt) is limited by the current limiting inductor as shown in Figure 2.5, but once the fault current goes beyond the tripping level in the SSPD, all of the SiC MOSFETs in the SSPD will be informed to open. The device current will be diverted into the parallel RC snubber, which limits the rate of rise in voltage (dv/di), and damped through the resistance [39].

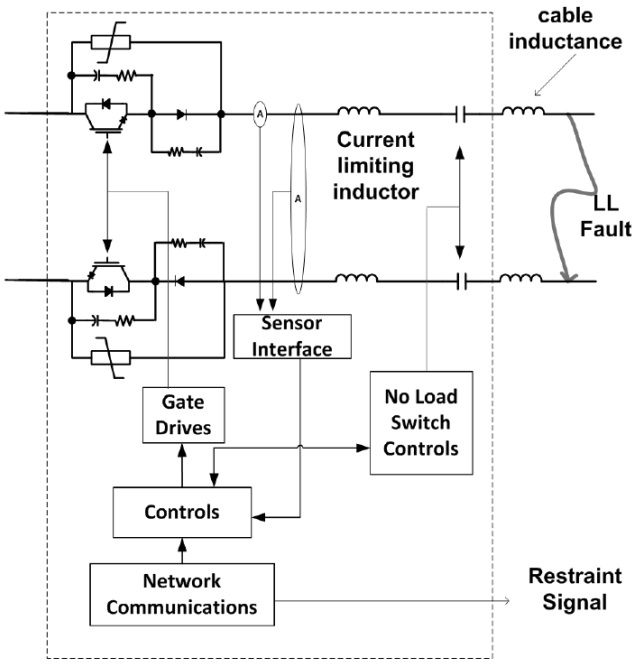
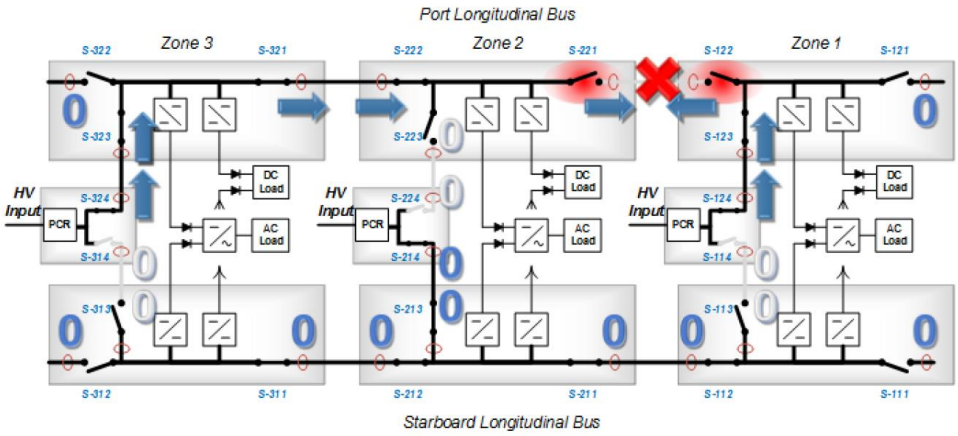
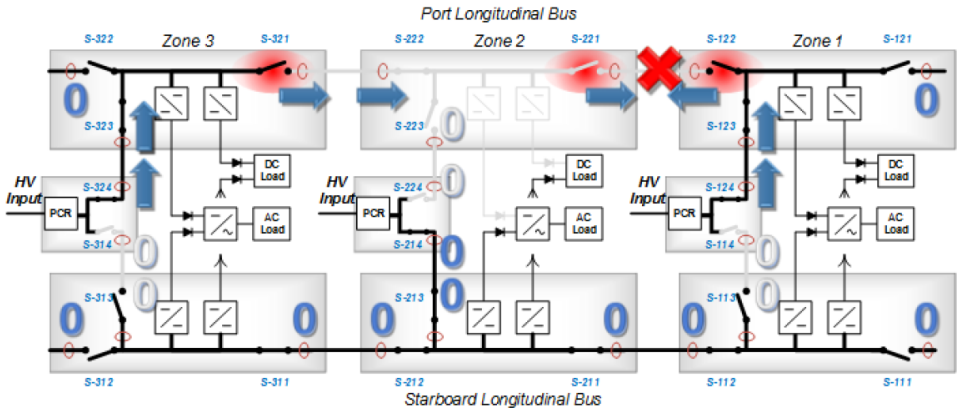


Figure 2.5 A unidirectional interrupting SSPD [39].

Currently, a DC Zonal Electrical System (DCZEDS) topology [40] as shown in Figure 2.6 has also been taken into consideration by the US Navy for the next generation all-electric ships. Similar to the architectures mentioned in Figure 2.1 and Figure 2.4, this system layout enables the sharing of energy resources via phase controlled rectifiers (PCRs) among different loads, such as electric propulsion, pumps, lighting and pulsed loads, so increases the overall system survivability. It can be noticed that every load can be feed bi-directionally and independently. The PCRs are followed by large output capacitors for harmonics filtering, so as these VSCs can bring in very high discharge current when short-circuit fault occurs. Again the electromechanical no load switches placed at various locations are for system segmentizing but not current interrupting purpose. When fault occurs on one of the longitudinal buses, PCRs that connected to the faulted bus (either the port longitudinal bus or the starboard longitudinal bus) will bring down the fault current to zero only after the filter capacitor at the output of PCR discharges, while the loads can still be fed through the other bus.



(a) Fault interruption with communications.



(b) Fault interruption without communications

Figure 2.6 Layout of a fault protection solution in DC Zonal Electrical System [40]

The fault identification and isolation process in this system is fulfilled via LAN communications between bus switch assemblies and PCRs. The current is measured at the current sensor in each assembly and constantly compared to a predetermined threshold (10kA) ten times of the rated current (1kA). If the value exceeds this threshold, the assembly detects the fault event and then sends out this information to all connected PCRs and switch assemblies via communications. Eventually each assembly gathers information from adjacent assemblies to determine a course of action by following two criterions:

a. If the summation of current going into/out of an assembly is not equal to zero, it means internal fault occurs inside this assembly, so as all switches within this assembly will be open to isolate the fault from the remained system.

b. If the current flowing out of a port of an assembly doesn't equal to the current flowing into the adjacent port of an adjacent assembly as shown in Figure 2.6(a), it means

fault occurs between the two, so as both assemblies open the switch at corresponding ports [40].

Though this fault protection scheme requires LAN communications among the assemblies, it doesn't rely on any centralized controllers for fault identification. However, if the communication is interrupted, only criterion *a* can be used for fault identification. Whereas for criterion *b*, all assemblies that detect the high fault current will assume the fault is just beyond the outgoing switch and consequently open the outgoing switch as shown in Figure 2.6(b). This will result in the isolation of a larger portion of the system compared to the case with communication.

2.2 FAULT LOCATION METHODS

2.2.1 CLASSIFICATION OF FAULT LOCATION METHODS

The concept of fault protection generally includes two parts: fault detection and fault location. The objective for fault detection is to determine the existence of a fault, whereas the localization of fault typically requires more effort in the accuracy of data measurement and data processing to determine the location of a fault.

Various kinds of conventional fault location methods have already been developed for large scale ac power grids over decades, such as methods that rely on phasor measurement unit (PMU) or phasor information [41][42], methods based on monitoring system reactance from one terminal of a line [43][44], and methods that use traveling wave generated from fault as an index for fault location, so as compare the difference in time of arrival at two or more locations of a bus to determine the fault location [45][46]. However these methods are typically applied for large scale systems with many miles long distance,

and they may face difficulties when it comes to dc microgrids with low cable impedance due to short distance [4]. Fortunately, some techniques used in the ac systems can still be applied directly to the MVDC systems. Different fault location methodologies are summarized in Table I [47], and they can be categorized as either communication-dependent method or communication-independent method.

Table 2.1 Comparison Of Different Fault Location Methods [47]

	Differential protection	**Directional protection**	**Impedance protection**	**Overcurrent protection**	**Current derivative protection**
Algorithm	Current summation equal to zero	Reverse of current direction after fault	Apparent impedance drop into the tripping zone after fault	Current go beyond threshold after fault	Current derivative go beyond threshold after fault
Wide area communication	Dependent	Dependent	Independent	Independent	Independent
Measurement	Global, low resolution	Global, high resolution	Local, medium/high resolution	Local, medium/high resolution	Local, medium/high resolution
Sensitivity	Highly depends on communication	Sensitive to dynamic interactions at transients; Highly depends on communication	Sensitive to fault impedance; Sensitive to fault close to next zone	Sensitive to distorted fault current waveforms	Sensitive to system noise
Issues in practical application	Limited by communication capability	Limited by communication capability	Coordination of tripping thresholds for different switches	Selection of proper tripping thresholds	Selection of proper tripping thresholds; Time delay introduced by the low pass filter

The communication-dependent methods rely on the exchange of information at different locations of the system via wide area communication: 1) Differential protection – The summation of current going into a given protection zone is compared to zero (or a given small value) to determine if fault happens within the protection zone. 2) Directional

protection – The direction of current flowing through the given relay will change when fault occurs at given protection zone. This protection method is often combined with other protection methods such as overcurrent protection in application.

Other fault location techniques are often used in combination with differential protection [4]. Take a dc microgrid system shown in Figure 2.7 for example, Solid State Circuit Breakers (SSCBs) are adopted for interruption of fault current and isolation of faulted branch. These SSCBs are grouped to set zones for differential protection. After the faulted segment has been identified via differential protection and separated by the SSCBs, the probe power unit will be connected to test the fault status before reclosing the SSCBs [4].

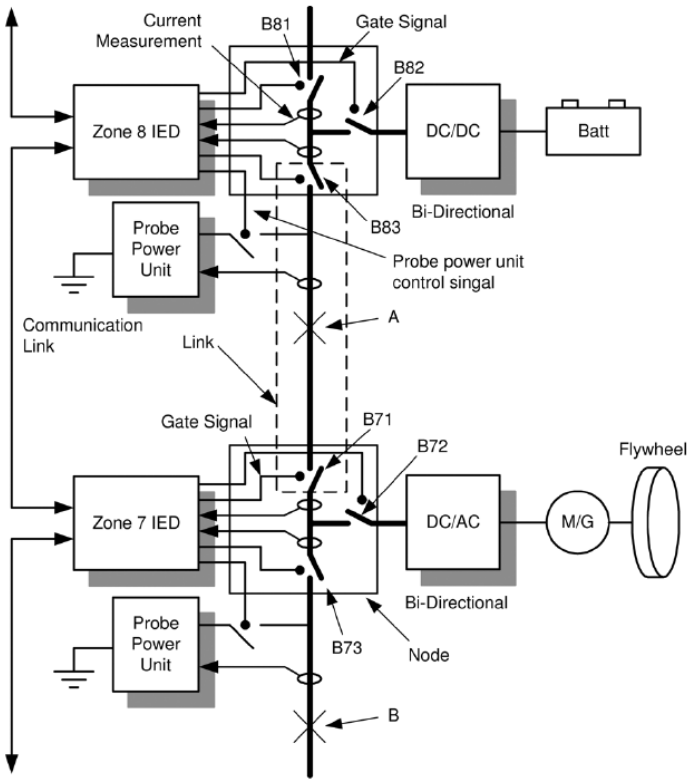


Figure 2.7 Implementation of active impedance estimation on fault location in a dc microgrid system with SSCBs [4]

Figure 2.8 shows the circuit diagram of this fault location technique via active impedance estimation. The probe power unit consists of its own power source (battery), probe capacitor, probe inductor and connection switch. Once the probe voltage is applied to the faulted bus, the probe current will be induced as a system response to this second-order RLC circuit. With the knowledge of the parameters of the probe circuit, the distance to the fault location d can be readily calculated from the probe current frequency, and the fault resistance can be obtained via the envelope waveform of the probe current [4]. However, this method assumes that the fault persists even at the low probe voltage.

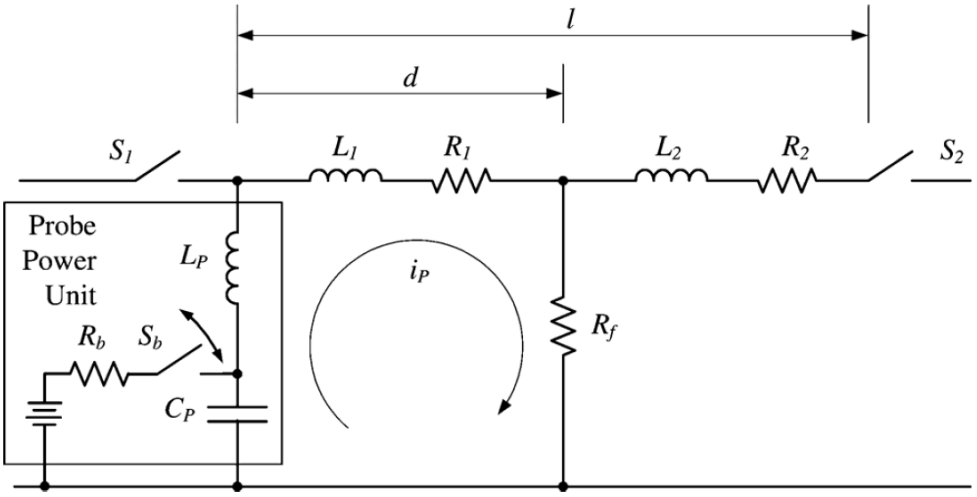


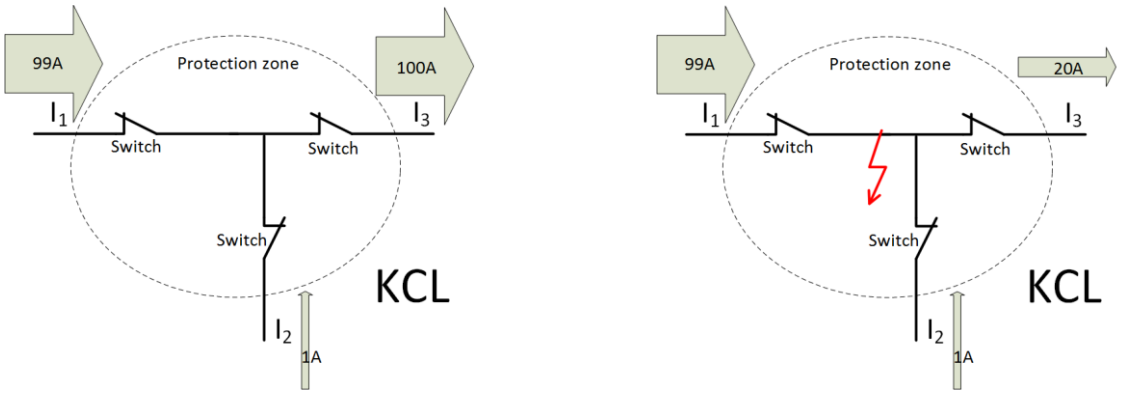
Figure 2.8 Circuit layout of fault location using active impedance estimation

Comparatively, the communication-independent methods only rely on information obtained locally: 1) Impedance protection – The apparent impedance, which is calculated through voltage and current measurements at switch terminals, is compared to tripping thresholds to determine if fault happens within the protection zone. 2) Overcurrent

protection – The current going through the switch is compared to tripping threshold to determine if fault occurs within the protection zone. This protection method often requires step-type coordination to guarantee the selectivity. 3) Current derivative protection – The current derivative is compared to tripping thresholds to determine if fault happens within the protection zone.

2.2.2 Differential Protection

The operating mechanism for differential protection is illustrated in Figure 2.9, as the summation of current going into a given protection zone should be equal to (or very close to) the summation of current going out of a given protection zone when no fault occurs within this protection zone.



(a) No fault in the protection zone (b) Fault occurs within the protection zone

Figure 2.9 Algorithm of differential protection

For the MVDC system shown in Figure 2.10, the whole system is partitioned into a number of protection zones for the purposes of fault localization and isolation. The remote sensors are distributed at the switches, where they measure current and send the digitized

current data to their corresponding controller. When a fault happens, the differential schemes will tell if the fault is inside or outside of its zone [22].

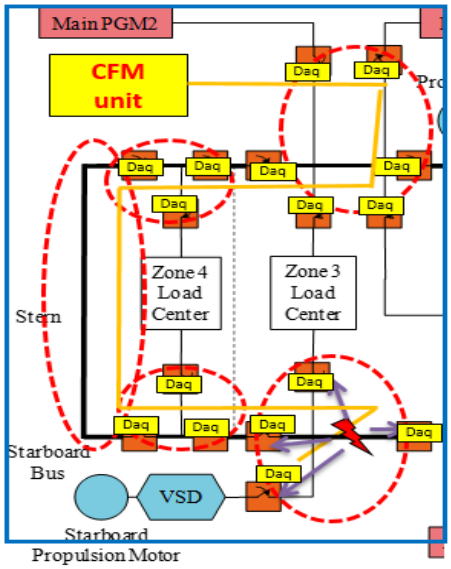


Figure 2.10 Zonal Arrangement of Differential Protection in the MVDC System [22]

2.2.3 Impedance Protection

In the impedance protection scenario, dc switches autonomously decide to open or not based on their local interpretation of time-to-trip curves as functions of apparent circuit resistance. In the terrestrial power community this method is also called "distance protection". Only the actual distances in a dc microgrid may be very short. Each dc switch needs to look at its own current and voltage status and simultaneously make the same decision – whether the fault is very near to itself, or is it beyond its range of influence. The process can be divided into two distinct steps [48]:

1. Terminal resistance calculation – voltage sensors and current sensors are installed at the terminal of each dc switch to obtain voltage and current values. These real-

time data are transmitted through local wiring to the controller, that has also been placed locally with the switch, to calculate real-time apparent resistance at the output terminal for each sampling cycle using (2.1),

$$R_n(t) = \frac{V_n(t)}{I_n(t)} \tag{2.1}$$

Where;

V_n is the voltage value at the terminal of switch $'n'$;

I_n is the current value at the terminal of switch $'n'$;

R_n is the apparent resistance at switch 'n' calculated from V_n / I_n.

2. Threshold resistance calculation – the real-time apparent resistance value R_n is then compared with pre-defined thresholds in the local controller. If the controller recognizes an apparent resistance beyond pre-defined thresholds, the local switch will get an enabling signal from the local controller, so that it knows to open after the system is de-energized (refer to time period t4 shown in Figure 4.1). Notice here we are using two thresholds instead of a single threshold. This is because for a multi-terminal closed-loop ring bus MVDC system, characteristics of the fault such as location, type and impedance value, may not only affect the value but also the direction of current flow, which will result in a negative value for corresponding apparent resistance at the terminal. Therefore, the positive threshold for fault detection has to be smaller than the apparent resistance corresponding to the heaviest power flow from the pre-defined positive direction, yet the negative threshold has to be larger than the apparent resistance

corresponding to the heaviest power flow from the pre-defined negative direction, as shown in (2.2),

$$R_{th+} < \frac{V_r^2}{P_{r+}};\ R_{th-} > \frac{V_r^2}{P_{r-}} \tag{2.2}$$

Where;

V_r is the voltage value at current limiting mode;

P_{r+} is the heaviest power flow at the direction by default;

P_{r-} is the heaviest power flow at the reverse direction by default;

R_{th+} is the positive threshold for fault detection;

R_{th-} is the negative threshold for fault detection.

It is obvious that dc switches in different zones/locations have different priorities for opening. Each dc switch open only when its terminal apparent resistance falls into its own tripping thresholds. Hence these threshold values need to be properly chosen in order to guarantee the robustness and selectivity of this distance protection scheme [49].

CHAPTER 3

ANALYSIS OF ARC FAULT IN MVDC SYSTEMS

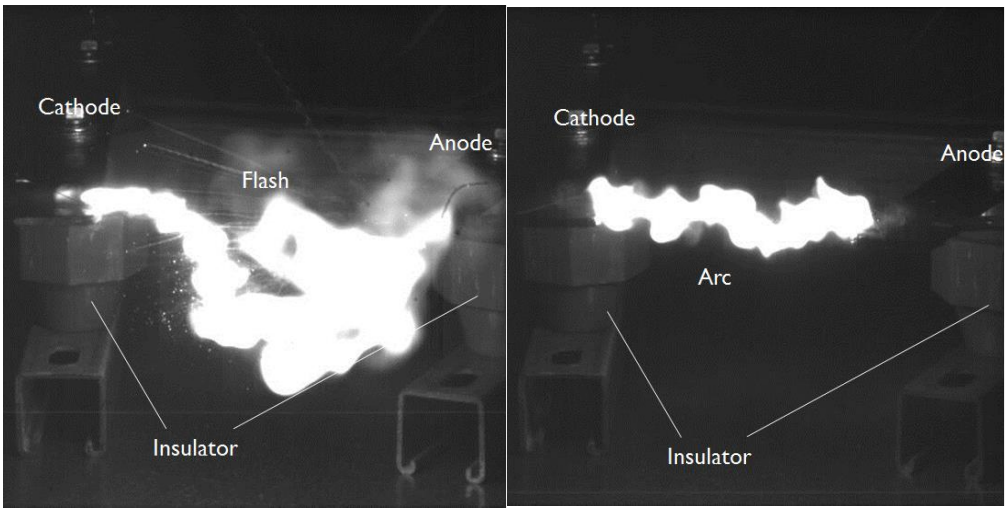
In order to evaluate our fault protection method, the characteristic of arc fault in MVDC systems should be studied. It is necessary to find out an arc model which can represent realistic arc effects that might hinder operation of the arc fault detector, so as the coverage and performance of LIFP regarding such fault scenarios can be identified.

As a most common fault in the MVDC system, short circuit fault can be triggered through a minor conductor (such as copper wire, steel screw, and pencil graphite) across the bus and the ground, a small animal bridging the conductors, condensation of water on an insulator or even impingement damage. It can rapidly develop into a lasting arc due to the absence of natural zero-crossing in the direct current. Apparently, this arc fault has different characteristics compared to bolted fault [48].

3.1 CHARACTERISTICS OF DC ARC FAULT

Various arc tests were performed by staff and researchers at CAPS on a fault testbed shown in Figure 3.1 [51]. These test data and test configurations are shared with us for research purpose. The cathode and the anode were connected across the dc source through metal rails, and supported by insulators off the ground. An ignition wire with 0.35 mm diameter was connected bridging the 88.9 mm (3.5 inch) gap between the electrodes. When MVDC was applied to the electrodes, current builds up in the wire and there is flash over the ignition gap as shown in Figure 3.1 (a). The evaporated metal materials from both

the wire and the surface of electrodes resulted in plasma jets, and eventually developed into a continually burning metal-vapor arc displayed in Figure 3.1 (b).

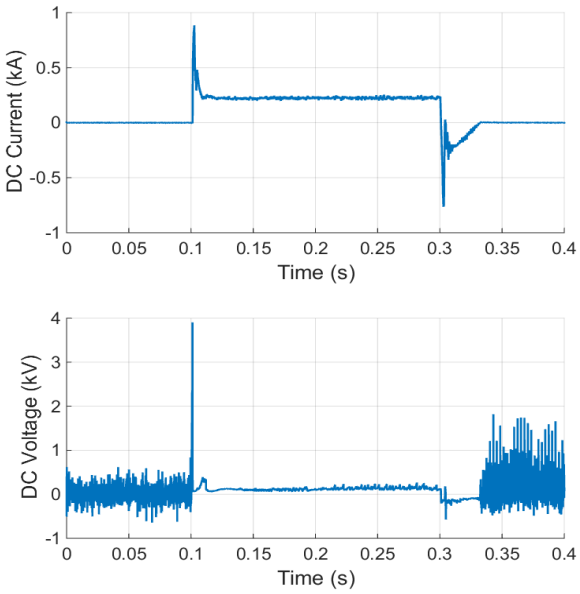


(a) Flash along the ignition wire (b) Arc across the electrode gap

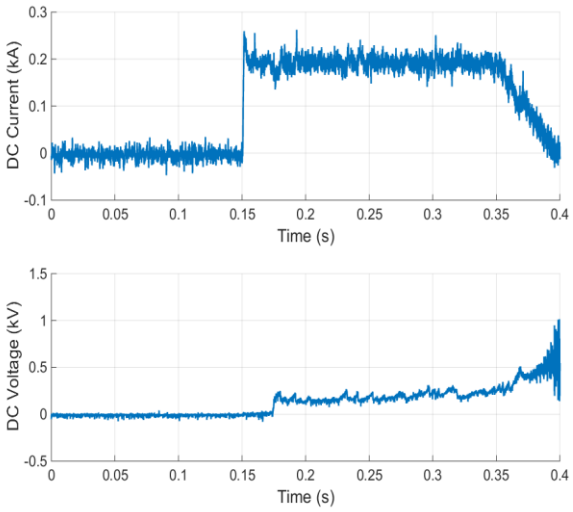
Figure 3.1 Arc fault test through ignition wire [51]

Due to the fact that the converters can run at different mode (voltage source mode (VSM) versus current source mode (CSM)) before and after fault occurs, it will be helpful to know how the characteristic of arc may vary regarding these two different modes. Figure 3.2 (a) shows an example of the arc voltage and arc current measured under VSM. The dc voltage across the electrodes was stepped from 0 to 6 kV at 0.1 s and then stepped back down to 0 kV after an additional 0.2 s. It is obvious that arc was formed rapidly once the testbed is energized, and lasted until the system is de-energized. The arc current varies from 200 A to 240 A, and the arc voltage varies around 100 V. Comparatively, Figure 3.2 (b) shows the measurements under CSM. The current was stepped from 0 to 200 A, and ramped down to 0 at 4 kA/s (limited by the power converter hardware settings) after 0.2 s.

It can be seen that the arc behaves differently as there is much less current overshoot at the initial phase of arc for the CSM than the VSM. This is one important reason why CSM is chosen over VSM when it comes to fault current limiting.



(a) Voltage source mode



(b) Current source mode

Figure 3.2 Arc current and voltage measured during test.

3.2 ARC BRANCH MODEL

The next step is to develop an arc model based on the test data taken by staff and researchers at CAPS [51]. Considering the highly randomness of arc behavior along with large measurement noise, a model of dc arc is in need for evaluating the effectiveness of the impedance-based LIFP method. This model should reveal how the arc impedance is related to factors such as arc current and arc length, so that the range of fault impedance, which is the key in this study, can be found regarding a wide variety in fault conditions.

Figure 3.3 shows a dc arc branch model derived from a hyperbolic approximation of the voltage and current trajectory of arc fault in dc microgrids [52]. This model consists of a resistance r in series with an EMF source V_0. The arc voltage can be represented as:

$$V_{arc} = v_0 + r * i = V + \Delta v + (R + \Delta r) * i \tag{3.1}$$

Where V and R represent the mean value, Δv and Δr represent the randomness in each component as:

$$v_0 = V + \Delta v \tag{3.2}$$

$$r = R + \Delta r \tag{3.3}$$

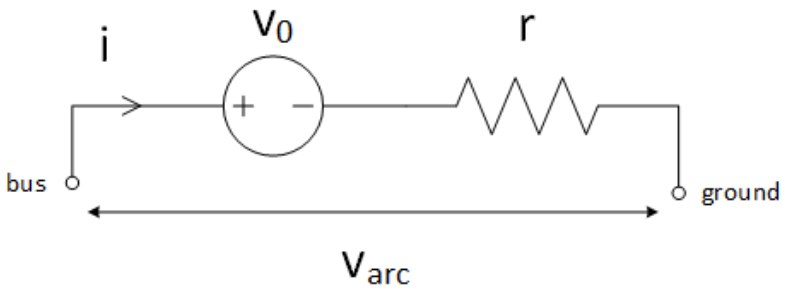


Figure 3.3 An dc arc branch model

The dynamic resistance in the arc model can be obtained through:

$$dv_{arc}/di = r = R + \Delta r \tag{3.4}$$

Thus, the built-in EMF source can be calculated via (3.1). For the arc test Figure 3.4 shows the probability density function and normal distribution fitting for 3600 sets of data regarding the built-in EMF source of arc calculated via (3.1)-(3.4) using a 1 kHz low pass filter. The two plots show good agreement in pattern. The mean value μ given by the normal (Gaussian) distribution fitting equals to 100.5 V.

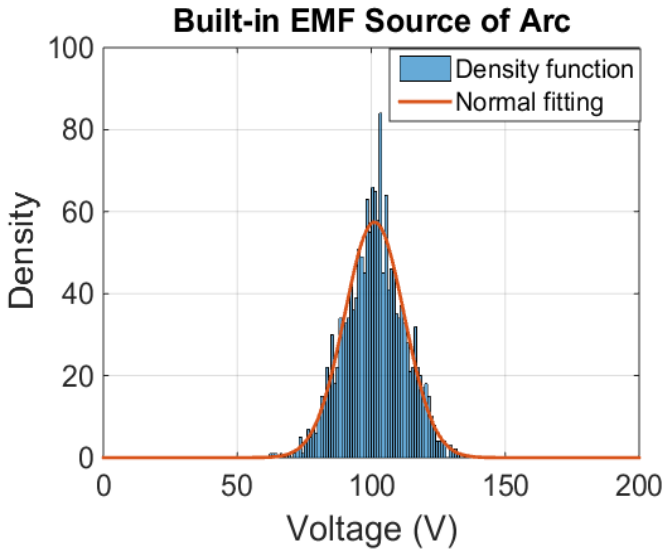


Figure 3.4 Density function and normal distribution fitting of the built-in EMF source in the arc model

Similar tests with larger (3.5 inch) gap between electrodes have been carried out to explore the distribution function of the built-in EMF source of the arc. Figure 3.5 compares the normal distribution fitting of the built-in EMF source at different currents (50 A, 100 A, 200 A). Apparently, the mean value μ of the built-in EMF source increases

with the arc current as also shown in Figure 3.5, while the standard deviation σ is in an inverse correlation with the arc current.

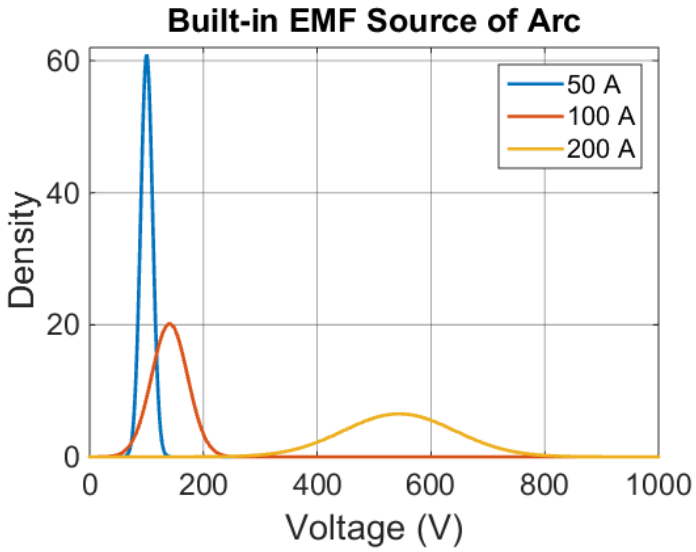


Figure 3.5 Normal distribution fitting of the EMF source of arc at different currents

Previous researchers have proposed various kinds of dc arc models, which were derived based on large amount of repetitive data through experiments, such as the Nottingham equation, the Stokes and Oppenlander equation, and the Paukert equations [53][54]. In Nottingham's study, the arc voltage for fixed arc length of 10 mm with copper electrodes is defined as a combination of a constant voltage drop and an exponential term related to the arc current [55]:

$$V_{arc} = 27.5 + 44 \cdot {I_{arc}}^{-0.67} \tag{3.5}$$

Stokes and Oppenlander also investigated the V-I characteristics of dc arc regarding different gap length (5 mm~500 mm) over a wide range of arc current (1 A~10 kA) through hugh amount of arc tests, including horizontal arc in open air with copper

electrodes and vertical arc in open air with aluminum electrodes. The arc voltage is found to decrease as the current level increase before a transition level, and increase after the transition level (10 A~100 A) which is related to the gap length. Their arc model removes the constant voltage drop, and defines that the arc voltage (so as the impedance) varies linearly with the length of gap L when the current is above transition level [53]:

$$V_{arc} = (20 + 0.534 \cdot L) \cdot {I_{arc}}^{0.12} \tag{3.6}$$

$$R_{arc} = (20 + 0.534 \cdot L) \cdot {I_{arc}}^{-0.88} \tag{3.7}$$

Similarly the Paukert equations provides very straightforward formulation of arc voltage and arc impedance in terms of arc current (ranged from 100 A to 100 kA):

$$V_{arc} = a \cdot {I_{arc}}^{b} \tag{3.8}$$

$$R_{arc} = a \cdot {I_{arc}}^{b-1} \tag{3.9}$$

Where a and b are both determined by the length of electrode gaps (ranged from 1 mm to 200 mm) [53]. A comparison of these three models shows that the arc impedance decreases nonlinearly with the increase of the arc current. However the arc impedance is highly unpredictable, and the three models show large discrepancy when current is less than 1 kA [55].

Figure 3.6 compares the test data with the Paukert equation and the Stokes and Oppenlander equation regarding the average value of arc impedance for different arc current when the length of gap is 88.9 mm (3.5 inch). It can be found from the test data that the arc impedance drops as the arc current increases from 100A to 300A. This can be explained as higher current level of arc will generate more heat, which can bring in more metal materials that evaporated from the electrodes to form a more conductive arcing

channel. However, as current level approaches to 400A, the arc impedance turns to increase, which may be caused by other factors such as the turbulence of air under higher temperature. Curve fitting of the test data shows a similar pattern compared to the other two models, though they are different in magnitude. Hence the steady-state arc impedance over the span that the arc current is from 100 A to 400 A:

$$R_{arc} = 79 \cdot {I_{arc}}^{-0.83} \tag{3.10}$$

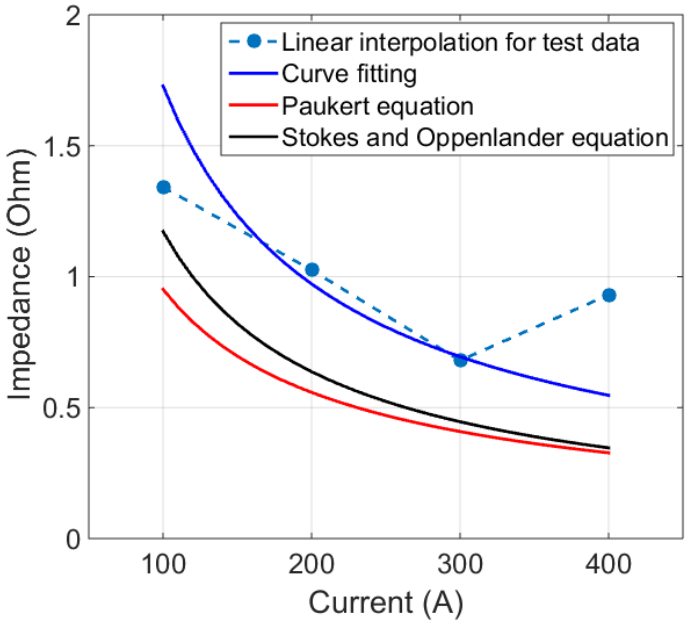


Figure 3.6 Comparison of test data with arc models regarding average value of arc impedance for different current level (length of gap at 88.9 mm)

The relationship between arc impedance and length of gap has been revealed in Figure 3.7, which is also based on data acquired through the experiments. There were two trials for each test point. The average value of arc impedance was calculated through the voltage and current measurements over a certain period of time (50ms) when the arc fault was relatively stable across the gap. It can be seen from Figure 3.7 that the average value of arc

impedance increases as the length of gap increases from 3.5 inches to 8 inches. This result can be explained as the increase of length of gap will result in the increase of arc length, and eventually cause the increase of arc voltage (as long as the source voltage is larger than the arc voltage). Calculations through the Paukert equation and the Stokes and Oppenlander equation show similar pattern that the arc impedance increases linearly with the length of gap. Thus an arc model with similar form of (3.7) is chosen based on the result in (3.10):

$$R_{arc} = (c + d \cdot L) \cdot {I_{arc}}^{-0.83} \tag{3.11}$$

The factors of equations (3.11) for the arc model can be obtained through curve fitting as show in Figure 3.7, so as the steady-state arc impedance over the span that the arc length is from 88.9 mm to 203.2 mm (3.5 inch to 8 inch):

$$R_{arc} = (44.9948 + 0.4634 \cdot L) \cdot {I_{arc}}^{-0.83} \tag{3.12}$$

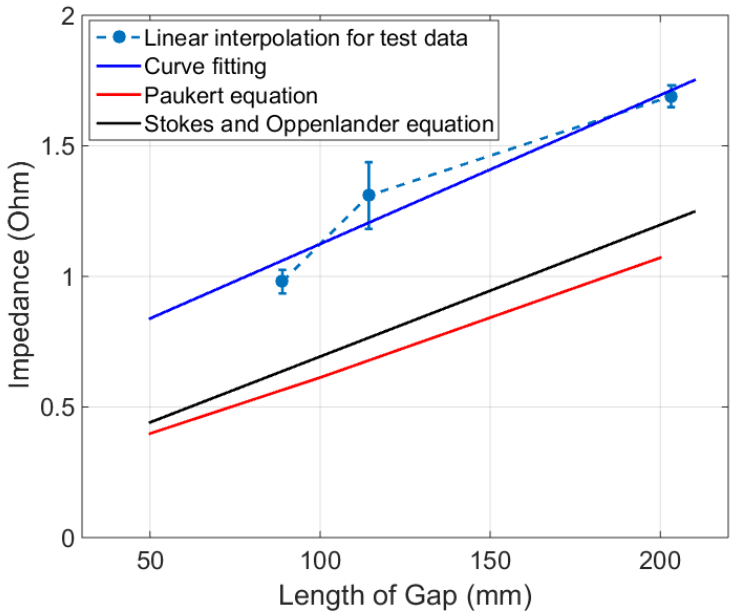


Figure 3.7 Comparison of test data with arc models regarding average value of arc impedance for different length of gap (current level at 200 A)

Apparently, these factors have different values compared to those formulated in (3.7). It can result from the highly dependency of arc impedance on various factors other than the length of gap and arc current, such as ambient temperature, electrode material, electrode configurations and etc. This finding further supports the fact that the arc characteristic can vary dramatically under different circumstances. Thus the problem in a circuit protection system is that a very broad range of all possible short-circuit arcs need to be correctly identified. Figure 3.8 lists the arc impedance for arc length from 1 mm to 300 mm and currents from 100 A to 10 kA based on the proposed model (3.12). The arc impedance is found can vary from 0.1 Ω to 4 Ω.

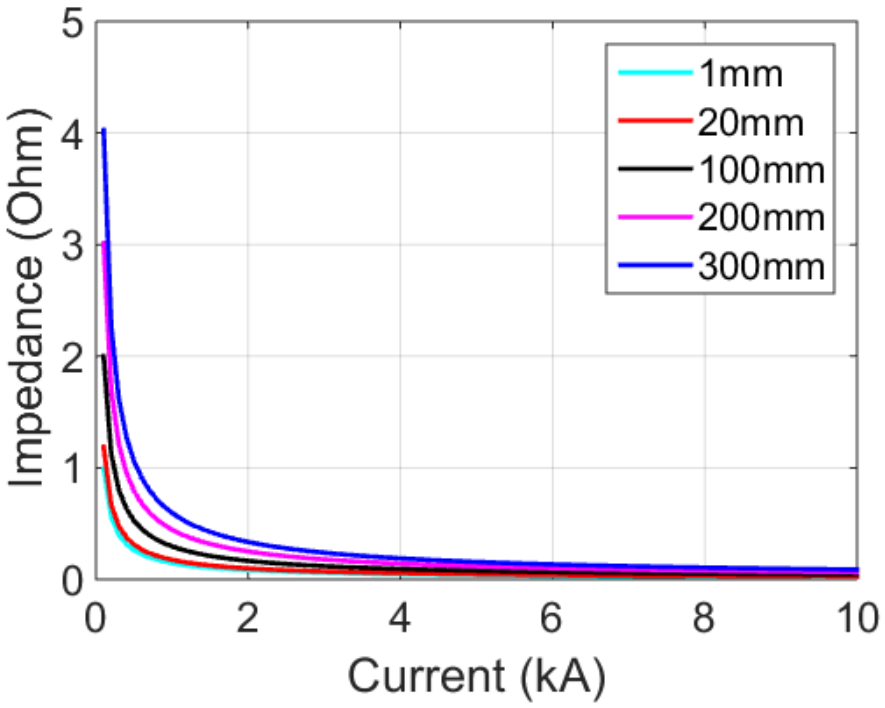


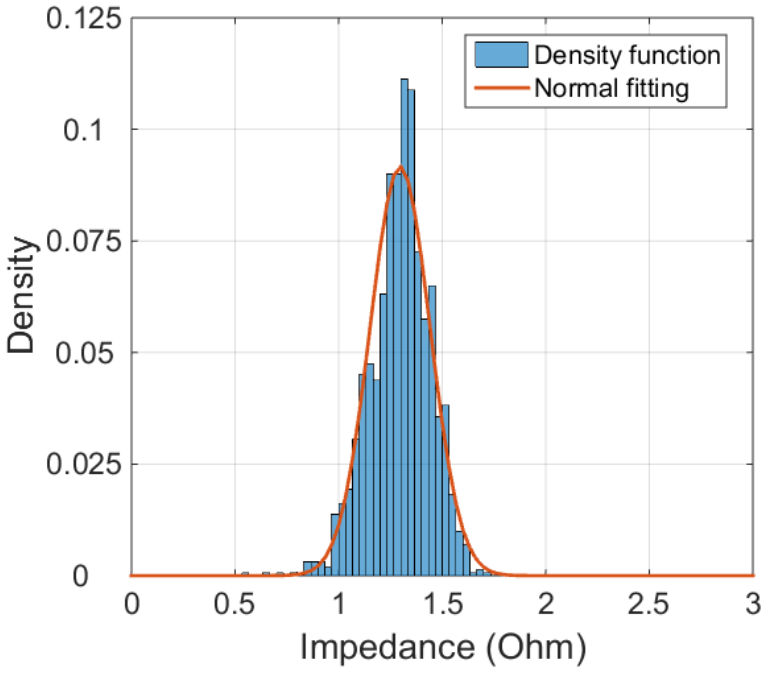
Figure 3.8 Arc impedance for different currents and arc length

Due to the highly randomness of arc impedance in time even when the arc is relatively stable, the distribution pattern of arc impedance in time is investigated to help form a more

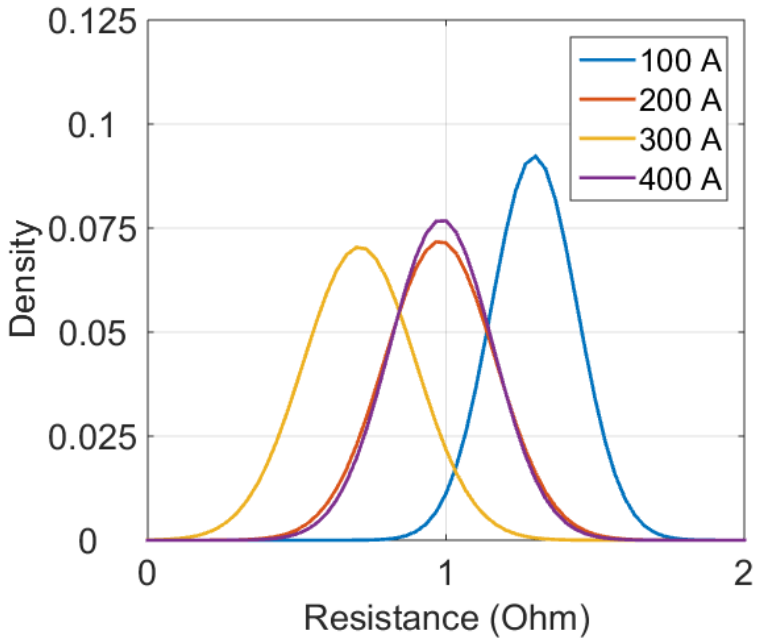
detailed arc model. Figure 3.9 (a) shows the probability density function and normal distribution fitting for 1600 sets of arc impedance data calculated through voltage and current measurements. The probability density of the normal distribution is described as:

$$f(x|\mu,\sigma^2 = \frac{1}{\sqrt{2\sigma^2\pi}}e^{-\frac{(x-\mu)^2}{2\sigma^2}}) \tag{3.13}$$

Where μ is the mean value, and σ is the standard deviation. Again it is an arc across 88.9 mm (3.5 inch) gap with current reference at 100A. A low pass filter was used for reducing measurement noise so the bandwidth is limited at 1 kHz. These two plots show good agreement in distribution pattern. Moreover, Figure 3.9 (b) compares normal distribution fittings of arc impedance regarding different arc current. Apparently μ falls into the range from 0.1 Ω to 4 Ω as discussed, while σ, which indicates the noise level of the arc impedance, is within the range from 0.15 to 0.19.



(a) Density function and normal distribution fitting of arc impedance



(b) Normal distribution fitting of arc impedance regarding different current

Figure 3.9 Statistical distributed behavior of arc impedance

It should be noticed that the characteristic of arc fault varies case by case in the dc systems. The behavior of the arc can still be affected by a combination of electrical, magnetic, thermal, dimensional and material factors other than current and arc length, so as it is difficult for an arc model to represent universal arc faults that may happen in the dc system. However, this analysis gives a general idea of how the dc arc may behave in such fault events. Also the upper and lower limits of likely arc impedance properties are obtained, so as the functionality of LIFP can be evaluated out to these limits. The normal distribution model (3.13) for the arc impedance is adopted for the following study to include the impact from arc noise.

CHAPTER 4

COORDINATION OF PROTECTION SCHEMES IN MVDC SYSTEMS

Conventional ac systems generally rely on mechanical breakers to interrupt fault current and eventually isolate the faulted section from the whole system. However when it comes to dc systems, especially MVDC system, this strategy may encounter with big problems, because it is rather difficult to extinguish dc arc across the contacts of breakers/switches as there is no natural zero-crossing for dc current. Some electronic circuit breakers, such as Z-source solid state circuit breakers, have been proposed in literatures as alternatives [56]-[58] because they don't arc and therefore are not susceptible to faults of arcing contacts. But they can have drawbacks in terms of conduction loss and voltage oscillations.

Another solution is to design an MVDC system which operates without breakers [59]. Instead, the fault current can be brought down to zero via power converters. Thus this protection scheme relies on coordinated control of power converters and non-fault-breaking mechanical disconnect switches to effect the fault clearance process— fault detection and localization, complete de-energizing of the system, isolation of faulted branch and re-energizing of the system [60]-[63]. On top of this fault protection scheme, the fault localization can be accomplished via various fault location methods categorized in Section 2.2. One proposed solution for an MVDC shipboard system is to combine a communication-dependent method with a communication-independent method: The

CFP method depends on communication between distributed sensors and a central decision-making authority to achieve fastest primary protection. It is backed up by a local response function LIFP that takes over in case of failure in the primary method.

4.1 PROTECTION PROCEDURES OF THE FAULT CLEARANCE

Due to the breakerless feature of the MVDC system, the fault clearance sequence is defined as follows [48]:

a. Fault detection and localization – When a fault happens, all power converters that feed the ring bus will be forced into current-limiting mode by their built-in overcurrent protection scheme. Then both CFP and LIFP will work independently to detect and locate the fault.

b. Completely de-energizing of the system – After the fault location is identified, the system will be completely de-energized.

c. Isolation of faulted branch – Corresponding disconnect switches will be actuated to open once the initial discharge current from all the capacitance in the MVDC system decays to zero thus isolating the faulted section.

d. Re-energizing the system – After the fault is isolated by proper operation of switches, the converters re-energize the system.

Figure 4.1 shows the generic voltage and current waveforms at the source during such a fault clearing process. The idea is to force the power converters to first go into current-limiting mode (t0), identify the fault location (via CFP and/or LIFP) (t1), then shut-down all sources (i.e.de-energize the system) after a preset time delay (t3), open the appropriate disconnect switches (t4) and finally re-energize the remaining healthy system (t6). The target for the full system response time (SRT), which includes the whole fault clearance

process, has been chosen aggressively as 8ms (equivalent to approximately one half of a 60 Hz cycle). However, even a SRT of 10 times that target will still provide a viable alternative to systems which are based on dc or ac side circuit breaker action. Not only are the fault currents limited to approximately the rated currents of the converters, the non-current-breaking disconnect switches are expected to be much more compart and more efficient compared to dc circuit breakers which are expected to be solid-state based. The function of limiting fault currents by a modular multilevel converter has already been demonstrated at MV levels and is described in [64].

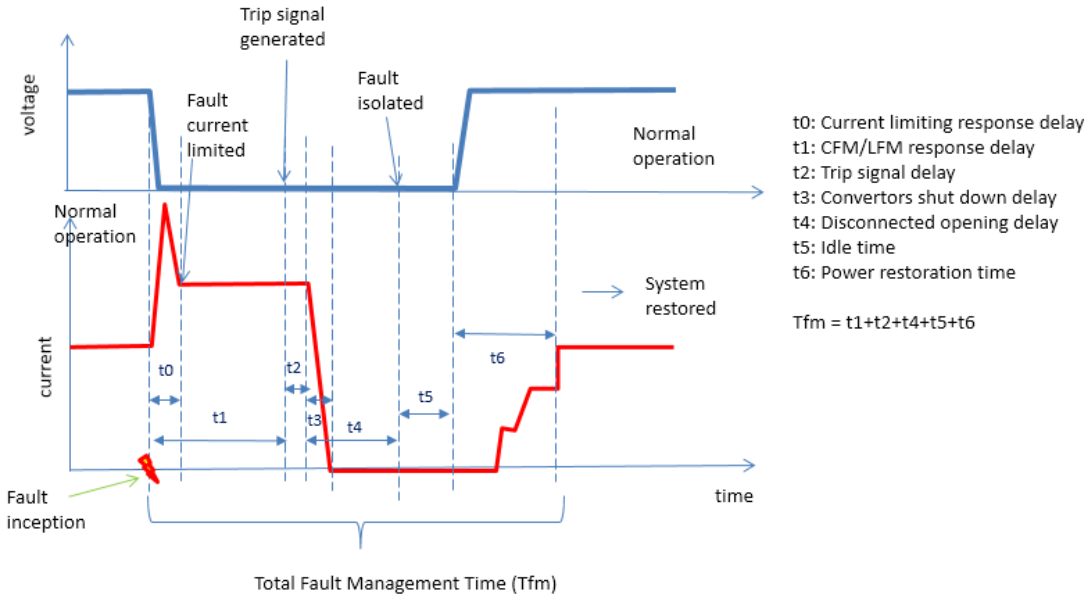


Figure 4.1 Conceptual view of the protection procedures for the MVDC system

4.2 IMPLEMENTATION OF FAULT PROTECTION CONTROLLERS

The MVDC system shown in Figure 4.2 indicates that the ring bus is divided into several sections by dc switches, so as to render the ring bus capable of maintaining its function of providing distribution routes for power generated from the generator cells to

major loads even when one section is cut off from the whole system. Also, it is necessary to notice that these dc switches are assumed to switch off the circuit under zero current condition, instead of directly interrupting fault currents. This requires converters to follow sequences b&c mentioned in Section 4.1, and reduce the fault current to zero. In this manner, switches will not endure high current arcs during its operation.

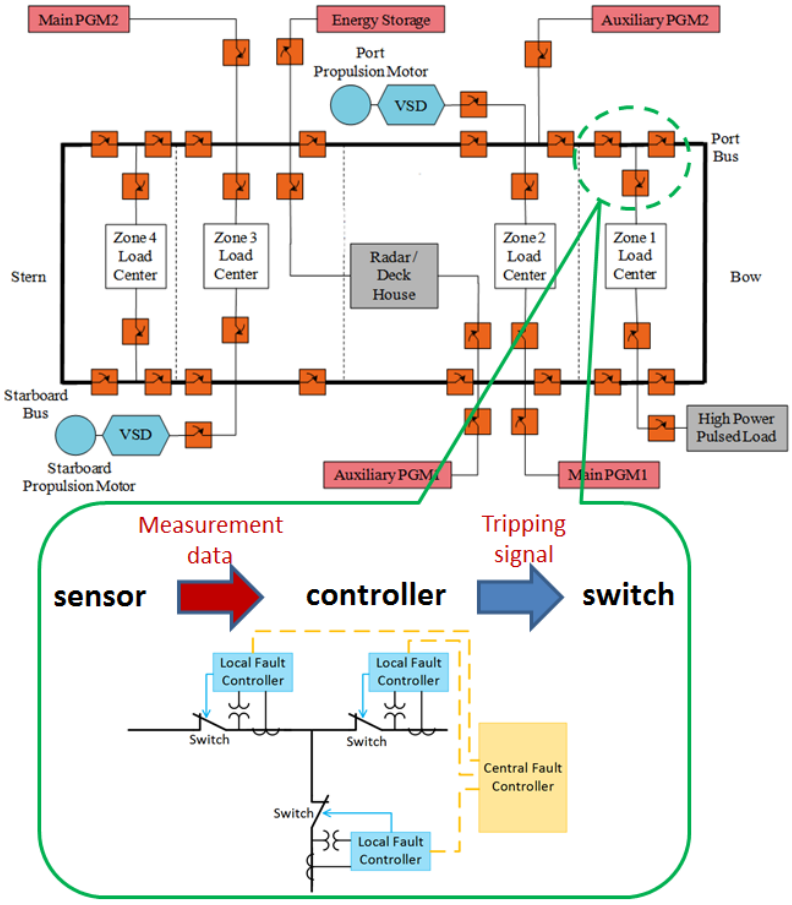


Figure 4.2 Implementation of Fault Protection Controllers

The CFCs and LFCs are deployed at different locations. The two CFCs (or more, depending on the size of the MVDC system) implemented remotely from the dc switches rely on communication to achieve their central decision-making ability, whereas the LFCs

implemented at each dc switch fulfill their local decision-making ability while only relying on the data obtained locally. Figure 4.2 shows the implementation of the central fault controller and local fault controller at a T-intersection of the system. The measurement data obtained through the sensors are both sent to the central fault controller and local fault controllers. The operation decision for protection is made in each controller separately, and the generated tripping signal is sent to the corresponding switch in a separate way as well. There exist interconnections from the central fault controller to all the local fault controllers that it covers, so the local fault controllers know whether or not the central fault controller is on duty.

The biggest advantage of LIFP over CFP lies in its independence of peer-peer communication. A LFC is implemented at each dc switch locally, and all the measurement and data processing are performed locally. In this manner, each switch is able to make its own decision for operation based on its local LIFP unit, even under the condition when the communication system is severely interfered or damaged, and CFP could most likely be paralyzed. Nonetheless, the price LIFP paid is its limited adaptability to a rapidly varying system due to its slower updating rates of presetting.

4.3 COORDINATION OF FAULT PROTECTION SCHEMES

The two protection schemes will work independently, but in a coordinated way. The coordination between the two schemes is implemented through operating speed. When a fault occurs, the CFP shall determine the presence of a fault in the shortest possible time. The current target for this is around 5ms. If it fails, the LIFP will take over the task after a preset time delay, and then determine the presence of a fault (expected within another 10-20ms).

Table 4.1 Comparison Of LIFP And CFP

	Local Information Based Fault Protection (LIFP)	**Centralized Fault Protection (CFP)**
Algorithm	Adapted distance protection	Adapted differential protection
Communication media	Local communication through dedicated channels	Wide area communication through shared channels
Devices	20-40 distributed controllers	2 or 3 central controllers, plus 20-40 distributed controllers
Data need to be processed	Local measurement data	Global measurement data
Target actuating time	After a preset time delay	As soon as fault is detected
Target tripping time	10-20ms	5ms

Table 4.1 categorizes the characteristics of CFP and LIFP for comparison. It is important to know that CFP and LIFP are separate fault protection schemes which only share voltage sensors and current sensors at each dc switch for data acquisition purposes. Though LIFP does not require far end communication among switches like CFP, it still needs local communication among a voltage sensor, a current sensor and a local controller, thus data obtained from the measurement can be sent to the local controller.

To validate not only that the CFP and LIFP can work independently but also that they can perfectly integrate and are compatible with each other, an overall shipboard power system was first modeled as shown in Figure 4.3 and simulated within a MATLAB-Simulink environment. It is described as a 5kV system including two generation sets and two loads rated at 4MW each, while all sharing a closed-loop ring bus for power distribution purposes. The test-bed cable impedances are scaled representations of anticipated MVDC bus impedances onboard a full-scale ship, which can refer to [21]. The

cable resistances are all at the milliohm level, which is much smaller than the load resistance (6.25Ω). Thus the major voltage drop is across the load, and every node of the ring bus is able to maintain its voltage level close to the rated voltage (5kV) during normal operation mode. On the other hand, it explains why the introduction of a short circuit or low impedance fault will render current flow in the ring bus to easily change direction.

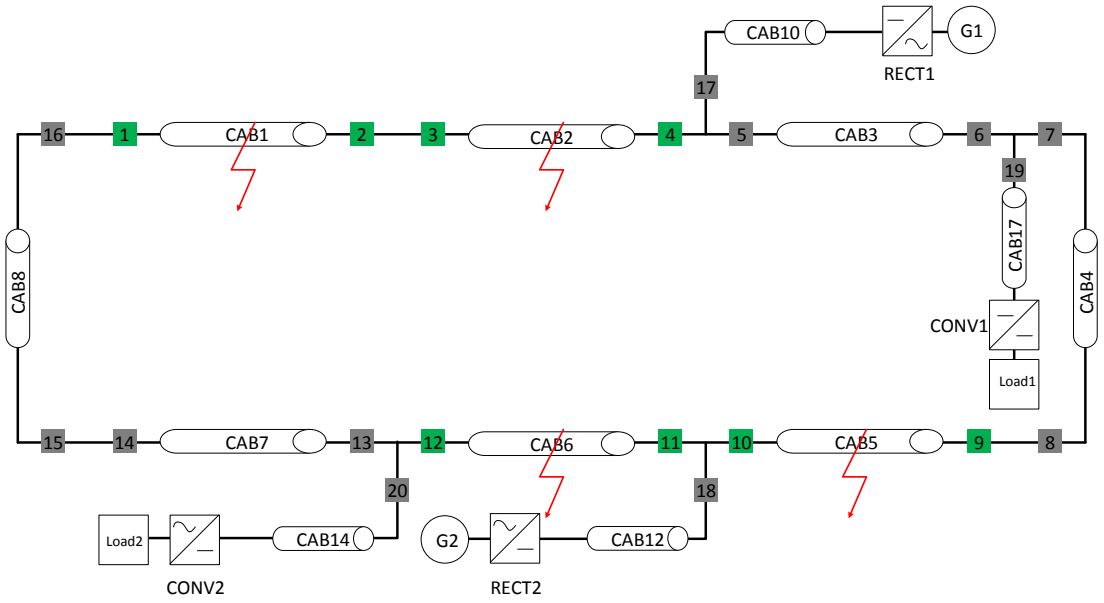


Figure 4.3 Shipboard Power System Model for Coordination Test

Figure 4.4 shows the comparison of apparent resistances at switch terminals 1 through 20 for five different scenarios, which are fault at the center of CAB1, CAB2, CAB5, CAB6 (refer to Figure 4.3) and no fault condition. When a fault happens at the ring bus, apparent resistances seen at all switch terminals (except for switches at load branches) will decrease significantly due to the contribution of a low impedance path to ground, so that all these switches sense a fault event.

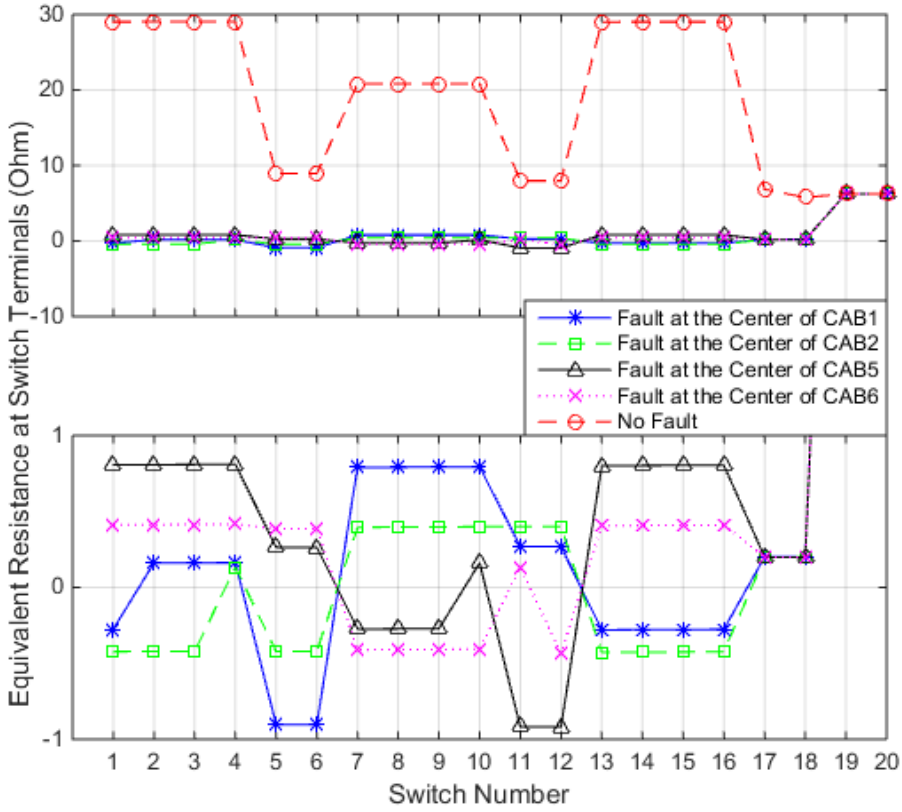


Figure 4.4 Comparison of Apparent Resistance at Switch Terminals 1-20 for Fault at the Center of CAB1, CAB2, CAB5, CAB6 and No Fault Condition

Meanwhile, Figure 4.4 indicates the apparent resistance can drop below zero which is due to the change of current flow direction under certain fault conditions. Unlike the tripping characteristics of conventional distance protection, the apparent resistance at a switch terminal doesn't always display the lowest value for the closest fault. Take Switch 1 and 2 for example, the apparent resistance at the switch terminal is smaller when a fault occurs at CAB2 than when a fault occurs at CAB1 as shown in Figure 4.5. This result further consolidates the assumption we've drawn that both a positive threshold and a negative threshold are necessary instead of just one.

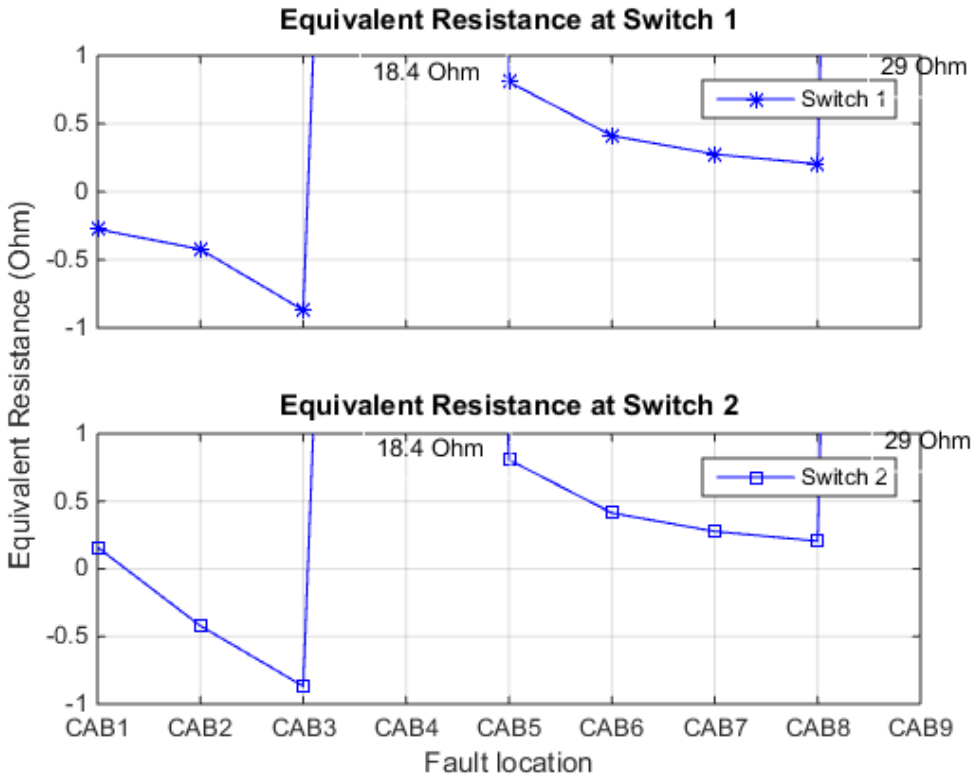
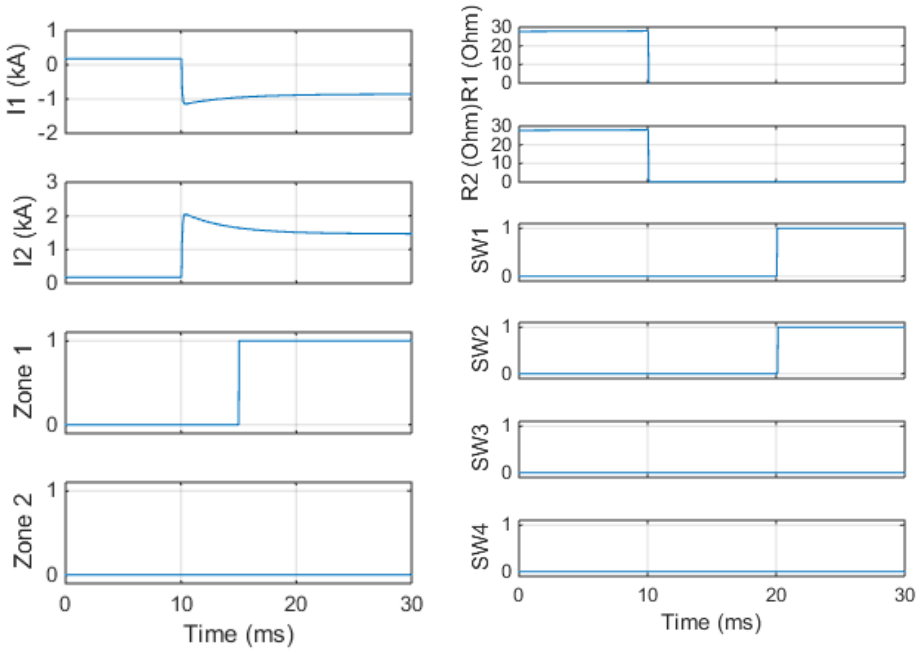


Figure 4.5 Apparent resistance at Switch 1 & Switch 2 for Different Fault Locations

Figure 4.6 shows the CFP and LIFP in response to a fault at the center of CAB1. When fault occurs at 10ms, the current through Switch 1 (I1) and the current through Switch 2 (I2) experience a dramatic change, which are shown in the subplot 1&2 of Figure 4.6 (a) respectively. Subplot 3&4 indicate CFP rapidly responding to the fault, and actuate a tripping signal to its protection Zone 1, which includes Switch 1 and Switch 2, 5ms after the fault event. Likewise, LIFP is capable of responding to this fault in a proper way. The apparent terminal resistance of Switch 1 (R1) and the apparent terminal resistance of Switch 2 (R2) almost instantly drop to a much lower value when a fault occurs, shown in subplot 1&2 of Figure 4.6 (b). Hence LIFP is able to detect and locate the fault and send

tripping signals to Switch 1 and Switch 2 within 10ms, while making Switch 3 and Switch 4 remain closed, shown in subplot 3-6 of Figure 4.6 (b). However it should be pointed out here that, LIFP is able to detect and locate the fault as fast as CFP. The reason for adding extra time delay (5ms) at LIFP is to follow the pre-defined role of CFP and LIFP for fault protection: the CFP, working as primary protection, will respond to fault in 5ms, yet if it fails, LIFP, acting as backup protection, will take over the duty in another 5ms.

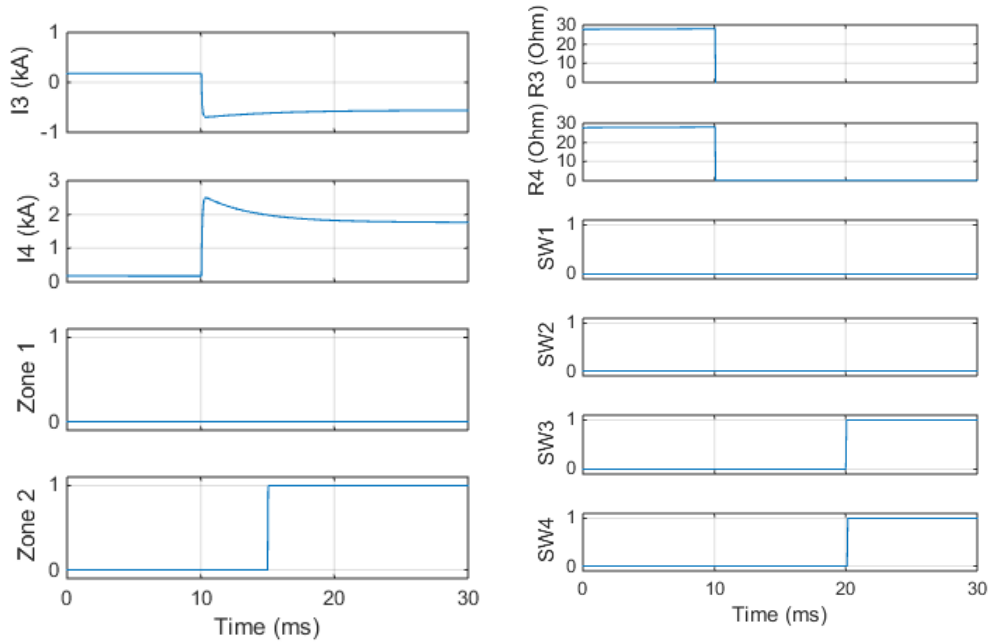


(a) Response of CFP (b) Response of LIFP

Figure 4.6 Responses of CFP&LIFP to Fault at CAB1

Figure 4.7 shows the CFP and LIFP in respond to a fault at the center of CAB2. CFP is able to respond to the fault correctly by actuating a tripping signal to its protection Zone 2, which includes Switch 3 and Switch 4. Also LIFP can detect and locate the fault in a

timely manner. This further validates that CFP and LIFP can function properly in the MVDC system and are perfectly compatible with each other.



(a) Response of CFP (b) Response of LIFP

Figure 4.7 Responses of CFP&LIFP to Fault at CAB2

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CHAPTER 5

LOCALIZED FAULT PROTECTION FOR ARC FAULTS

The previous chapter reveals the impact of pure resistive short circuit fault to the MVDC system [48]. Similarly, this section aims to discuss how the system will behave when it comes to arc fault, and to what degree the system behavior may vary for different fault location. The result shows that, LIFP is found to be capable of clearing fault at various locations, including source branch, load branch and main bus. There are no cases where a fault was not disconnected from the system, and only a few cases where loads lost power when they optimally should not have.

5.1 A BASELINE MVDC SYSTEM

In order to test the system response to the arc fault model developed in Section 3.2, a baseline MVDC system as shown in Figure 5.1 is built in MATLAB/Simulink. It is derived from the system diagram shown in Figure 2.1 (which is assumed to be always operating with open-loop ring bus no matter in pre-fault or post-fault condition) as a more generic example for the verification and validation of the protection scheme.

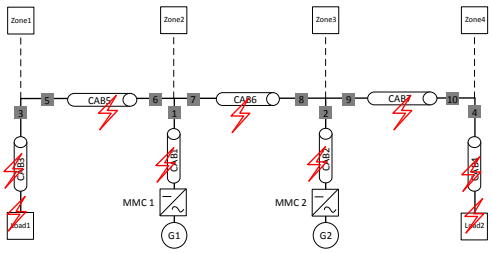


Figure 5.1 A baseline MVDC system

This system consists of two generation units interfaced with two AC/DC MMCs, two major resistive loads, and several distributed loads. Sectionalizers (dc disconnect switches) are placed at each end of each cable section on the ring bus, and at the connecting end of the cables on branches connected to the ring bus. Table 5.1 lists the system parameters and the reference settings for the converters in different operating modes.

Table 5.1 System Parameters

Parameters	**Symbols**	**Values**
DC bus reference voltage	V_{ref}	5 kV
Nominal power of Load 1, Load 2	P_{Load1}, P_{Load2}	4 MW
Apparent load resistance	R_{Load1}, R_{Load2}	6.25 Ω
Current limit of MMC 1, MMC 2 at normal operating mode	I_{limit}	1200 A
Current limit of MMC 1, MMC 2 at current limiting mode	I_{limit}'	160 A

The cables ratings and sizes are chosen based on system configuration, such as the maximum current flow and the physical length for corresponding bus segment [21]. Table 5.2 categorizes the cable impedance regarding different section and length [48].

Table 5.2 Cable Parameters

Section (mm^2)	**Length (m)**	**r (mΩ/m)**	**L (μH/m)**	**R (mΩ)**	**L (μH)**
223	10	0.426	0.183	4.26	1.83
	50	0.426	0.183	21.3	9.15

	100	0.426	0.183	42.6	18.3
	200	0.426	0.183	85.2	36.6
400	10	0.0283	0.46	0.283	4.6
	50	0.0283	0.46	1.415	23
	100	0.0283	0.46	2.83	46
	200	0.0283	0.46	5.66	92
630	10	0.047	0.48	0.47	4.8
	50	0.047	0.48	2.35	24
	100	0.047	0.48	4.7	48
	200	0.047	0.48	9.4	96

Arc fault occurs in the baseline MVDC system is represented by the arc model derived in Section 3.2. The average resistance of the arc is chosen to vary from 1 Ω to 4 Ω, while the standard deviation of arc resistance, which indicates the noise level, is chosen within the range from 0.15 to 0.19. Figure 5.1 also indicates various locations to inject the arc fault, including the source branch cable, the load and ring bus.

5.2 CURRENT LIMITING TO ARC FAULT VIA CONVERTERS

No matter at what location the fault occurs, all the power converters that feed the ring bus will be forced into current-limiting mode once they detect an overcurrent scenario. Figure 5.2 shows the simulation result of voltage and current waveforms at the output of MMC 1and MMC 2 when an arc fault occurs at Load 1 (refer to Figure 5.1). There is simultaneously a voltage drop and a current rise beginning at the fault incident at 5ms. The oscillation of the curves is contributed by the arc noise discussed in Section 3.2. The rectifiers, which were originally operating at voltage source mode, go into current-limiting mode one discontinuous step (50μs) after the output current reaches 1.2 kA (150% of the rated value), and bring down the fault current to a safe value (in this notional case to 20% of the rated value) within 10 ms.

Notice here that the fault current is contributed by two main factors: a fast peak current due to the discharge of capacitors and a slow decaying current due to the discharge of inductors. Due to the fact that dc switches are assumed to only open at zero current, the value of line capacitance and inductance can affect the idle time that fault protection scheme needs before switches can actually respond.

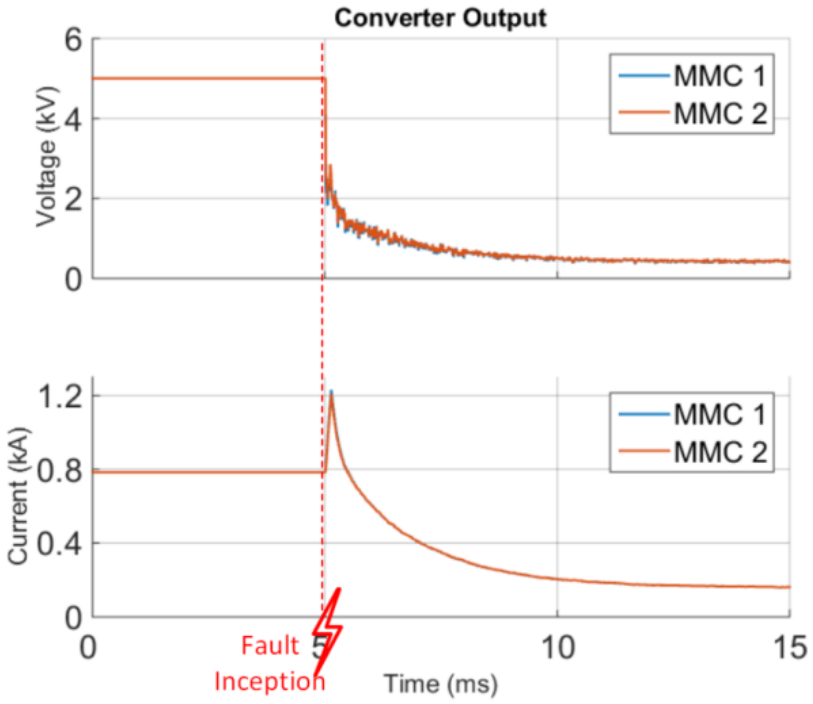


Figure 5.2 Voltage and Current at the Output of Power Converters to Arc Fault

5.3 LOCAL RESPONSE TO ARC FAULT

This localized fault protection scheme is communication- independent, which means not only each power converter but also each dc switch should be able to detect and respond appropriately to the arc fault based only on the information (bus voltage and current) obtained locally. Hence it is helpful to figure out how these parameters may vary

for a “healthy” condition versus arc fault occurs at various locations including cable at the source branch, cable at the ring bus, and load. The simulation is performed based on the system model proposed in Figure 5.1, and the arc model discussed in Section 3.2.

1) Arc fault at source branch cable: When arc fault occurs at the source branch CAB 1, Switch 1 at the source branch is expected to respond which means tripping signal should be generated at its local fault controller during the fault identification process, while all the other switches should remain closed. Figure 5.3 shows the voltage, current and impedance at the terminals of Switch 1, Switch 2 and Switch 3 respectively. Also, moving average filters are adopted to reduce both arc noise and measurement noise in the apparent impedance, so as a 2ms sampling delay will be introduced as shown at the bottom subplot in Figure 5.3. This sampling delay is determined by the sampling frequency of the local fault controller and the size of the average filter, which are 10μs and 200 in this notional case.

It can be observed that the terminal voltage at Switch 1, Switch 2 and Switch 3 all decrease significantly as soon as the arc fault occurs, so that they all sense the fault event. However, subplot 2 of Figure 5.3 indicates the current at these switches, though at the same level before the fault event, vary differently during the fault event: Current at Switch 1 reverses in direction as G2 is feeding the fault at CAB 1 through Switch 1; Current at Switch 2 reaches to the output current limit of MMC 2 (1.2 kA), and then be limited to 160 A, while current at Switch 3 decays to an even lower level due to the bypass of fault. Apparently, the reversed current at Switch 1 results in a negative apparent impedance at its terminals as shown in the subplot 3 of Figure 5.3. Therefore it is quite straightforward for

Switch 1 to differentiate arc fault at the source branch it connects to from those happen at other locations of the system.

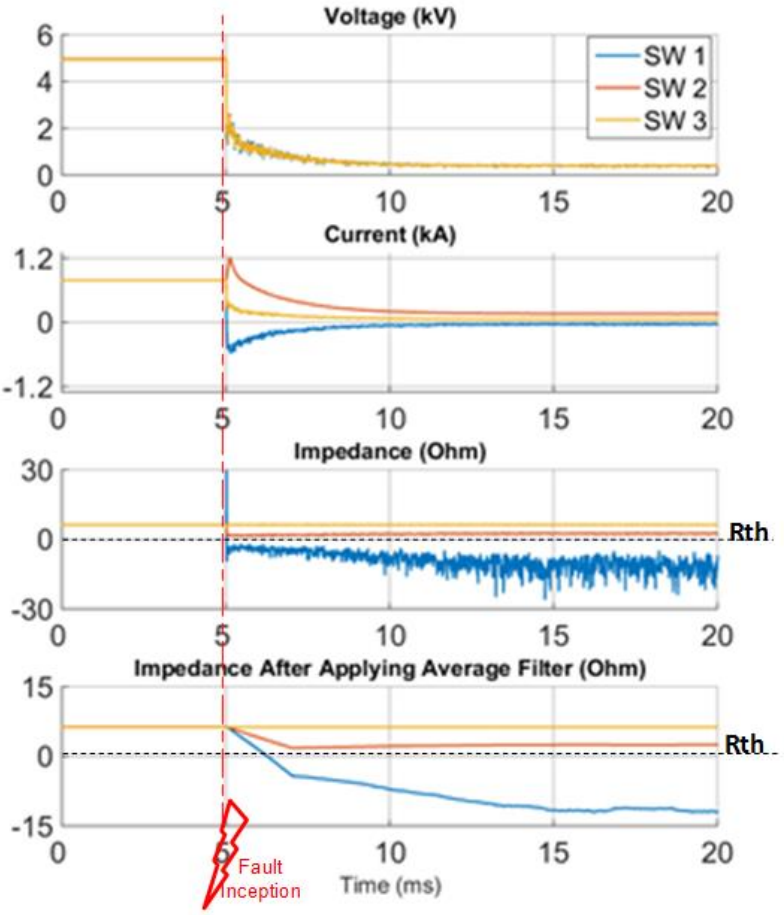


Figure 5.3 Arc Fault at Source Branch CAB 1

2) Arc fault at load: Figure 5.4 shows the voltage, current and impedance at the terminals of Switch 3, Switch 4 and Switch 7, when arc fault occurs at Load 1. The current at Switch 7 reverses in direction as G2 is feeding the fault at Load 1 through the ring bus CAB 6. The apparent impedance at Switch 3 drops from 6.25 Ω to a much lower value

(less than 2 Ω) as soon as the fault happens, because Load 1 is in parallel with the arc fault under this fault condition. Comparably, the apparent impedance at Switch 4 remains at the original level. Therefore, it provides a way for the switch at load branch to distinguish faults at the local branch from faults at other load branches.

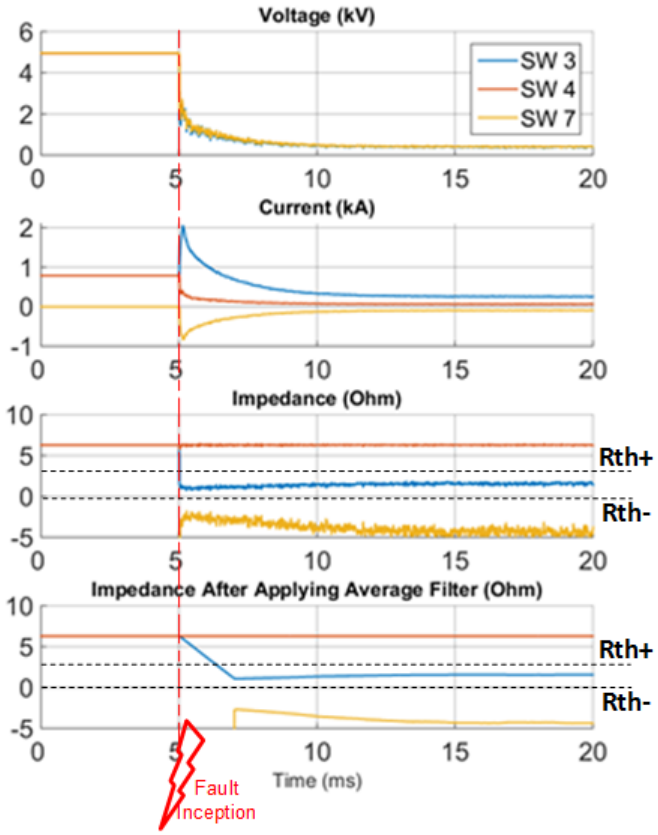


Figure 5.4 Arc Fault at Load 1

3) Arc fault at ring bus: It becomes tricky when arc fault occurs at the ring bus CAB 6. There is one dc switch placed at each end of CAB 6. And they are both expected to respond when there is a local fault. Figure 5.5 shows the impedance at the terminals of Switch 1drops to a much lower value while still remains positive, yet the impedance at Switch 8 turns to a negative value. These two switches will need both a positive and a negative threshold, as has been discussed in Section 1.2. It can also be observed that

impedance at the source branch Switch 1drops to a lower value as well, but Switch 1 will not trip as it is set to only react to fault at the corresponding source branch, in which case the impedance turns to be negative. Comparatively, impedance at load branch Switch 3 remains unaffected.

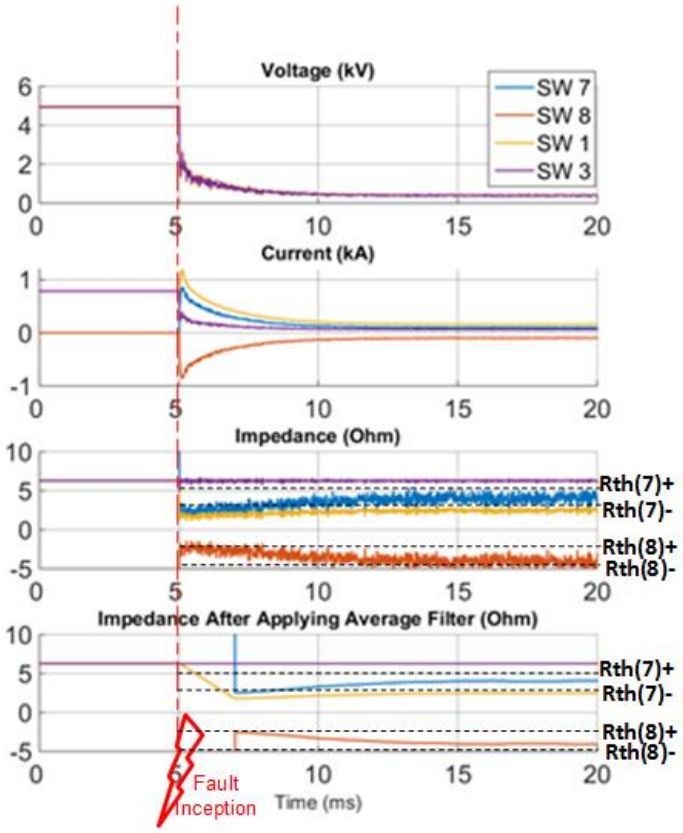


Figure 5.5 Arc Fault at Ring Bus CAB 6

In order to analyze all the cases discussed above, Table 5.3 lists the behavior of apparent impedance at switch terminals for various fault locations. "+" means the impedance drops to a lower positive value due to the fault event; "-" means the current direction reverses so as the impedance shifts to a negative value due to the fault event; "N" means the impedance stays at the same level during the fault event. It can be observed

from Table 5.3 that the impedance pattern discussed in the former paragraphs can be further applied to other cases.

Table 5.3 Apparent Impedance At Switch Terminals

Fault \ Switch #		1	2	3	4	5	6	7	8	9	10
Source Branch	CAB1	-	+	N	N	N	N	-	-	N	N
	CAB2	+	-	N	N	N	N	+	+	N	N
Load Branch	LOAD1	+	+	+	N	+	+	-	-	N	N
	CAB3	+	+	+	N	+	+	-	-	N	N
	LOAD2	+	+	N	+	N	N	+	+	+	+
	CAB4	+	+	N	+	N	N	+	+	+	+
Ring Bus	CAB5	+	+	N	N	N	+	-	-	N	N
	CAB6	+	+	N	N	N	N	+	-	N	N
	CAB7	+	+	N	N	N	N	+	+	+	N

5.4 COORDINATION OF SWITCHES

As been illustrated in previous studies [48], the dc disconnect switches can autonomously detect and locate the fault, which is achieved by constantly evaluating the apparent impedance at switch terminals through the local measurements. Moreover, there will be tripping thresholds setting of impedance values at the local fault controller for each switch. The value of the calculated apparent impedance is also constantly compared to these tripping thresholds, so that the local fault controller can decide whether or not to send tripping signal to the switch in the following fault-clearing sequence. Apparently, the key of LIFP is the coordination of all these thresholds settings. An optimized design solution is aimed to make each switch only react to a fault that happens within its

protection zone while ignoring any fault that happens beyond its protection zone. Therefore, it is necessary to investigate the characteristic of apparent impedance at switch terminals regarding different fault scenarios.

1) Switches at load branch: These include Switch 3 and Switch 4 as shown in Figure 5.1. Take Switch 3 for example, it is designated to isolate the branch of Load 1 from the system when fault occurs at Load 1 or Cable 3. Figure 5.6 shows the voltage and current waveforms at Switch 3 regarding fault at different locations of the system. Similar to what observed at converter terminals during fault scenarios, the voltage at Switch 3 will drop to a much lower value as soon as fault occurs. This indicates the switch can be aware of the fault event no matter where the fault occurs. However when fault occurs at the branch of Load 1, the current at Switch 3 will experience a sharply rise and stabilize at a higher value compared to those when fault occurs beyond the branch of Load 1.

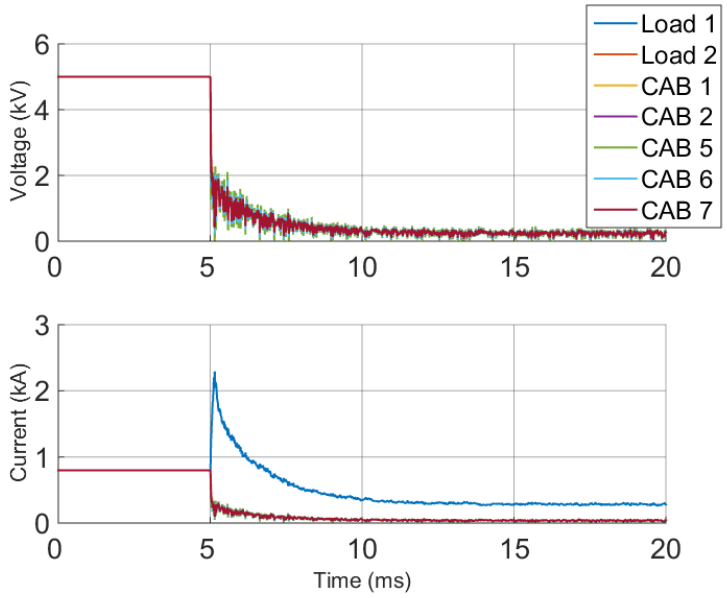


Figure 5.6 Voltage and Current at the terminals of Switch 3 regarding arc fault at different locations of the system

Figure 5.7 shows the apparent impedance at the terminals of Switch 3, which is calculated via the voltage and current measurement data shown in Figure 5.6. It can be seen from the first subplot of Figure 5.7 that, when fault occurs at the branch of Load 1, the mean value of the apparent impedance at Switch 3 will be much lower (0.84 Ω) than when fault occurs beyond the branch of Load 1 (6.25 Ω). However, due to the impact of arc noise, it is almost impossible to place a tripping threshold properly between these values without causing Switch 3 to mistrip for faults beyond its protection zone. Therefore, moving average filters are adopted to reduce both arc noise and measurement noise in order to extract the average impedance value for evaluation. The filtered impedance is shown in the subplot at the bottom of Figure 5.7, which has a much clearer margin between fault within the protection zone and fault beyond the protection zone. The 2ms sampling delay is determined by the sampling frequency of the local fault controller and the size of the average filter, which are 10μs and 200 counts in this notional case.

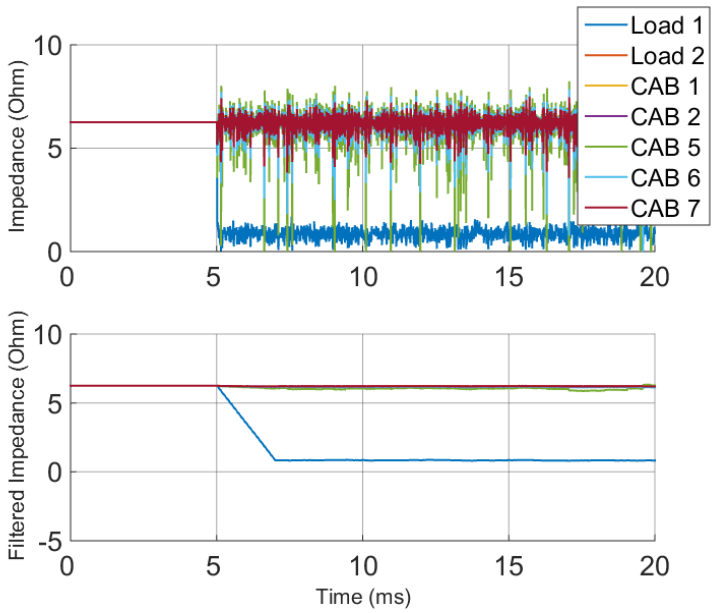


Figure 5.7 Apparent impedance at the terminals of Switch 3 regarding arc fault at different locations of the system (arc impedance 1 Ω)

Similar tests have been conducted with different types of arc faults. The apparent impedance at the terminals of Switch 3 for arc faults with different impedance level (0.1 Ω and 4 Ω) are shown in Figure 5.8 and Figure 5.9 respectively. It can be seen from these results that Switch 3 is capable of differentiating in-zone and out-of-zone faults for a very wide fault impedance range (from 0.1 Ω to 4 Ω). Figure 5.10 compares the apparent impedance at Switch 3 regarding different faults at the branch of Load 1, so as a tripping threshold can be easily defined within the margin (4 Ω to 6 Ω).

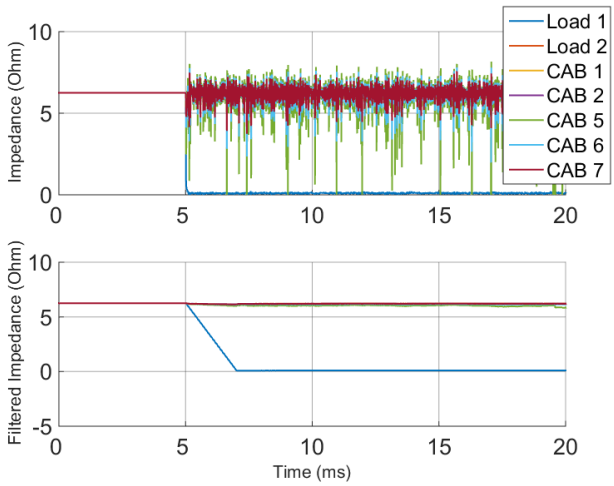


Figure 5.8 Apparent impedance at the terminals of Switch 3 regarding arc fault at different locations of the system (arc impedance 0.1 Ω)

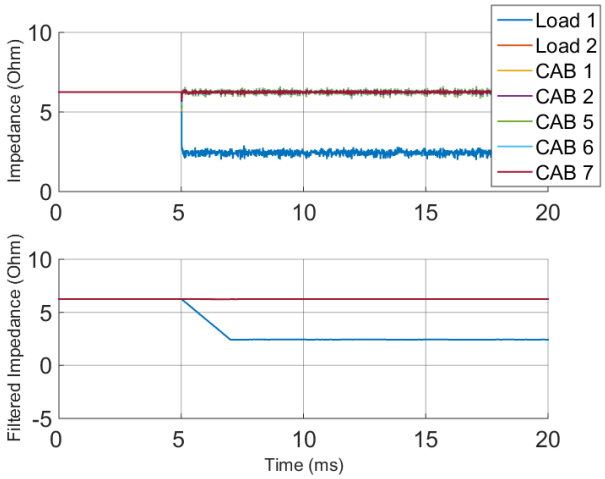


Figure 5.9 Apparent impedance at the terminals of Switch 3 regarding arc fault at different locations of the system (arc impedance 4 Ω)

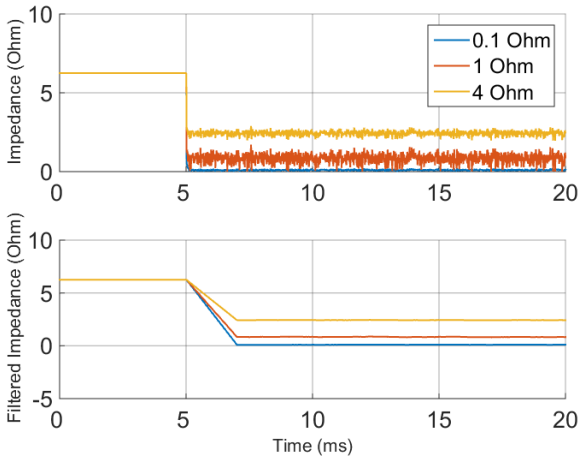


Figure 5.10 Apparent impedance at the terminals of Switch 3 regarding different types of arc faults at the branch of Load 1.

2) Switches at source branch: These include Switch 1 and Switch 2 as shown in Figure 5.1. Take Switch 1 for example, it is responsible for clearing fault that occurs at the branch of G1. The voltage and current at the terminals of Switch 1 regarding arc fault at different locations of the system is shown in Figure 5.11.When fault occurs at the branch of G1, the direction of current flow through Switch 1 will reverse, which induce negative apparent impedance as shown in Figure 5.12. However when fault occurs beyond the branch of G1, apparent impedance seen at Switch 1 will drop to much lower value but remain positive.

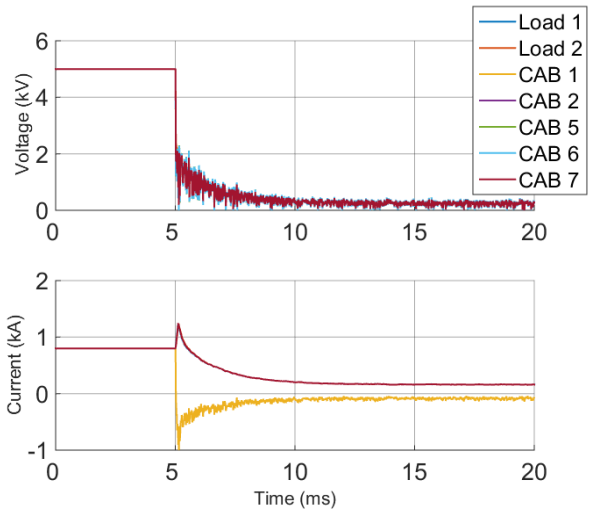


Figure 5.11 Voltage and Current at the terminals of Switch 1 regarding arc fault at different locations of the system

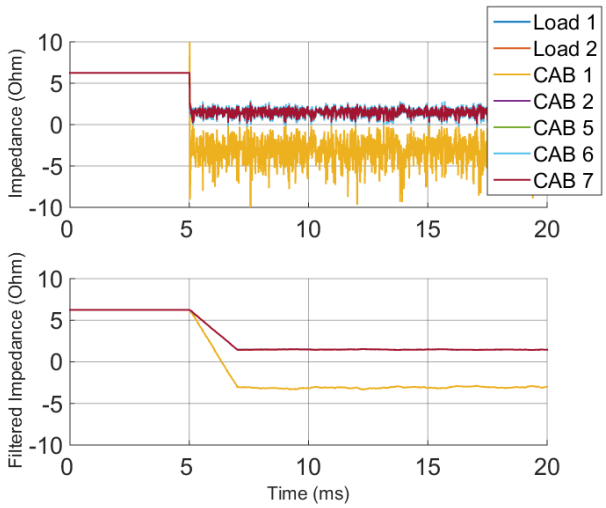


Figure 5.12 Apparent impedance at the terminals of Switch 1 regarding arc fault at different locations of the system (arc impedance 1 Ω)

Figure 5.13 and Figure 5.14 show the apparent impedance at Switch 1 for different types of arc faults (average impedance level at 0.1 Ω and 4 Ω respectively). For an in-zone arc fault with lower average impedance (0.1 Ω), the apparent impedance at Switch 1 goes to negative value as shown in Figure 5.13, whereas for an in-zone arc fault with high average impedance (4 Ω), the apparent impedance at Switch 1 jumps to much higher value as shown in Figure 5.14.

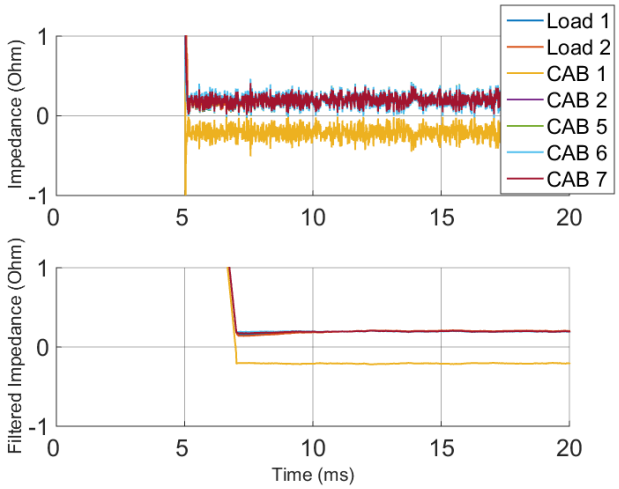


Figure 5.13 Apparent impedance at the terminals of Switch 1 regarding arc fault at different locations of the system (arc impedance 0.1 Ω)

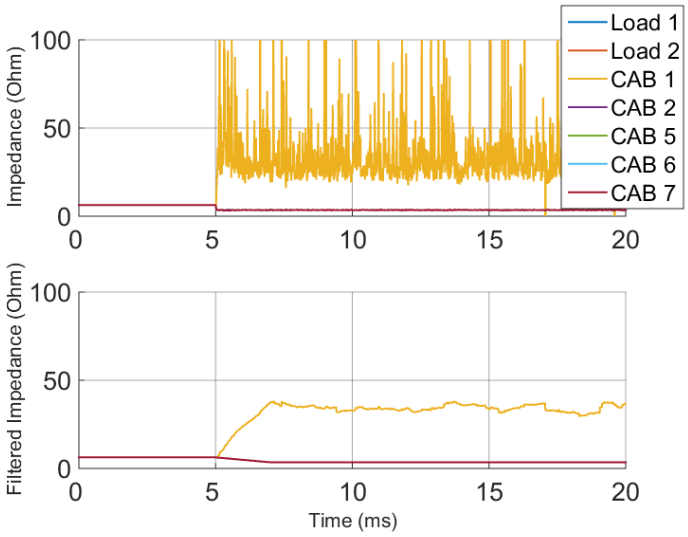


Figure 5.14 Apparent impedance at the terminals of Switch 1 regarding arc fault at different locations of the system (arc impedance 4 Ω)

Figure 5.15 compares the apparent impedance at Switch 1 regarding different faults at the source branch G1, so as two tripping thresholds can be easily defined, one lower tripping threshold right at zero and one upper tripping threshold within the margin (7 Ω to 20 Ω).

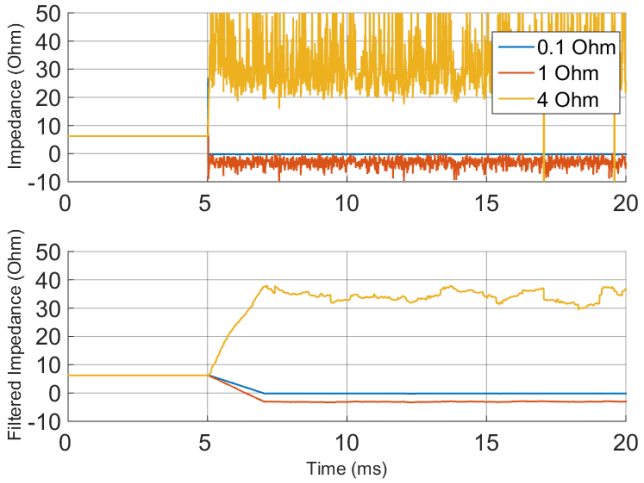


Figure 5.15 Apparent impedance at the terminals of Switch 1 regarding different types of arc faults at the source branch G1.

3) Switches at interconnect bus: These include Switch 5, Switch 6, Switch 7, Switch 8, Switch 9 and Switch 10 as shown in Figure 5.1. Take Switch 7 and Switch 8 for example, they are responsible for clearing fault that occurs at CAB6 of the ring bus. Figure 5.16 shows the voltage and current at the terminals of Switch 7 regarding arc fault at different locations of the system. Due to the symmetrical topology of the system, the current flow through Switch 7 is neglectable when no fault occurs. However when fault occurs in the system, the fault current through Switch 7 and CAB6 will increase sharply, and its direction can either be the same or reversed depending on the fault location.

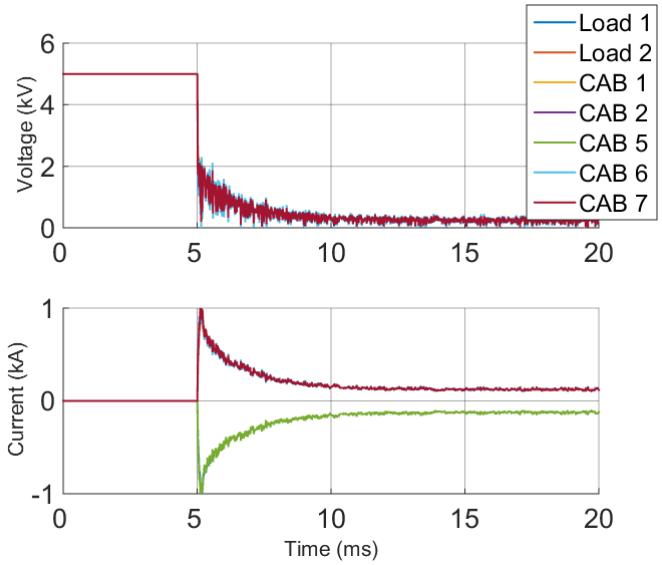


Figure 5.16 Voltage and Current at the terminals of Switch 7 regarding arc fault at different locations of the system

Figure 5.17 shows the apparent impedance at the terminals of Switch 7 regarding arc fault at different locations of the system. The calculated impedance shown in subplot1 as well as the impedance after average filter shown in subplot2 clearly denotes that Switch 7 is capable of differentiating whether the fault is at the left side of Switch 7 (CAB1, Load1,

and CAB5) or at the right side of Switch 7 (CAB2, Load2, CAB6, and CAB7). However a zoom-in of the filtered impedance shown in subplot3 of Figure 5.17 reveals the fact that Switch 7 cannot accurately identify which cable segment the fault is located at because the margin of the apparent impedance for faults at the same side are very small, so as it is almost impossible to coordinate tripping thresholds to enable optimized selectivity.

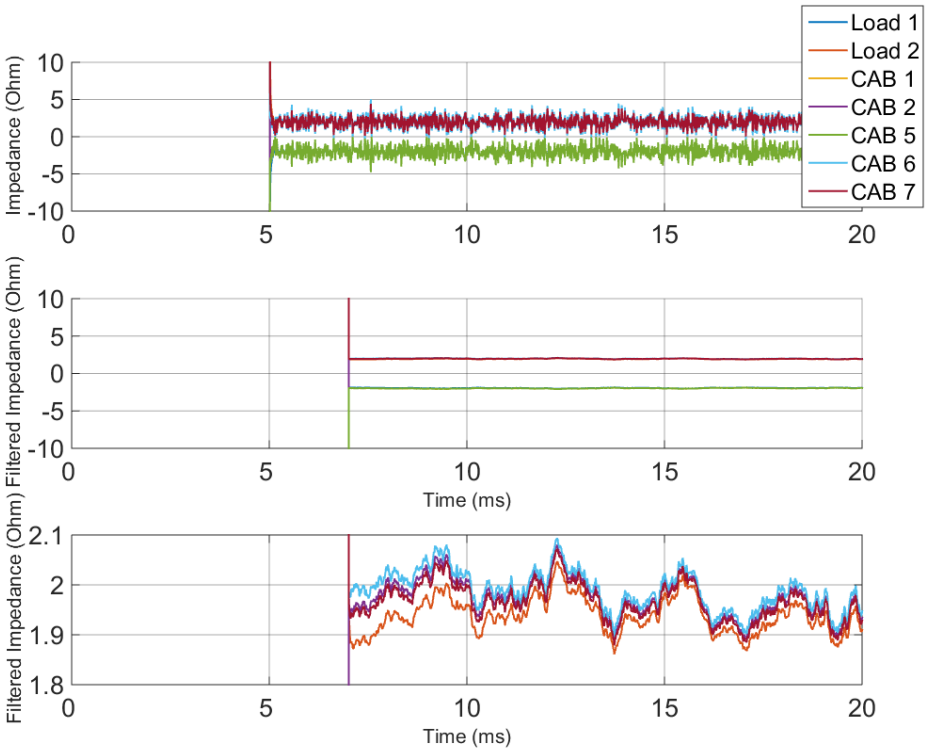


Figure 5.17 Apparent impedance at the terminals of Switch 7 regarding arc fault at different locations of the system (arc impedance 1 Ω)

Figure 5.18 shows the apparent impedance for arc faults at different average impedance levels. The apparent impedance increases from 0.2 Ω to 7.95 Ω as the arc impedance rises from 0.1 Ω to 4 Ω. Therefore, a fixed tripping setting for Switch 7 will not be able to differentiate all these fault scenarios.

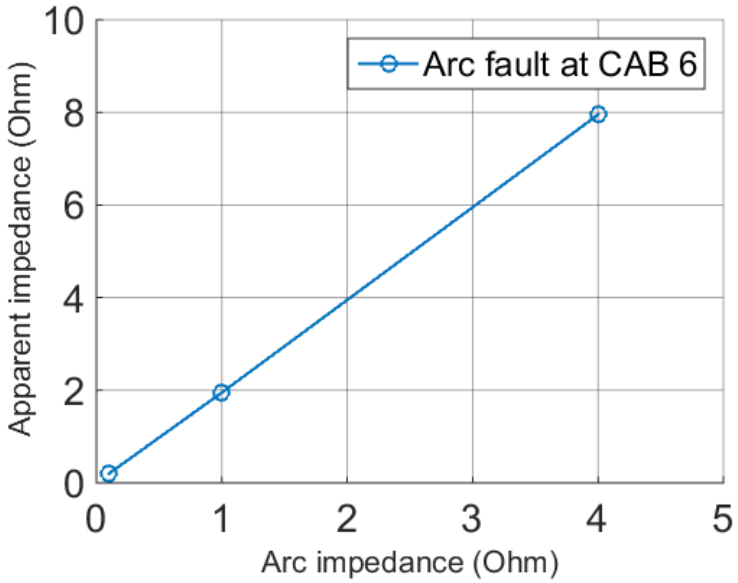


Figure 5.18 Apparent impedance at the terminals of Switch 7 as a function of arc impedance

Table 5.4 summarizes the availability of power to every load after the LIFP method takes fault clearing action. “1” denotes that the load has power and remains operational; “0” denotes that the load lost power. In cases where “0” is the correct state because the fault occurred in the circuit that serves the load, the cell is yellow. In a few cases, “0” is a safe-but-undesirable final state because a load lost power even though a better protective decision should have left it with power. Yellow cell indicates optimal fault isolation, only loads beyond fault were disconnected, red cell indicates effective but non-optimal fault isolation, where an additional load was disconnected. LIFP is found to be capable of clearing fault at various locations. However, due to limited selectivity of LIFP for high impedance fault at the main bus, Zone 1 will be cut off along with Load 1 when fault occurs at Load 1 or CAB 3, wheras Zone 4 will be cut off along with Load 2 when fault occurs at Load 2 or CAB 4. The table shows that there are no cases where a fault was not

disconnected from the system, and only a few cases where loads lost power when they optimally should not have.

Table 5.4 Operational Status Of Loads After Operation Of Fault Protection System For Various Fault Locations

Fault Location \ Load		Main Load 1	Main Load 2	Zone 1	Zone 2	Zone 3	Zone 4
Source Branch	CAB1	1	1	1	1	1	1
	CAB2	1	1	1	1	1	1
Load Branch	LOAD1	0	1	0	1	1	1
	CAB3	0	1	0	1	1	1
	LOAD2	1	0	1	1	1	0
	CAB4	1	0	1	1	1	0
Main Bus	CAB5	0	1	0	1	1	1
	CAB6	1	1	1	1	1	1
	CAB7	1	0	1	1	1	0

Table 5.5 summarizes the effectiveness ratio of LIFP regarding various fault locations. The effectiveness ratio is defined as the total number of loads that remain connected to the system when using the LIFP method, divided by the number that should remain connected by an optimal selection process (only the faulted section is cut off from the system during the fault clearing stage). The total number of loads within the system is normalized to 1. And the weight of Load 1~2 is considered as three times of Zone 1~4, so Load 1~2 are taken as 0.3 wheras Zone 1~4 are taken as 0.1 in this calculation. The effectiveness ratio is found to be 100% for a fault that occurs at a source branch or main bus, and it remains above 85% for faults occuring at the load branch.

Table 5.5 Effectiveness Ratio Of LIFP

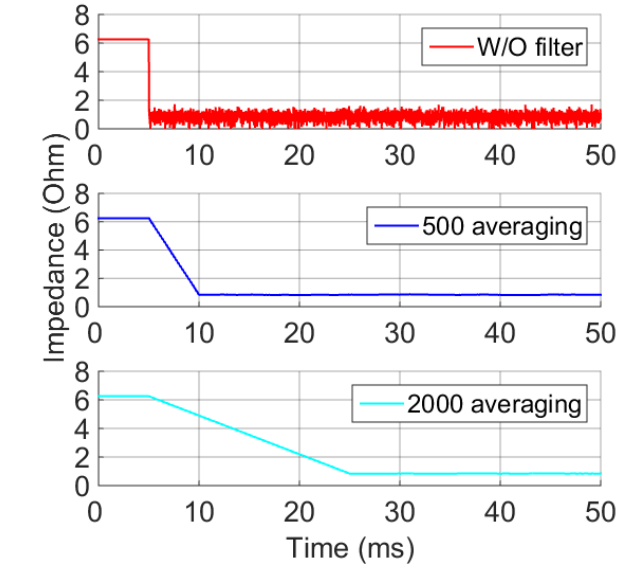
Fault Location		**Loads Remain**		**Effectiveness Ratio**
		Optimal	**LIFP**	
Source Branch	CAB1	1	1	100%
	CAB2	1	1	100%
Load Branch	LOAD1	0.7	0.6	85.7%
	CAB3	0.7	0.6	85.7%
	LOAD2	0.7	0.6	85.7%
	CAB4	0.7	0.6	85.7%
Main Bus	CAB5	0.6	0.6	100%
	CAB6	1	1	100%
	CAB7	0.6	0.6	100%

5.5 APPLICABILITY OF THE LIFP METHOD

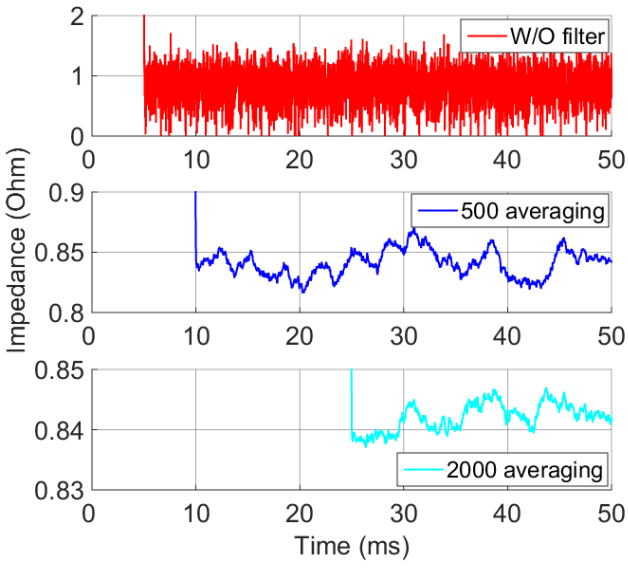
The idea of adopting average filter (low pass filter) for noise reduction has been illustrated in Section III. Tradeoff decisions need to be made between more noise reduction, which helps to generate larger margin for setting tripping threshold, and shorter time delay for making decision. As the time delay of the average filter is determined by the sampling frequency of the local fault controller and the size of the average filter, it is necessary to investigate how these filter configurations can affect the performance of LIFP.

Figure 5.19 compares the apparent impedance at the terminals of Switch 3 regarding different filter configurations. Figure 5.19 (b) is a zoom in of Figure 5.19 (a) in y axis. An arc fault with average impedance of 1 Ω occurs at Load1, so as the apparent impedance without filter shown in subplot1 drops immediately. After adding an averaging filter with

size of 500 counts, the noise level of apparent impedance has been largely reduced as shown in subplot2. Also a 5ms time delay has been introduced with sampling frequency at 100 kHz. A further increase of the filter size to 2000 counts will further bring down the noise level as shown in subplot2, so as will extend the time delay to 20ms.



(a)



(b)

Figure 5.19 Apparent impedance at the terminals of Switch 3 regarding different filter configurations

Figure 5.20 shows the noise level (peak to peak) of the apparent impedance versus filter size. As the filter size increases from 200 counts to 2000 counts, the noise level drops from 0.1 Ω to under 0.01 Ω. Given a higher sampling frequency of 1 MHz, the noise level can be reduced to 0.1 Ω, while a time delay of only 200 μs is required.

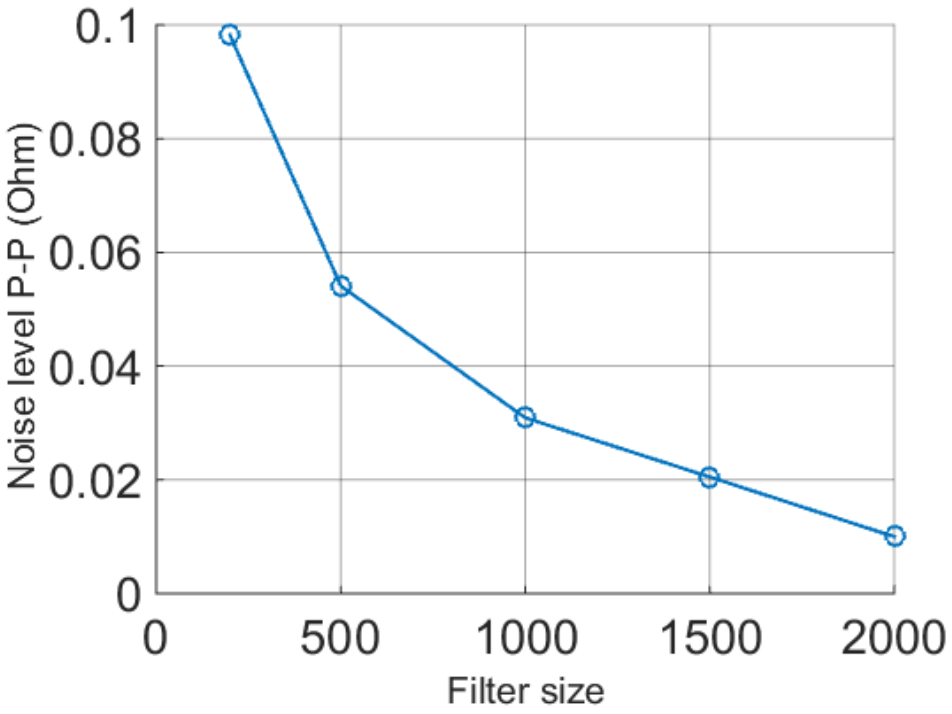


Figure 5.20 Noise level (peak to peak) versus filter size

The performance of LIFP may be affected by system configuration such as the cable impedance. The analysis in Section III has shown the effectiveness of LIFP in handling arc faults at source branches and main bus, versus insufficient selectivity for arc faults at load branches. For example, if fault occurs at CAB 3, both Switch 3 and Switch 6 will open during the fault clearing stage, which not only isolate the load branch but also unnecessarily cut CAB 5 and Zone 1 away from the system. However, these characteristics may vary as the cable impedance can be different in other applications.

As been discussed in Section 1.2, the apparent impedance at Switch terminals needs to be obtained to evaluate the impact of cable impedance to LIFP. Table 5.6 lists the tripping margin of apparent impedance, which calculated through (10)-(17), for Switch 6 regarding different cable impedance. It clearly denotes that the margin increases linearly from 2 mΩ to 2 Ω as the cable impedance increases from 2 mΩ to 2 Ω. However, it can be found that Switch 6 will still be incapable of differentiating fault, for which the average fault impedance can vary from 0.1 Ω to 4 Ω, at CAB 5 from CAB 3 due to the limited tripping margin even as the cable impedance reaches 2 Ω. Besides, the increase of cable impedance will result in higher power dissipation as well as voltage drop along the cable. Take the 2 Ω cable impedance for example, a rated current of 800 A can cause 1.28 MW power disspation and 1600 V voltage drop, which is not applicable to this 5 kV system.

Table 5.6 Tripping Margin Regarding Cable Impedance

			Cable impedance (Ω)			
			0.002	0.02	0.2	2
Apparent impedance (Ω)	Fault location	Load 1	0.8661	0.9021	1.2621	4.8621
		CAB 3	0.8651	0.8923	1.1639	3.8788
		CAB 5	0.8631	0.8726	0.9675	1.9024
Margin (Ω)			0.002	0.0197	0.1964	1.9764

CHAPTER 6

COORDINATION OF TRIPPING THRESHOLDS

6.1 DETERMINING THE TRIPPING THRESHOLDS

The tripping thresholds define the tripping zone and non-tripping zone of each switch, and further determine the operation status of each switch during fault scenarios. Therefore, it is of great importance to optimize the settings of tripping thresholds, otherwise the switches may operate incorrectly under certain circumstances.

The pre-defined tripping thresholds can be calculated through the voltage value at current limiting mode and the heaviest power flow through the switch terminal. However in the MVDC shipboard power system, the output power for each generation unit and the power demand for each zone can vary with different operating conditions. Even the system topology can change during operation. It is time consuming (or even impossible) to reevaluate all the parameters and manually adjust tripping threshold settings for each switch. Therefore, an adaptive automatic approach for adjusting the tripping thresholds is necessary.

A) Normal Operation – Voltage Source Mode

The power converters (MMCs) within the baseline system shown in Figure 5.1 are working at voltage source mode in order to maintain the ring bus voltage at the rated level (5kV) when the system is in normal operating condition.

According to nodal analysis in circuit theory, the voltage potential V at the nodes and the current I injected by sources into the nodes meet with Equation (6.1):

$$V = Y^{-1} \cdot I \tag{6.1}$$

Where Y is the bus admittance matrix with m×m (number of nodes) dimension:

$$Y = \begin{bmatrix} y_1 & -y_{12} & -y_{13} & \cdots & -y_{1m} \\ -y_{21} & y_2 & -y_{23} & \cdots & -y_{2m} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -y_{1m} & -y_{2m} & -y_{3m} & \cdots & y_{mm} \end{bmatrix} \tag{6.2}$$

The controlled voltage sources are expressed in I as:

$$I = [\cdots \; V_r/R_p \; \cdots \; V_r/R_q \; \cdots 0 \; 0 \;] \tag{6.3}$$

Where V_r is the rated voltage at the output of the MMCs during normal operation, p and q are the nodes connected to the MMCs, R_p and R_q are the corresponding output resistance of the MMCs.

The current flow I_n^H through Switch n during this normal operating condition can be expressed as:

$$I_n^H = (V_i - V_j)/R_{CAB_{ij}} \tag{6.4}$$

Where V_i and V_j are the voltage of adjacent nodes calculated via (6.1), and $R_{CAB_{ij}}$ is the cable resistance between the two nodes i and j, which can refer to Table IV.

Thus, the apparent impedance at the terminals of Switch n during this normal operating condition can be derived as:

$$R_n^H = V_n^H/I_n^H \tag{6.5}$$

B) Fault Limiting – Current Source Mode

The power converters (MMCs) will be working at current source mode when short circuit fault happens in the system. In this case, limited current (usually with overshoot limited below 120% of rated current value, and current limiting target at 20% of rated current value) rather than huge (10 times or higher) surge current will be injected into the system during fault, so as the energy dumped into the fault can be largely reduced. The converter outputs are equivalent to controlled current sources.

The bus admittance matrix in (6.2) is adjusted by adding two columns and two rows (the number of added columns and rows is aligned with the number of power sources):

$$Y = \begin{bmatrix} y_1 & -y_{12} & -y_{13} & \cdots & -y_{1m} & \cdots & 0 & 0 \\ -y_{21} & y_2 & -y_{23} & \cdots & -y_{2m} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & y_p & 0 & \cdots & 0 & -1/R_p \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & y_q & \ddots & -1/R_q & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \cdots & 0 & -1 & \cdots & 1 & 0 \\ 0 & 0 & \cdots & -1 & 0 & \cdots & 0 & 1 \end{bmatrix} \quad (6.6)$$

And Equation (6.3) should be adjusted correspondently as:

$$I = [0 \quad 0 \quad \cdots \quad I_{limit\_q} * R_q \quad I_{limit\_p} * R_p] \quad (6.7)$$

Where p and q are the nodes that are connected to the power sources. $I_{limit_q}$and I_{limit_p} are the output target of the MMCs during current limiting mode.

Thus follow the same procedure as (6.4)-(6.5), the apparent impedance at the terminals of Switch n after fault event happens at location x can be derived as:

$$R_n^{F\_x} = V_n^{F\_x}/I_n^{F\_x} \quad (6.8)$$

C) Setting the Tripping Zone

The calculation methods shown in Part A and B play key roles in determining the pre-defined tripping characteristics of the dc switches. Each time the system parameters are updated in local controllers, an algorithm integrated at these local controllers will calculate corresponding tripping thresholds as follows:

For a given Switch n, it is expected to only respond to fault at location x. Due to the possible variation of fault impedance, the apparent resistance at the terminal of Switch n will meet the inequity:

$$R_n^{F\_x}{}_{min} \ll R_n^{F\_x} \ll R_n^{F\_x}{}_{max} \tag{6.9}$$

Based on the information listed in Table III, the algorithm will calculate and search through all possible fault locations to find the highest impedance value below $R_n^{F\_x}{}_{min}$, and the lowest impedance value above $R_n^{F\_x}{}_{max}$, so as fulfill the inequities:

$$R_{n\_}^{F} = \left\{(\alpha \in \mathbb{R}) \cap \left(\alpha < R_n^{F\_x}{}_{min}\right)\right\}_{max} \tag{6.10}$$

$$R_{n+}^{F} = \left\{(\alpha \in \mathbb{R}) \cap \left(\alpha > R_n^{F\_x}{}_{max}\right)\right\}_{min} \tag{6.11}$$

where $\mathbb{R} = \left\{R_n^{F\_1}, R_n^{F\_2}, \cdots, R_n^{F\_m}\right\}$.

The tripping thresholds $R_n th_-$ and $R_n th_+$ for Switch n can then be set as:

$$R_{n\_}^{F} \ll R_n th_- \ll R_n^{F\_x}{}_{min} \tag{6.12}$$

$$R_n^{F\_x}{}_{max} \ll R_n th_+ \ll R_{n+}^{F} \tag{6.13}$$

6.2 EFFECTIVENESS OF AUTO THRESHOLD ADJUSTMENT

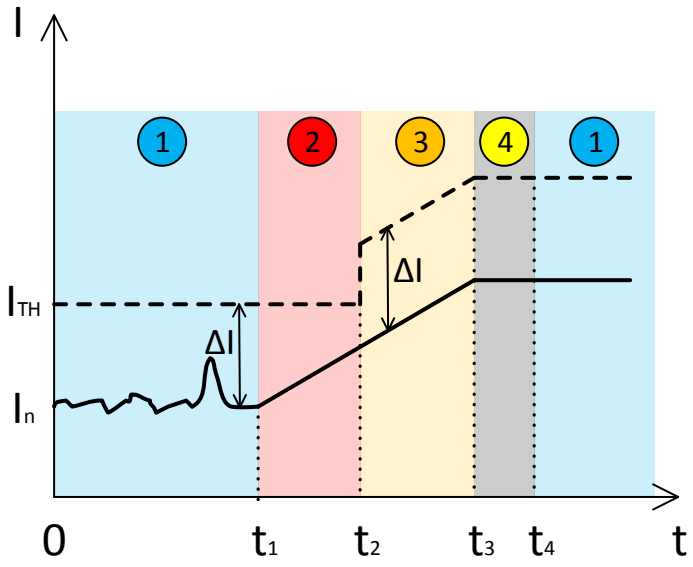
The previous sections clarified the coordination of tripping settings among disconnect switches, and illustrated how to determine the tripping thresholds based on existing knowledge of system parameters via nodal analysis. We have drawn an assumption that the system remains operating with the same configuration until next update at local fault controllers. These updates can only be carried out via wide area communication. They are considered as not desirable to this communication-independent fault protection scheme, so as the interval between each update should be maximized as much as possible, which can be several hours or even days. However for typical operating conditions of the shipboard system, the load demands can vary in a notable way, such as load increasing, decreasing, connecting or disconnecting, during the interval of updates. This results in problems to the fault detection algorithm of the existing method, because load variation can cause current or apparent resistance that observed at converters or switches to change as well, which may trigger mistripping of LIFP as the fixed tripping thresholds set by existing algorithm do not vary correspondently with loads. Therefore in addition to the existing algorithm of LIFP, a local information based algorithm is in need to differentiate whether the system is experiencing a short-circuit fault or just normal load variation.

This goal can be achieved by evaluating the current ramping rate di/dt that measured at the output of converter (or the ramping rate of apparent resistance dR/dt that calculated through voltage and current measurement at the terminals of switch). There are regulation standards for the ramping rate of input current of loads in the shipboard system during normal operating condition: a connected load cannot draw more power from the DC bus than is allowed by the load di/dt rating, which is addressed in IEEE 1709. And this

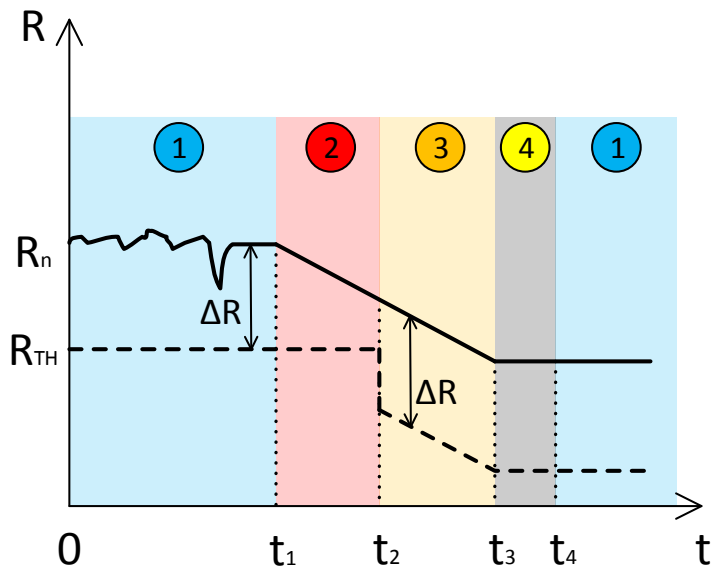
ramping rate is limited to less than $110A/ms$ for the shipboard system shown in Figure 2.1. In contrary, a short-circuit fault can result in much higher di/dt (larger than $1kA/ms$) before the converter switches to current source mode, which has been illustrated in Section III. Hence it is feasible to draw a boundary between $110A/ms$ and $1kA/ms$ for di/dt to tell the fault events apart from the normal operation events.

Besides, this di/dt from raw measurement can vary dramatically due to the presence of noise, which may include switching noise generated from converters, white noise in the system and arc noise from fault, so low-pass filter is a must to reduce the impact of noise and to facilitate the pattern recognition process.

The mechanism of this adaptive algorithm is illustrated in Figure 6.1 (using di/dt and dR/dt as index respectively in (a) and (b)), which shows a typical load increase event. The whole process can be divided into four distinct steps:



(a) Auto adjustment of tripping thresholds at MMCs



(b) Auto adjustment of tripping thresholds at DC Switches

Figure 6.1 Procedures of Auto Adjustment of Tripping Thresholds during a Load Increase Event

1. Normal operation – While the system is operating at normal condition, which means no major load variation or fault, the tripping threshold I_{TH} (R_{TH}) of corresponding converter (switch) will keep its preset value.

2. Load variation detection – When a load increase event starts at t_1, so as I_n (R_n) will increase (decrease) with a ramping ratio that limited by the power converter ($110A/ms$ maximum for this shipboard system application). In order to identify that the system is our of normal operating condition, and to further determine that the system is experiencing load variation rather than short-circuit fault, both the mean value of $I_n(R_n)$ and the derivative $\frac{dI_n}{dt}(\frac{dR_n}{dt})$ are constantly compared with predefined ranges. It should be noticed that I_{TH} (R_{TH}) will remain at its original value throughout

this step until the mean value of I_n (R_n) over a certain period of time (determined by sampling frequency and number of samples) exceeds the predefined range at t_2. However, Figure 6.1 also indicates a shrinking margin ΔI (ΔR) between I_n(R_n) and I_{TH} (R_{TH}) during this step. To avoid mistripping, the initial margin should meet inequalities (6.14) and (6.15):

$$\Delta I > \int_{t_1}^{t_2} \frac{dI_n}{dt} \tag{6.14}$$

$$\Delta R > \int_{t_1}^{t_2} \frac{dR_n}{dt} \tag{6.15}$$

3. Adjustment of tripping thresholds – Begins at t_2, both the mean value of I_n(R_n) and $\frac{dI_n}{dt}$($\frac{dR_n}{dt}$) have met the criterion for confirming that the system is going through a load step event. Then the local fault controller will allow the adjustment of I_{TH} (R_{TH}) along with I_n (R_n) to maintain the original margin ΔI (ΔR). For a load increase event, I_{TH} (R_{TH}) will increase (decrease) gradually as shown in Figure 6.1.

4. End of session detection – The load increase event ends at t_3, whereas the local fault controller should be able to determine the end of session at t_4 and go back to step 1 by evaluating the mean value of I_n(R_n).

Figure 6.2 shows the functional flow chart of this adaptive algorithm. Apparently, whether the system is in normal operation or out of normal operation is determined by the indicator I_n (R_n). Once the system has been identified as out of normal operation, the indicator $\frac{dI_n}{dt}$($\frac{dR_n}{dt}$) can further identify which sub-state the system is running at, so as the local fault controller can response correspondently: For a load step event, the tripping threshold will be automatically adjusted until the system goes back to normal operation

statue; for a short-circuit fault event, the tripping threshold will be maintained until the tripping signal is generated to initiate the fault clearance sequence as been discussed in Section 4.1.

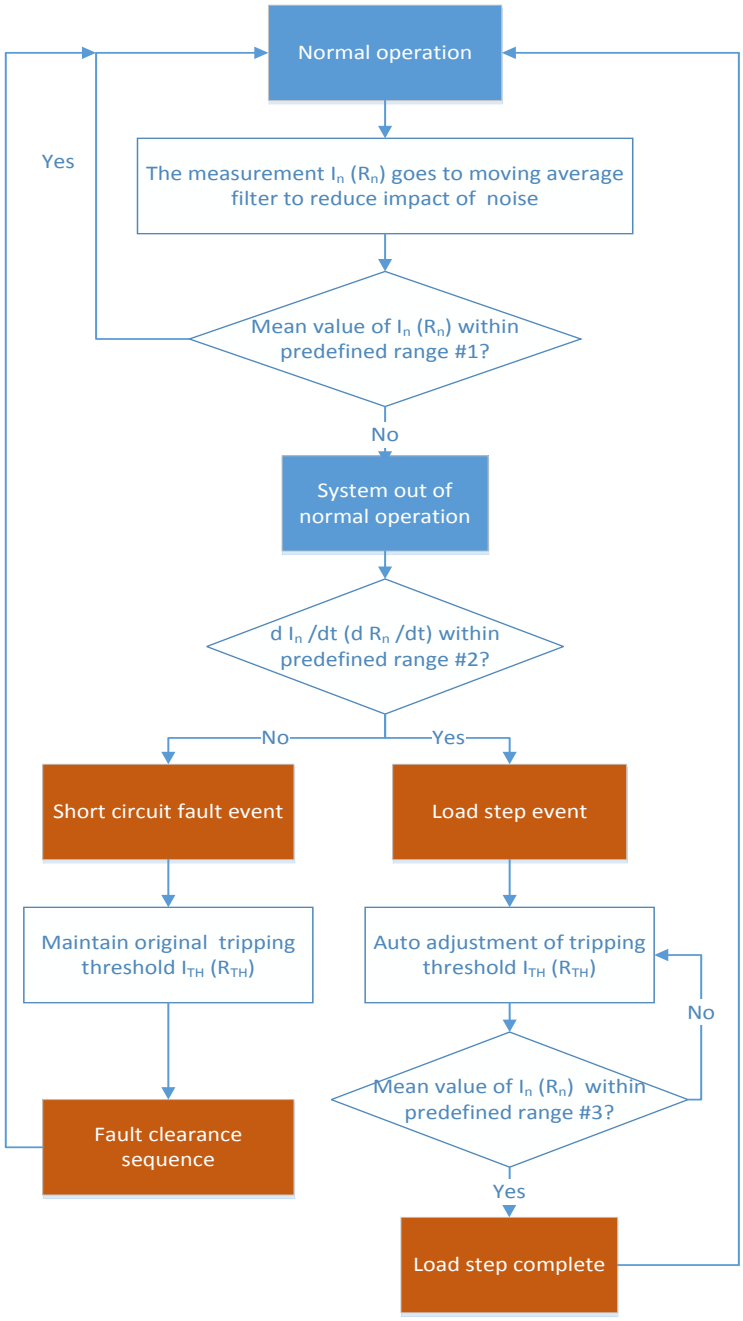
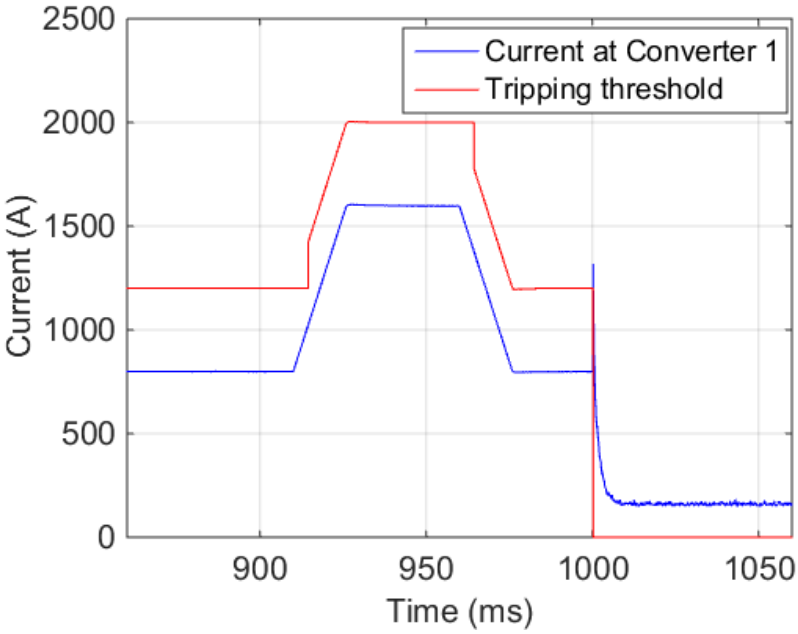


Figure 6.2 Flow chart of the auto adjustment of tripping thresholds

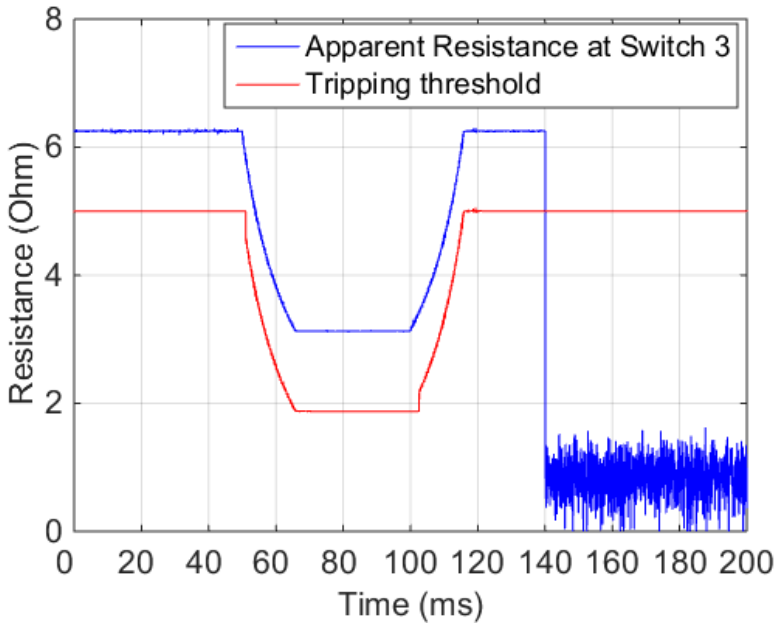
6.3 RESULTS

This algorithm has been validated in simulation through the baseline system shown in Figure 5.1. The whole test scenario has been designed as going through three major transitions: First, both Load 1 and Load 2 double their power from the rated value 4 MW to 8 MW. Second, both Load 1 and Load 2 decrease their power from 8 MW back to the rated value 4 MW. Third, a short-circuit arc fault occurs at Load 1. Figure 6.3 shows the current measurement at Converter 1 and the apparent resistance obtained at Switch 3 along with tripping threshold at corresponding local fault controller during the test scenario. The load step up event initiates at 50 ms as shown in Figure 6.3, and the power of the two loads doubles. However, due to the restriction of $\mathrm{di/dt}$ imposed by IEEE 1709 as discussed in previous context, the input current at Load 1 as well as the output current at Converter 1 starts to increase from 800 A with a ramping rate of 50A/ms. Meanwhile, the current measurement is processed via a 100-sample moving average filter at a rate of 20 kHz, which introduces a time delay of 2.5 ms. The boundary for identifying if the system is out of normal operation is set at 900 A. Considering a ramping rate of 50A/ms, it takes 2 ms for the converter current to reach at this critical level, so the total amount of time that required for load variation detection shown as $(t_2 - t_1)$ in Figure 6.1 is 4.5 ms.

Apparently, the length of this pre-adjustment time delay $(t_2 - t_1)$ is affected by the trigger level of detection that shown as predefined range #1 in Figure 6.2, the ramping rate of current (resistance), the sampling frequency and number of samples of the moving average filter. Trade off decisions need to be made among these factors, so that this time delay can be sufficient for identifying system status as well as not causing fault protection to mistrigger.



(a) Adjustment of tripping threshold at Converter 1



(b) Adjustment of tripping threshold at Switch 3

Figure 6.3 Adjustment of tripping threshold in response to different operating conditions of the system: load increase, load decrease, and short-circuit arc fault.

Table 6.1 compares the time delay under various conditions. It can be observed that less sample numbers as well as higher sampling frequency will result in less time delay. There is always hardware limit imposed by measurement sensors and local fault controller for the sampling frequency, whereas no such restriction for the number of samples that the moving average filter can take for computing during each step. However, less number of samples for the moving average filter will attenuate the noise reduction. Hence in order to avoid mistripping of fault protection, larger tripping margin ΔI will be required, which can adversely affect the coordination of tripping settings.

Table 6.1 Time Delay For Load Variation Detection Under Various Configurations

ΔI (A)	**Trigger Level of Detection (A)**	**Sample #**	**Sampling Frequency (kHz)**	**Time Delay (ms)**	**Mistrigger**
400	± 100	100	20	4.5	No
		50	20	3.25	No
		100	40	3.25	No
		50	40	2.625	No
400	± 200	100	20	6.5	No
	± 300	100	20	8.5	Yes
	± 300	50	20	7.25	No
	± 300	100	40	7.25	No
200	± 100	100	20	4	Yes
	± 50	100	20	3.2	No
	± 100	50	20	2.25	No
	± 100	100	40	2.25	No

It can also be observed from Figure 6.3 (a) that the tripping threshold rapidly goes into and stays at a steady value 2 kA, once the load increase ends and the output current at Converter 1 stops increasing. This denotes that the proposed algorithm successfully detects the completion of the load increase event. The following sequence, for which the power of the loads drops back to the rated value, starts at 100 ms, so as the tripping threshold at Converter 1 is adjusted automatically back to 1.2 kA, while the tripping margin ΔI is still kept at 400 A. This algorithm is also tested under the fault scenario which begins at 140 ms as shown in Figure 6.3. The fault occurrence has been successfully identified and differentiated from load variations by the proposed algorithm.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

We present a generic and effective protection method LIFP for protection of dc microgrids against short circuit arc faults. The main contributions of this work include:

The characteristics of dc arc were investigated regarding a wide variety in fault conditions including arc current from 100 A to 400 A and arc length from 88.9 mm to 203.2 mm, so as a generic dc arc model was developed based on minor-conductor-triggered arc test results to facilitate system level simulation study. The time average value of arc resistance is represented via the Paukert equations as a function of current, parameterized by arc length, with the coefficients fitted to experimental data from dc converter-fed arcs. Due to the highly randomness of arc resistance in time even when the arc is relatively stable, the distribution pattern of arc resistance in time was studied and found to be aligned with normal distribution. Apparently the expectation of arc resistance μ falls into the range from 0.1 Ω to 4 Ω, while the standard deviation σ, which indicates the noise level of the arc resistance, is within the range from 0.15 to 0.19.

LIFP was validated to be perfectly integrated and compatible with CFP. Both of these methods serve for the robust management of short-circuit faults in MVDC systems, and rely on coordinated control of power converters and non-fault-breaking mechanical disconnect switches to effect the fault clearance process— fault detection and localization,

complete de-energizing of the system, isolation of faulted branch and re-energizing of the system. CFP depends on communication between distributed sensors and a central decision-making authority to achieve fastest primary protection. It is backed up by a local response function LIFP that takes over in case of failure in the primary method. Both of these methods were evaluated in a shipboard power system that was first modeled and simulated within a MATLAB-Simulink environment. The results show good performance and compatibility of LIFP and CFP in fault detection and location. CFP is able to locate the fault within 5ms, and LIFP is able to locate the fault within 10ms.

The response of LIFP to arc faults was investigated regarding different fault locations via simulation. The characteristic of apparent resistance at switch terminals were evaluated to coordinate the operation of switches. There are no cases where a fault was not disconnected from the system and only a few cases where loads lost power when they optimally should not have. The effectiveness ratio of LIFP was found at 100% for fault occurs at the source branch or main bus, and it still stays above 85% for fault occurs at the load branch. The impact of system configurations including filter configurations and cable impedance to LIFP was analyzed. For an average filter (low pass filter) with sampling frequency at 100 kHz, the noise level of apparent resistance drops from 0.1 Ω to under 0.01 Ω as the filter size increases from 200 counts to 2000 counts. Given a higher sampling frequency of 1 MHz, the noise level can be reduced to 0.1 Ω, while a time delay of only 200 μs is required. Also, simulation results reveal that the tripping margin of a switch increases linearly from 2 mΩ to 2 Ω as the cable impedance increases from 2 mΩ to 2 Ω.

Most importantly, the coverage of LIFP was greatly extended to arc faults under varying load conditions. This is achieved via a novel algorithm which allows LIFP to automatically determine and adjust the tripping thresholds for each switch. The current ramping rate (di/dt) is used for differentiating load variations ($di/dt < k_{limit}$) from faults ($di/dt > k_{limit}$). The mechanism of auto adjustment of tripping thresholds via LIFP can be described as four stages: normal operation, load variation detection, adjustment of tripping thresholds and end of session detection. The goal of adjustment of tripping thresholds is to maintain the original tripping margin ΔR between the measured apparent resistance R_n and the tripping threshold R_{TH} at the converter, when the system shifts toward another balance point. This algorithm has been evaluated through load variation events with a ramping rate up to 50A/ms followed by short circuit arc fault event. Simulation results show LIFP can successfully identify the load ramping incidents and initiate adjustment of tripping thresholds within 4.5ms, whereas generate tripping signals for the fault event within 1ms.

7.2 FUTURE WORK

The arc model derived in this work is based on arc experiment under limited test conditions. Future work may take into account more arc test data to improve this model, and to extend the applicable range of this model.

In this work, LIFP has been verified analytically and in simulation. Future work may involve validation of LIFP in real-time test bed/hardware environment. Also, future work may consider to study the performance of LIFP in a more complex larger scale MVDC system.

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