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Growth and transport properties of complementary germanium nanowire field-effect transistors

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n- and *p*-type Ge nanowires were synthesized by a multistep process in which axial elongation, via vapor–liquid–solid (VLS) growth, and doping were accomplished in separate chemical vapor deposition steps. Intrinsic, single-crystal, Ge nanowires prepared by Au nanocluster-mediated VLS growth were surface-doped *in situ* using diborane or phosphine, and then radial growth of an epitaxial Ge shell was used to cap the dopant layer. Field-effect transistors prepared from these Ge nanowires exhibited on currents and transconductances up to 850 $\mu\text{A}/\mu\text{m}$ and 4.9 $\mu\text{A}/\text{V}$, respectively, with device yields of >85%. © 2004 American Institute of Physics.

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One-dimensional nanostructures, such as semiconductor nanowires and single-walled carbon nanotubes are promising building blocks for nanoscale device applications ranging from biological sensors to nanoelectronics.^{1–5} The ability to control rationally and predictably the properties of these building blocks will be essential for improving the properties of individual devices and moving toward integrated nanosystems. In particular, the availability of both *n*- and *p*-type semiconductor components would enable the assembly of complementary logic devices, which can exhibit faster switching speeds and lower power consumption than unipolar devices. Complementary devices based on carbon nanotubes have been demonstrated by several groups,^{4,5} although the simultaneous production of metallic and semiconducting nanotubes during growth,⁵ as well as the fact that *n*-type doping is typically accomplished following device assembly and is not always permanent,⁵ could limit applications.

Semiconductor nanowires offer the ability to control composition and doping at the time of synthesis by applying the knowledge gained from research on planar semiconductor systems.¹ Complementary doping has been demonstrated in several nanowire materials such as silicon (Si) and gallium nitride (GaN),^{1,2,6} and has been used to assemble inverters, bipolar transistors, and light-emitting diodes.^{2,6} However, achieving good electronic properties for both *p*- and *n*-channel field-effect transistors (FETs) (*p*-FETs and *n*-FETs) in the same material has proved challenging. As transistor switching speeds and on currents are ultimately limited by carrier mobilities, it is desirable to fabricate complementary nanowire devices using semiconductors with high carrier mobilities. Germanium has higher electron and hole mobilities than Si⁷ and, therefore, offers potential performance gains compared to Si-based planar and nanowire devices.

Here, we describe the synthesis of *p*- and *n*-type Ge nanowires and the fabrication of Ge nanowire *p*- and *n*-FETs. Previously, Ge nanowires have been synthesized by the vapor–liquid–solid (VLS) approach in which vapor

phase Ge is provided by laser ablation,⁸ physical vapor transport,^{9,10} or by a molecular precursor in a chemical vapor deposition (CVD) process.^{11,12} The CVD approach coupled with VLS is especially attractive since it enables the precise control of reactants and dopants needed to achieve high-quality electronic materials and, furthermore, can be extended to produce more complex nanowires, such as core-shell structures via homogenous radial growth.¹¹

Our overall approach to the controlled growth and doping of complementary Ge nanowires is outlined in Fig. 1. Intrinsic nanowire growth from 10 nm Au nanoclusters^{11,13} was initiated at 320 °C and 500 Torr using 1.5% germane (GeH₄) in an atmosphere of hydrogen (H₂). After this nucleation step, elongation of the single-crystal nanowire structure was carried out at a reduced temperature of 285 °C to minimize nonspecific decomposition of germane on the nanowire surface.¹⁴ The nanowire surfaces were then doped at 380 °C with either phosphine (PH₃) or diborane (B₂H₆) (both 100 ppm in H₂) at 5 Torr in the absence of germane. The doping conditions were chosen to produce a self-limited layer of activated dopant atoms¹⁵ as estimated from atomic-layer-doping studies on planar SiGe.^{16–18} The 10 nm δ -doped cores were then coated with a \sim 5 nm thick *i*-Ge shell.¹¹

Transmission electron microscopy (TEM) was used to characterize the core diameter, shell thickness, and crystallinity of Ge nanowires grown by our core-shell method.¹⁹

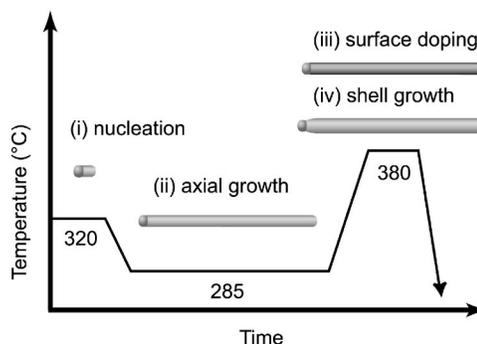


FIG. 1. Schematic illustrating the approach used to synthesize *n*- and *p*-type Ge nanowires.

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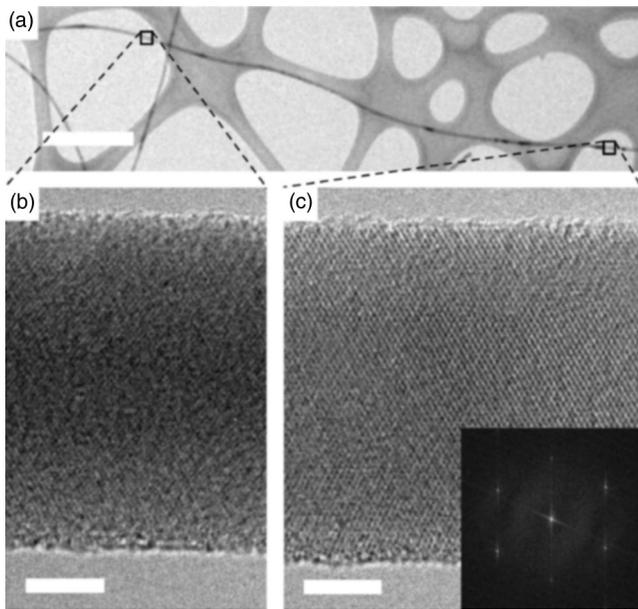


FIG. 2. TEM characterization of a Ge nanowire prepared using the approach outlined in Fig. 1. (a) Ge nanowire on lacey carbon support film. Scale bar is 0.5 μm . (b) and (c) High-resolution TEM images recorded from the two indicated regions of the nanowire in (a); the images are separated by 3 μm . Scale bars are 5 nm. [Inset of (c)] two-dimensional Fourier transform of the data in (c) showing the [111] zone axis and a {110} growth direction. The six inner peaks are forbidden 1/3 {422} reflections that arise due to the finite thickness of the nanowire (see Ref. 24).

Figure 2 shows a representative Ge nanowire with a diameter of 22 nm. In agreement with previous studies of VLS-grown nanowires,¹³ the diameter of Ge nanowires grown without shells correlated well with the diameter of the Au nanoclusters: Among 50 wires grown from 10 nm nanoclusters, the diameter was 10 ± 3 nm. The same nanocluster size, nucle-

ation step, and axial growth step, followed by the doping and shell growth steps described above, were used to produce the nanowire shown in Fig. 2. Among 50 wires in this sample, the diameter was 20 ± 4 nm, confirming that a shell of thickness ~ 5 nm was grown. The TEM data also demonstrate that the diameter is uniform along the length of the wire [Figs. 2(b) and 2(c)], and thus that radial shell growth occurred after, but not during, axial core growth, as concomitant axial and radial growth lead to tapering. High-resolution TEM images shown in Figs. 2(b) and 2(c) further show that the capping shell is epitaxial along the entire length of the nanowire.

Systematic electrical transport measurements were carried out to evaluate the performance of FETs fabricated from our doped Ge nanowires. The FETs consisted of individual Ge nanowires with Ti source and drain contacts (typical separation 1.5 μm), and were gated via the degenerately doped Si substrate through a 60 nm thick zirconium oxide (ZrO_2) dielectric layer. Figure 3(a) shows the current (I_D) versus drain-source bias voltage (V_D) (output characteristics) for a boron-doped Ge nanowire at different values of the gate voltage (V_G). The curves are characteristic of a *p*-channel metal-oxide-semiconductor (MOS) FET.⁷ The linear relationship of I_D and V_D at low bias indicates good ohmic contact to the nanowire with a contact resistance of < 200 k Ω , which was typical for the devices studied. Only slight curvature corresponding to saturation effects is observed for $|V_D| < 2$ V. A plot of I_D versus V_G (transfer characteristic) with V_D fixed at 1 V shows the on/off ratio of 10^5 and subthreshold slope of 240 mV/dec [Fig. 3(b)]. The transconductance at $V_D = 1$ V was 3.3 $\mu\text{A}/\text{V}$, corresponding to an estimated field-effect mobility of ~ 115 cm^2/Vs .²⁰ The on current at 1 V drain and -2 V gate overdrive was 4.8 μA . For comparison with planar devices, this is equivalent to an

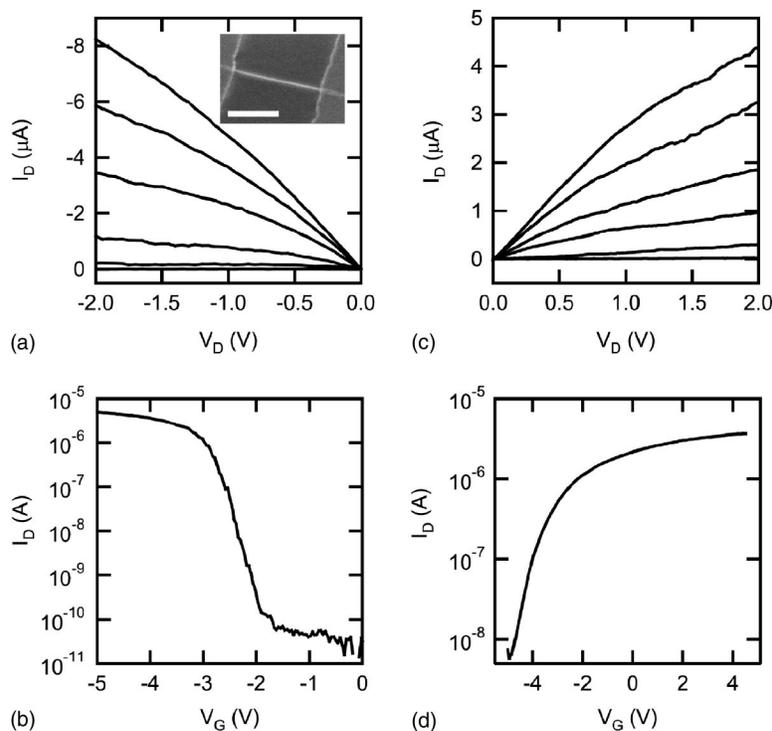


FIG. 3. Germanium nanowire *p*- and *n*-FETs. (a) Output characteristics of *p*-FET. The gate voltage V_G was stepped in 0.5 V increments from -5 to -2.5 V. Inset: Scanning electron microscopy image of a typical device. Scale bar is 1 μm . (b) Transfer characteristic of *p*-FET at 1 V drain. (c) Output characteristics of *n*-FET. The gate voltages V_G were, starting from the top, +5 V, +2.5 V, 0 V, -0.5 V, -1.5 V, and -5 V. (d) Transfer characteristic of *n*-FET at 1 V drain.

on current of $360 \mu\text{A}/\mu\text{m}$ for a $1 \mu\text{m}$ gate length. Among 30 *p*-FETs measured on two separately fabricated samples, the total yield was 86%. The average (maximum) on current was $250 \mu\text{A}/\mu\text{m}$ ($850 \mu\text{A}/\mu\text{m}$), and the average (maximum) transconductance was $2.8 \mu\text{A}/\text{V}$ ($4.9 \mu\text{A}/\text{V}$) corresponding to a field-effect mobility of $\sim 100 \text{ cm}^2/\text{V s}$ ($170 \text{ cm}^2/\text{V s}$).

Output and transfer characteristics for a phosphorus-doped Ge nanowire FET are shown in Figs. 3(c) and 3(d). The Ti contacts are ohmic with low contact resistance, as in the case of the *p*-FET. The gate response is characteristic of an *n*-channel MOSFET.⁷ The on current for the *n*-FET was $200 \mu\text{A}/\mu\text{m}$ at 1 V drain and 4 V gate overdrive, the subthreshold slope was 675 mV/dec, and the on/off ratio was 10^3 . The relatively higher off current observed in the *n*-FETs versus the *p*-FETs could be caused by acceptor impurities in the intrinsic Ge core or by acceptors at the (unpassivated) nanowire surface. The transconductance of $0.6 \mu\text{A}/\text{V}$ at 1 V drain corresponds to a field-effect mobility of $\sim 20 \text{ cm}^2/\text{V s}$. Forty-five *n*-FETs on three separately fabricated samples had a yield of 88%. The average (maximum) on current was $125 \mu\text{A}/\mu\text{m}$ ($200 \mu\text{A}/\mu\text{m}$), and the average (maximum) transconductance was $0.6 \mu\text{A}/\text{V}$ ($1.0 \mu\text{A}/\text{V}$) corresponding to a field-effect mobility of $\sim 20 \text{ cm}^2/\text{V s}$ ($35 \text{ cm}^2/\text{V s}$).

The on currents and transconductances of our complementary Ge nanowire FETs exceed those of previously reported Si (Ref. 20) and GaN (Refs. 6 and 21) nanowire transistors, and are similar to those recently published for *p*-type Ge nanowire FETs by Wang *et al.*¹² The on currents also compare favorably to that of a recently reported planar Ge *p*-MOSFET which had an on current of $100 \mu\text{A}/\mu\text{m}$ at 2 V drain and -1 V gate overdrive for a $2 \mu\text{m}$ gate length.²² The calculated mobility of the planar FET, $313 \text{ cm}^2/\text{V s}$, was larger than we found for our system, although this is not surprising given that the surfaces of the Ge nanowire FETs were unpassivated. Higher mobilities and smaller subthreshold slopes should be obtainable for future Ge nanowire FETs by deposition of a Ge oxynitride²³ or SiGe capping layer that could limit charge traps at the nanowire surface. Our bottom-up approach to device fabrication will allow such passivation to be carried out *in situ* following Ge nanowire synthesis, and this should lead to improved characteristics for both *n*- and *p*-type Ge nanowire FETs.

In conclusion, our multistep low-temperature nanocluster-mediated VLS nanowire growth and doping method represents a straightforward and flexible way to produce *n*- and *p*-Ge nanowires for nanoscale device applications. Complementary FETs made from these nanowires show high transconductances and excellent ohmic contacts. Further improvements in Ge nanowire FET performance are

expected from optimization of the doping procedure and attention to surface passivation. Self-limiting surface doping of nanowires also offers the potential advantage of controlling dopant fluctuations that become critical at the nanoscale. The efficacy of this method in Ge suggests that it should be considered as a general and rational approach to the controlled doping of other nanowire materials in the future.

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