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Simulation of gate lag and current collapse in gallium nitride field-effect transistors

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Results of two-dimensional numerical simulations of gate lag and current collapse in GaN heterostructure field-effect transistors are presented. Simulation results clearly show that current collapse takes place only if an enhanced trapping occurs under the gate edges. Hot electrons play an instrumental role in the collapse mechanism. The simulation results also link the current collapse with electrons spreading into the buffer layer and confirm that a better electron localization (as in a double heterostructure field-effect transistor) can dramatically reduce current collapse. © 2004 American Institute of Physics. [DOI: 10.1063/1.1823018]

Gate lag and current collapse effects observed in most GaN-based transistors represent an important roadblock for applications of these devices. The elimination of current collapse and gate lag requires understanding of physical phenomena responsible for these nonideal effects. Several contradictory mechanisms have been proposed, ranging from the “virtual gate model”¹ to an explanation linking current collapse and gate lag to trapping at the gate edges.² The latter mechanism has been confirmed by gated transmission line measurements on GaN metal-semiconductor field-effect transistors (MESFETs), metal-oxide-semiconductor field-effect transistors,³ heterostructure field-effect transistors (HFETs), and metal-oxide-semiconductor heterostructure field-effect transistors (MOSHFETs).⁴ Figure 1 plots experimentally measured channel resistances of HFETs as a function of the gate length. $R(0)$ is the resistance measured immediately after the gate bias goes from below the threshold up to zero; $R(\tau)$ is measured after the transient process is over and the channel current reaches the steady-state value. The measurements were done both for the linear and saturation regimes. Qualitatively same dependencies have been obtained for HFETs, MOSHFETs and MESFETs. As seen from Fig. 1, in all these cases the transient channel resistance change is essentially independent of the channel length. Therefore, the gate voltage stress did not change the channel sheet resistance under the gate but rather led to a dramatic increase in the drain and source access resistances.

Motivated by these experimental results and previously proposed qualitative models, we now present the results of numerical simulations that clearly show that trapping at the gate edges could explain the observed features of the current collapse.

To investigate the role of edge traps in current collapse, two-dimensional simulations of AlGaN/(In)GaN HFETs

were carried out using the multidimensional device simulator DESSIS, from Integrated Systems Engineering.⁵ The simulated device structure includes a 2 μm GaN layer, capped by a 4 nm $\text{In}_x\text{Ga}_{1-x}\text{N}$ channel and a 25 nm $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier. The In content in the channel was varied from $x=0$ up to $x=0.05$ in our simulations. We employed 1.5 and 2.4 μm for source/gate and gate/drain separations, respectively, and a gate length of 1.1 μm .

Since hot electrons play an important role in the vertical real space charge transfer and subsequent capture in bulk traps,⁶ they were accounted for by the hydrodynamic transport model available in DESSIS. For comparison, simulations using drift-diffusion transport equations, which do not account for hot electrons, were also performed.

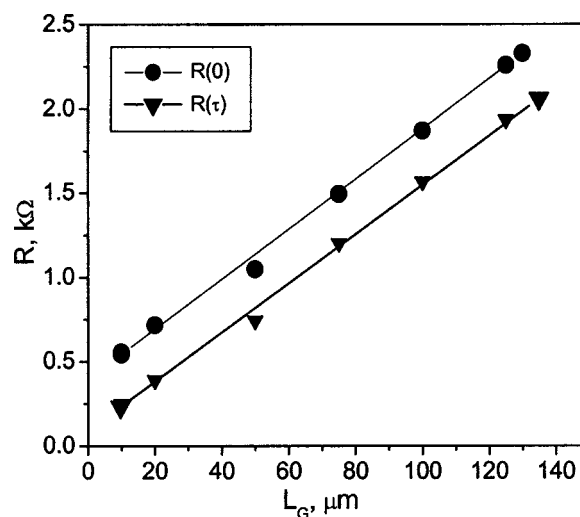


FIG. 1. HFET channel resistance as a function of gate length. $R(0)$ —immediately after the gate bias goes from below the threshold up to zero; $R(\tau)$ —after the transient process is over and the channel current reaches the steady-state value.

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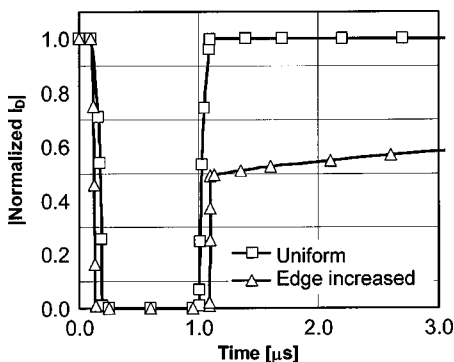


FIG. 2. Normalized drain current as a function of time for uniform trap distributions (squares) and with increased edge trap concentration (triangles).

Pyroelectric and piezoelectric contributions to polarization fields, typical of nitride based semiconductors, were accounted for via a fixed AlGaIn/(In)GaIn interface sheet charge, $N_p = 1.15 \times 10^{13} \text{ cm}^{-2}$. An extended discussion on the choice of the interface charge value, as well as on other model parameters used in our simulations, can be found elsewhere.⁶ To take into consideration stress and field induced traps, we increased the trap density around both gate edges, overlaying that to a uniform distribution of background traps. We chose a Gaussian profile for spatial distribution of traps under the gate edges [see Fig. 3(b)]. We adopted a single level acceptor trap in all our simulations, positioned 1 eV above mid band gap.

Initial simulations were run for three device models, all of them simple HFETs with no In added to the channel region. The first one contained a uniform distribution of traps throughout the entire device, with a density of $8.4 \times 10^{17} \text{ cm}^{-3}$. In the second model we used a uniform background distribution with density $5.0 \times 10^{17} \text{ cm}^{-3}$ superimposed by two lateral Gaussian profiles, as described above, such that the resulting peak concentration under the gate edges was $3.5 \times 10^{18} \text{ cm}^{-3}$. These two trap distributions are such that their integrated value under the channel is the same, leading to an identical steady-state drain current, $I_{D0} = 22.6 \text{ mA/mm}$ at $V_D = 0.1 \text{ V}$ and $V_G = 0 \text{ V}$. A third device was also simulated with uniform trap distribution, but with a concentration corresponding to the peak value of the Gauss-

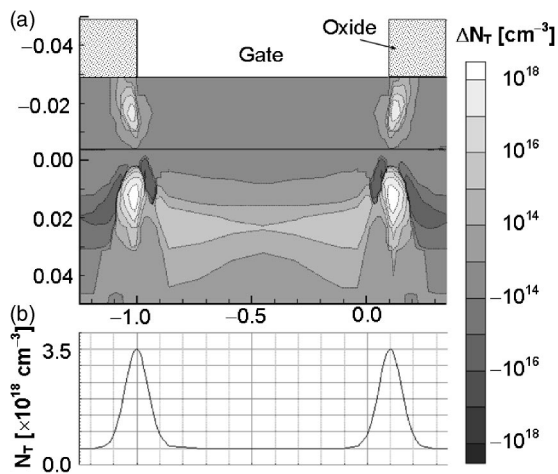


FIG. 3. (a) Net trap occupation with respect to the steady state, right after negative bias is applied to gate, and (b) spatial distribution of trapped electrons along a horizontal cut in the channel.

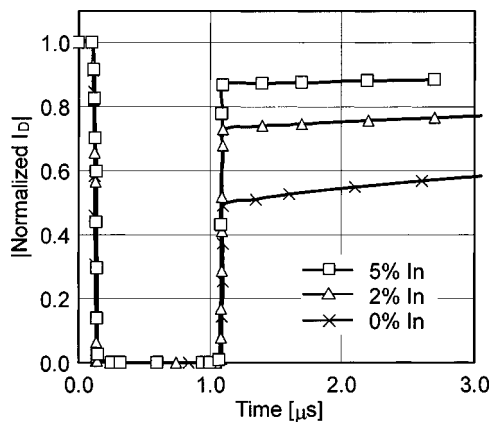


FIG. 4. Drain current as a function of time for different In mole fractions.

ian, i.e., $3.5 \times 10^{18} \text{ cm}^{-3}$ and an increased AlGaIn/(In)GaIn interface charge, $N_p = 1.89 \times 10^{13} \text{ cm}^{-2}$, such that I_{D0} remains unchanged. The drain voltage was set to 0.1 V for all simulations, followed by a 1 μs gate pulse from 0 to -5 V , with fall and rise times of 150 ns, and then left at 0 V for the rest of the simulation.

Figure 2 shows results from simulations with hydrodynamic transport equations in a plot of the normalized drain current versus time, where the normalization factor is the drain current at the start of the transient simulation, i.e., I_{D0} , identical for all three simulations. Notice that while a collapse of about 50% is observed for the simulation with gate-edge traps (triangle markers) virtually no collapse is observed for the simulations with uniform trap concentrations (squares), virtually identical for both uniform trap distribution cases. Although the applied drain voltage is low, the gate pulse provides enough energy to heat up electrons during the transient, and hot electrons may play an important role in current collapse. Results from simulations carried out with drift-diffusion transport equations for all device structures revealed no collapse, emphasizing the instrumental role of hot electrons in the collapse mechanism.

Figure 3 shows the simulated trapped electron distribution difference compared to the steady-state occupation. The snapshot was taken from the device with gate-edge traps immediately before the gate pulse was returned to 0 V. The analysis of the snapshot in Fig. 3, along with other similar snapshots taken during the negative bias pulse, shows that there is a trade-off, with electrons de-trapping in the entire region under the gate and channel electrons being temporarily trapped in the bulk, primarily under the gate edges. When the gate is negatively biased, equilibrium conditions determine the de-trapping process. On the other hand, excess channel electrons will spill over in all directions while the gate bias is ramped down and acquire enough energy at the gate edges to reach far deep into the substrate where a number of traps were initially unoccupied. By monitoring the simulated trap occupation under the gate during the applied pulse to the device with gate-edge traps, we noticed that the average occupation increases while ramping down the gate bias and then remains approximately constant while $V_G = -5 \text{ V}$. On the other hand, the average trap occupation does not increase, but rather even slightly decreases as governed by equilibrium trap dynamics, during the negative gate pulse in the devices with uniform doping.

Since simulation results for the current collapse are consistent with trapping of electrons that are hot enough to reach deep portions of the substrate where a number of initially unoccupied traps were available, the existence of an energy barrier should minimize the effect by reducing electron spill over into the substrate. Also, there is experimental evidence that the incorporation of indium in the channel, forming a double heterostructure FET (DHFET), leads to significantly smaller collapse or gate lag.⁷ To verify our model on DHFET, we also compared results from numerical simulations of the model with gate-edge traps where In was incorporated in the channel to form the desired conduction band barrier. Figure 4 plots the resulting normalized drain current as a function of time for three different In mole fractions: 0%, 2%, and 5%, where the collapse clearly decreases as the mole fraction increases.

In summary, simulation results show that current collapse and gate lag take place only if an enhanced trapping occurs under the gate edges. No current collapse occurs for uniform trapping under the gate. Collapse results from trapping of hot electrons deep into the bulk, primarily under the

gate edges. The simulation results also link the current collapse with electrons spreading into the substrate, and confirmed that a better electron localization (as in a DHFET) can dramatically reduce current collapse. A possible approach for minimizing current collapse that follows from our simulations is gate-edge engineering, such as gate recess or double gate recess.

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