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We present a digital-oxide-deposition (DOD) technique to deposit high quality SiO_2 dielectric layers by plasma-enhanced chemical vapor deposition using alternate pulses of silicon and oxygen precursors. The DOD procedure allows for a precise thickness control and results in extremely smooth insulating SiO_2 layers. An insulating gate AlGaN/GaN heterostructure field-effect transistor (HFET) with 8 nm thick DOD SiO_2 dielectric layer had a threshold voltage of −6 V (only 1 V higher than that of regular HFET), very low threshold voltage dispersion, and output continuous wave rf power of 15 W/mm at 55 V drain bias. © *2006 American Institute of Physics*.
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III-nitride based heterostructure field-effect transistors (HFETs) are rapidly emerging as the most promising solid-state high-power rf sources since their demonstration in 1993 by Khan *et al.*[1] Very high power densities, 10–30 W/mm, which are close to the theoretical limits for this material system, have been achieved in the past two years.[2–4] One of the most critical issues limiting the performance of these devices at high rf power levels is the device degradation primarily caused by high gate leakage currents.[5–8] Insulated gate HFETs (IGHFETs) with SiO_2 and Si_3N_4 gate dielectrics[9,10] can potentially overcome this problem by reducing both the reverse and the forward gate leakage currents by several orders of magnitude. Such insulating gate devices have been reported[4,6] with much superior stability at high rf power levels as compared with the conventional Schottky gate HFETs.

The insulated gate HFET design leads to a larger threshold voltage. While it has been shown that the rf gain and the knee voltage for submicron IGHFETs are the same as those of submicron HFETs,[11] the larger gate-channel separation in the IGHFETs results in stronger short-channel effects. The reduced gate capacitance further makes IGHFETs more vulnerable to the effects of parasitic circuit capacitances. Thus, the IGHFETs with threshold voltages close to those of HFETs are very desirable. Such devices can be achieved either (i) by reducing the silicon dioxide or silicon nitride thickness or (ii) by using the materials with higher dielectric permittivity. In this letter, we focus on approach (i) to obtain low threshold IGHFETs with significantly reduced gate leakage currents.

The quality of the gate dielectric plays a crucial role in the insulated gate HFET device performance. The presence of interface and bulk charges in the dielectric film adversely affects the gate control by introducing threshold voltage and peak current dispersion. Most of the reported III-nitride IGHFETs used dielectric layers which are deposited using the plasma-enhanced chemical vapor deposition (PECVD) technique. This technique produces reasonable quality dielectric layers when the thicknesses are in excess of 10 nm. However, the PECVD dielectric layers, for thickness less than 10 nm, show increased leakage currents, threshold voltage dispersion, and poor reproducibility.

In this letter, we present the digital-oxide-deposition (DOD) approach to avoid the issues arising in very thin PECVD silicon dioxide layers. In the DOD process the silicon and oxygen precursor sources are alternatively supplied to the PECVD growth chamber. This increases the silicon

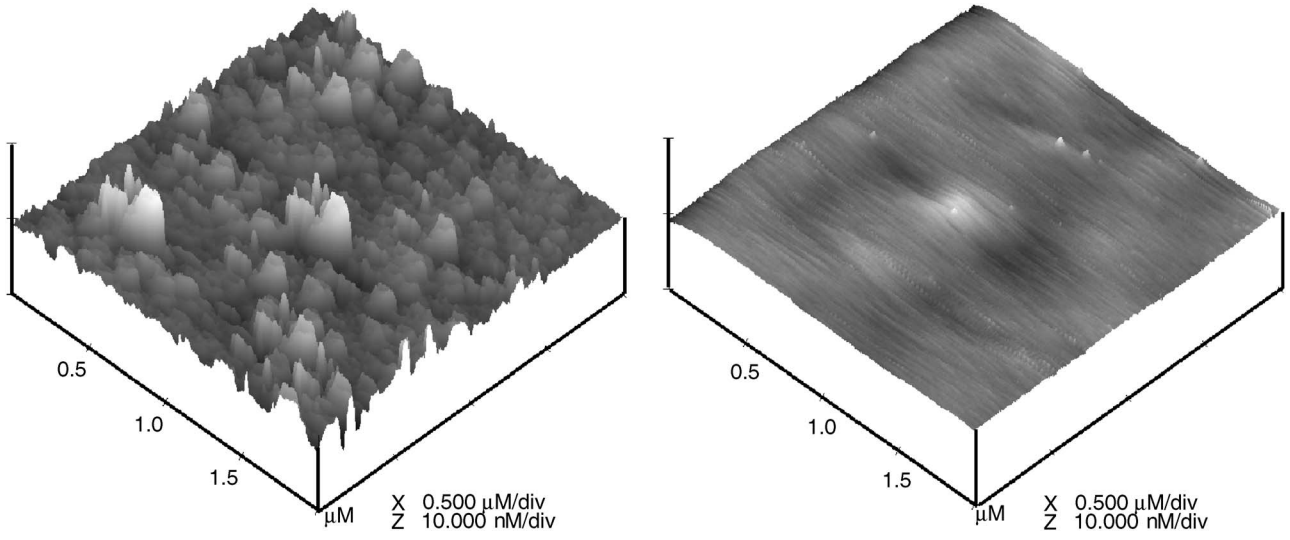

FIG. 1. AFM images of PECVD SiO_2 layers: (a) conventional deposition, and (b) digital oxide deposition.

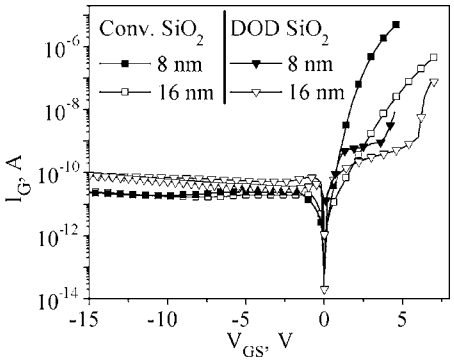

FIG. 2. Gate leakage characteristics of MOSHFETs using conventional and DOD SiO_2 layers.

atom surface mobility, allowing for a complete reaction with oxygen and thus providing the basis for superior atomic layer epitaxy. The DOD technique also suppresses unnecessary gas phase reactions due to the alternate supply of the precursors.[10] For the present study, SiO_2 gate dielectric layers with thickness ranging from 8 to 16 nm were deposited over AlGaN/GaN heterostructures. The depositions were carried out at a temperature of 250 °C. For comparison similar SiO_2 layers with the same thicknesses were also deposited using conventional PECVD technique, keeping the same process conditions except that the flows of the precursors were continuous and simultaneous.

The quality of the DOD and the conventional dielectric layers was characterized using an atomic force microscope (AFM). As shown in Figs. 1(a) and 1(b), the root mean square (rms) roughness for 8 nm silicon dioxide layers decreased by approximately a factor of 3 from 0.62 nm for conventional silicon dioxide to 0.24 nm for DOD silicon dioxide. This rms roughness for the DOD layers does not appreciably change when the thicknesses range from 8 to 16 nm. However, for conventional PECVD films the rms value decreased to 0.41 nm when the thickness was increased to 16 nm. The improvement in the film rms roughness resulted in significant reduction of the forward gate leakage currents as indicated in Fig. 2. It is clearly seen that even for the 16 nm conventional PECVD films, the forward gate leakage for IGHFET was higher than that for the device with an 8 nm thick DOD layer. Since the forward gate currents play a key role in determining the stability of the III-nitride HFETs at the maximum rf powers,[4,7] the IGHFETs with DOD layers should have a superior stability. Metal-oxide-semiconductor heterostructure field-effect transistors (MOSHFETs) with 8 nm thick DOD SiO_2 layers under the gate had threshold voltage of 6.0 V, which is only 1.0 V larger than that of the Schottky gate HFET fabricated from the same wafer. The transfer characteristics of these low threshold MOSHFETs and a conventional HFET (from the same wafer) are compared in Fig. 3(a).

The threshold voltage dispersion induced by the interface and the bulk charges in the gate insulator SiO_2 films was then studied by comparing the dc and pulse transfer characteristics of the conventional MOSHFETs and DOD MOSHFETs. Device width and the gate length were 100 and 1.2 μm, respectively. For pulse measurements, the dynamic *I-V* analyzer (DIVA) by Accent Optical Technologies, Inc. was used.[12] The devices were pulsed from the unbiased condition ($V_D=V_G=0$) with a pulse width of 0.2 μs. The threshold voltage obtained from pulse measurements was compared with that for dc biasing at 10 V drain bias. The difference between dc and pulsed threshold voltages was used as a measure for the threshold voltage dispersion. In Fig. 3(b), we show the threshold voltage dispersion as a function of thickness of the gate dielectric layer. For conventional PECVD SiO_2 films, the difference between the pulse and dc threshold voltages was found to linearly increase with the dielectric thickness. This observation suggests that the dispersion is primarily caused by the bulk charges in the SiO_2 layer rather than by the interface charges (at the SiO_2/AlGaN interface). For the DOD films, the dispersion is much lower as compared with that of conventional dielectric, indicating a significantly lower concentration of the bulk charges and hence the interface charges may be the dominating contribution. No threshold dispersion was observed for the HFETs.

The rf performance of low threshold MOSHFETs with DOD dielectric films was then studied on filed-plated devices fabricated as described in Ref. 5. The rf powers were measured at 2 GHz using a Maury automated tuning system. The device used for this measurement had a total width of 200 μm and a gate length of 1.2 μm. The rf powers at 3 dB gain compression point exhibit linear drain bias dependence. At 55 V drain bias, the output power of 15 W/mm was measured, closely corresponding to the powers expected from the device direct current-voltage (*I-V*) characteristics. This is indicative of a nearly current-collapse-free operation.

The rf stability tests were then performed on wafer at 2 GHz. The testing was carried out at room temperature without any cooling of probe station chuck. Before the rf stress, the devices were tuned for input and output impedance matching. After tuning, the drain bias of 55 V and the input power of 24 dB m were applied to reach the output power level corresponding to a 3 dB gain compression. The time dependency of the output powers for the DOD

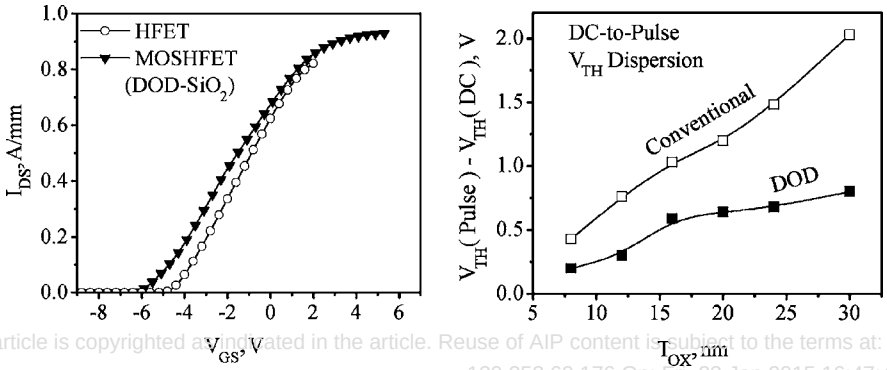

FIG. 3. (a) dc transfer characteristics of MOSHFETs using conventional and DOD SiO_2 layers and (b) dc-to-Pulse dispersion of V_{th} for conventional and DOD MOSHFETs.

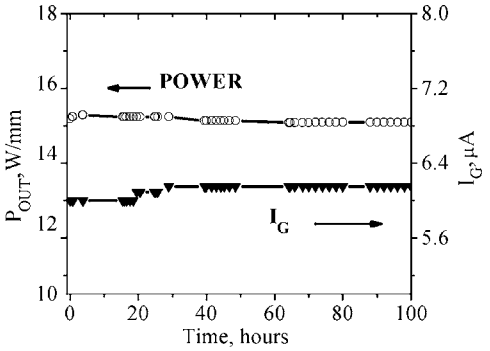

FIG. 4. rf power stability of the MOSHFET with DOD SiO_2

MOSHFET under the rf stress is shown in Fig. 4. As seen the output power remained remarkably constant during the stress, showing no appreciable drop for up to 100 h of cw operation when the test was stopped.

In conclusion, using the DOD technique, we were able to obtain very high quality silicon dioxide layers even with thicknesses as small as 8 nm. Using these layers for the gate dielectric, low threshold voltage MOSHFETs with very low gate leakage currents and voltage dispersion were fabricated. These MOSHFET devices delivered rf powers as high as 15 W/mm at 55 V drain bias. No rf power degradation was observed during a 100 h stress at a power level of 15 W/mm.

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