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Thermal Management of AlGaN–GaN HFETs on Sapphire Using Flip-Chip Bonding With Epoxy Underfill

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Abstract—Self-heating imposes the major limitation on the output power of GaN-based HFETs on sapphire or SiC. SiC substrates allow for a simple device thermal management scheme; however, they are about a factor 20–100 higher in cost than sapphire. Sapphire substrates of diameters exceeding 4 in are easily available but the heat removal through the substrate is inefficient due to its low thermal conductivity. The authors demonstrate that the thermal impedance of GaN based HFETs over sapphire substrates can be significantly reduced by implementing flip-chip bonding with thermal conductive epoxy underfill. They also show that in sapphire-based flip-chip mounted devices the heat spread from the active region under the gate along the GaN buffer and the substrate is the key contributor to the overall thermal impedance.

Index Terms—Epoxy underfill, flip chip, GaN AlGaN, HFETs, thermal impedance.

I. INTRODUCTION

ALGAN–GaN heterostructure field effect transistors (HFETs) [1], [2] have demonstrated great microwave power performance due to the high-breakdown field and the high-electron saturation velocity. For HFETs, the GaN–AlGaN epitaxial layers have been grown on either sapphire or SiC substrates. Although sapphire has the advantage of lower cost and availability in larger wafer sizes, its poor thermal conductivity ($\sigma \approx 0.3$ W/cm-K) limits the achievable powers due to severe self-heating. The thermal impedance can be significantly reduced by flip-chip (FC) mounting the devices onto highly conducting substrates such as AlN ($\sigma = 1.80$ W/cm-K). Such an FC mounting scheme has been demonstrated to achieve high-output power GaN HFETs on sapphire [3]–[5]. These past works used gold bump bonding and AlN carrier for device thermal management. However, no data was presented comparing devices with and without FC. In addition, there was

no discussion of the thermal impedance value and the effect of device design parameters on it. In this paper, we now present a novel thermal management approach for GaN HFETs over sapphire, which uses an FC technique with thermoconductive epoxy underfill. We demonstrate our approach to be effective for controlling the heat dissipation from the active area of device to the AlN substrate. We also show that the heat spread along the chip contributes significantly into the total thermal impedance of FC devices.

II. FC HFETs DESIGN, FABRICATION, AND CHARACTERIZATION

The HFET epilayers structures for our study were grown over basal plane sapphire or insulating SiC substrates using the low-pressure metal organic chemical vapor deposition (MOCVD) technique. The AlGaN–GaN layers were deposited at 1000 °C and 76 torr. The growth details were published elsewhere [6]. The ohmic contacts for source and drain were fabricated using e-beam deposited Ti(200 Å)–Al(500 Å)–Ti(200 Å)–Au(1500 Å). They were annealed at 850 °C for 1 min in nitrogen ambient. Ni(200 Å)–Au(1000 Å) gate electrodes were then deposited. The devices had a U-shaped double gate-finger geometry with a single gate length and width of 1.5 and 100 μm , respectively. Reactive ion etched mesas were used for device-to-device isolation. The devices were then FC bonded onto 500- μm -thick AlN substrate using gold bumps. No-flow epoxy underfill was then used to fill the air gap between the chip and the AlN substrate with thermoconductive material. Ours is the first report of using epoxy underfill for FC GaN based HFETs.

For our experiments, an automated FC die bonder RD M-10A system and thermoconductive boron nitride epoxy with low coefficient of thermal expansion (CTE) was used. The alignment accuracy of the RD system is within ± 1 μm . No flow underfill (controlled volume epoxy) is applied on the substrate through an advanced syringe dispensing system. The charge-coupled device (CCD) images of FC samples show that the bumps were aligned within ~ 6 μm from the gate electrode. The bumps' diameter and the height (after bonding) were about 120 and 10 μm , respectively.

For our experimental study of lateral heat spreading along the chip, we selected HFET devices on sapphire and SiC substrates with nearly identical peak currents (measured in pulsed mode to avoid the self-heating). The HFETs over sapphire substrates were also FC mounted with and without epoxy underfill.

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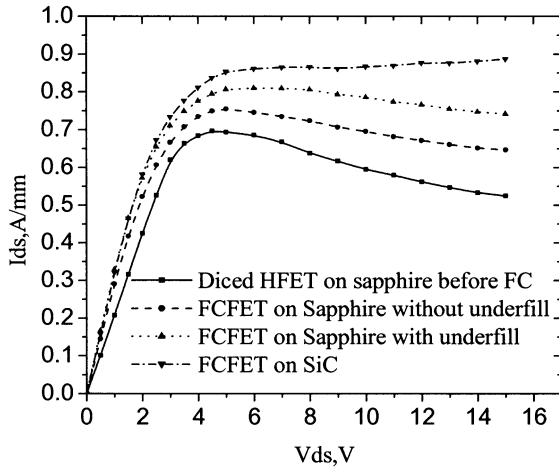


Fig. 1. DC I - V characteristics of HFETs over sapphire at $V_g = 0$ V after dicing, after FC bonding, after FC with epoxy underfill. Also shown is the I - V for FC HFET grown over SiC substrate.

TABLE I
THERMAL IMPEDANCE OF THE FC HFETs

Device packaging configuration	Thermal impedance
Diced HFET on sapphire before FC	51.7 K-mm/W
FC FET on sapphire without underfill	22.4 K-mm/W
FC FET on sapphire with underfill	16.5 K-mm/W
FC FET on SiC	4.9 K-mm/W

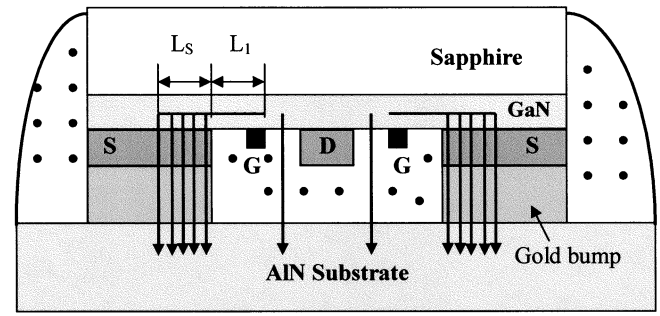
DC current-voltage I - V characteristics at zero gate bias for the different devices of this study are shown in Fig. 1. The I - V 's before and after FC without underfill are shown for the same device, other I - V 's are shown for devices with identical pulse peak currents. As seen, the FC bonding results in dramatic improvement of the dc- I - V characteristics. The threshold voltage and the gate leakage current practically did not change after the FC process.

The thermal impedance R_{th} of FC devices was then extracted by a comparison of the pulsed (200-ns pulse width, 0.05% duty cycle) and the dc I - V characteristics at different ambient temperatures. These values for the various packaging configuration in our study are summarized in Table I.

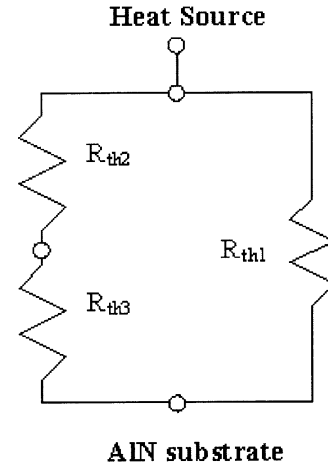
III. DISCUSSION

Schematic layout of an FC HFET device with gold bumps and epoxy underfill is shown in Fig. 2(a). The gold bumps ($\sigma = 3$ W/cm-K) serve as paths for heat dissipation as well as low-inductance connection. A simplified equivalent thermal impedance "network" for this design is shown in Fig. 2(b). Here, R_{th1} represents the heat flux through epoxy underfill region, R_{th2} is the impedance due to lateral heat spread along the chip, and R_{th3} is the thermal impedance of the gold bumps.

For the lateral heat flow in the HFET chip, one has to take into account the nonuniform heat spread in the bump area [see Fig. 2(a)]. This problem is very similar to the lateral electrical current spreading in the contact area as analyzed in [7]. Using



(a)



(b)

Fig. 2. (a) Schematics of the FC bonded AlGaIn-GaN HFETs with epoxy underfill. (b) Simplified thermal impedance network.

a thermo-electrical analogy and the approach developed in [7], we can estimate the effective heat-spreading length

$$L_S = \sqrt{\frac{\sigma_2}{\sigma_3}} \cdot d \cdot h \quad (1)$$

where the thermal conductivities of GaN and the bump are, respectively, $\sigma_2 \approx 1.6$ W/(cm-K) and $\sigma_3 \approx 3$ W/(cm-K), d is the thickness of GaN buffer, and $h \approx 10$ μ m is the bump height. The lateral component of thermal impedance R_{th2} can, therefore, be estimated as $R_{th2} = (1/\sigma_2) \times (L_1 + L_S)/d$ [please refer to Fig. 2(a)]. For our sample $d \approx 1.5$ μ m and $h \approx 10$ μ m, thus from (1) we find $L_S \approx 2.8$ μ m. Noting the gold-bump width to be 120 μ m, we conclude that only the edge of the bump contributes significantly into heat removal from the chip. Using $L_1 \sim L_G + L_{GS} \approx 2.5$ μ m, where $L_G \approx 1$ μ m and $L_{GS} \approx 1.5$ μ m are the gate length and the gate-source spacing, respectively, we estimate $R_{th2} \approx 22.1$ K-mm/W. For a 5- μ m-thick buffer R_{th2} can be as low as 16 K-mm/W. The thermal impedance of the gold bumps can be found as follows [8]:

$$R_{th3} = \frac{1}{\pi \sigma_3} \ln \left(\frac{16h}{\pi L_S} \right). \quad (2)$$

This results in $R_{th3} \approx 3.1$ K-mm/W $\ll R_{th2}$. Therefore, the lateral heat spread along the HFET chip is the limiting factor in the overall thermal impedance of the FC samples. This analysis, therefore, shows GaN buffer thickness to be the key controller of

lateral thermal impedance and hence the thermal management of FC devices over sapphire [9]. This conclusion is clearly supported by the experimental data of Table I.

The value of R_{th1} associated with epoxy filling can be estimated from (2), replacing σ_3 with the epoxy thermoconductivity $\sigma_1 \approx 0.05$ W/(cm-K), and L_S with L_0 , where L_0 is the effective width of the heat source. Using (1) we can see that for GaN-epoxy interface $L_S \approx 20$ μm , i.e., much larger than the entire source-drain spacing, $L_{\text{DS}} = 5$ μm for our samples. Therefore, considering the heat flow through epoxy underfill, the effective length of the heat source is about $L_0 \approx L_{\text{DS}} = 5$ μm . From (2), we can now find the thermal impedance associated with epoxy underfill, $R_{\text{th1}} \approx 140$ K-mm/W. We can see that epoxy underfill improves the total thermal impedance by about 20%. This agrees quite well with the experimental data of Table I for the FC devices with and without epoxy underfilling (lines 2 and 3). The RF performance analysis of the FC devices is undergoing; however, a simple estimate shows that with a typical 40% PAE in class A mode, the maximum active region temperature of 250 °C and 16.5 K-mm/W thermal impedance the RF power of ~ 6 W/mm can be achieved using FC devices.

IV. CONCLUSION

In conclusion, we report the thermal management of AlGa_N-Ga_N HFETs on sapphire by FC bonding with epoxy underfill. We show the FC bonding procedure not to affect the device performance parameters. Compared to a diced chip, the thermo-compression gold bump FC bonding with epoxy

underfill decreases the thermal impedance of HFETs over sapphire by a factor of three. Our experimental data and heat spread analysis show that the thermal impedance can be further reduced by increasing the GaN buffer layer thickness.

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