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MODELING OF SIC POWER SEMICONDUCTOR DEVICES FOR SWITCHING CONVERTER APPLICATIONS

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ABSTRACT

Thanks to recent progress in SiC technology, SiC JFETs, MOSFETs and Schottky diodes are now commercially available from several manufactories such as Cree, GeneSiC and Infineon. SiC devices hold the promise of faster switching speed compared to Si devices, which can lead to superior converter performance, because the converter can operate at higher switching frequencies with acceptable switching losses, so that passive filter size is reduced. However, the ultimate achievable switching speed is determined not only by internal semiconductor device physics, but also by circuit parasitic elements. Therefore, in order to accurately predict switching losses and actual switching waveforms, including overshoot and ringing, accurate models are needed not only for the semiconductor devices, but also for the circuit parasitics.

In this dissertation, a new physics-based model accounting for non-uniform current distribution in JFET region for the power SiC DMOSFET is presented. Finite element simulation shows that current saturation for typical device geometry is due to two-dimensional (2-D) carrier distribution effects in JFET region caused by current spreading from the channel to the JFET region. Based on this phenomenon, a new model is proposed that represents the non-uniform current distribution in the JFET region using a non-linear voltage source and a resistance network. Advantages of the proposed model are that a single set of equations describes operation in both the linear and saturation regions, and that it provides a more physical description of MOSFET operation. The model represents an original contribution in the area of physics-based power

semiconductor device modeling. This model is validated both statically and under resistive conditions for SiC DMOSFET showing overall good matching with experimental results and finite element simulations.

This dissertation also presents a simple physics-based power Schottky diode model which is comprised of a voltage controlled current source, a temperature dependent drift region resistance and a nonlinear capacitance. A detailed parameter extraction procedure for this model is also discussed in this work. The developed procedure includes the extraction of doping concentration, active area and thickness of drift region, which are needed in the power Schottky diode model. The main advantage is that the developed procedure does not require any knowledge of device fabrication, which is usually not available to circuit designers. The only measurements required for the parameter extraction are a simple static I-V characterization and C-V measurements. Furthermore, the physics-based SiC Schottky diode model is also temperature dependent and is generally applicable to SiC Schottky diodes. This procedure is demonstrated for four different Schottky diodes from two different manufacturers. The parameter extraction procedure represents an original contribution in the area of characterization of power semiconductor devices.

In order to capture the parasitic ringing in the very fast switching transients, a procedure to accurately model circuit parasitics is also presented. A double pulse test-bench was built to characterize the resistive and inductive switching behavior of the SiC devices. The parasitic inductances for resistive and inductive switching of SiC devices in this switching test circuit were modeled and analyzed using a three-dimensional (3-D) inductance extraction program. The gate-to-source switching loop and drain-to-source

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LIST OF SYMBOLS

β	Constant for saturation velocity
ε_r	Relative dielectric constant
ε_{SiC}	Dielectric constant of silicon carbide (F/cm)
φ_b	Barrier height between the metal and N-type semiconductor (V)
μ_{300}	Electron mobility at room temperature T=300K (cm^2/V s)
μ_n, μ_D	Electron mobility (cm^2/V s)
μ_{CH0}	Low-field mobility in inversion layer (cm^2/V s)
$\mu_D(T)$	Temperature dependent electron mobility (cm^2/V s)
$\mu_{n\text{-}drift}$	Electron mobility in drift region (cm^2/V s)
μ_{CH}	Channel mobility (cm^2/V-s)
μ_A	Accumulation layer mobility (cm^2/V s)
μ_{JFET}	JFET region mobility (cm^2/V-s)
a	Half of width of channel region (cm)
a_i	Ratio of intercell area to total die area
A	Active area (cm^2)
A^*	Effective Richardson constant (A cm^{-2} K^{-2})
C_{GD}	Capacitance between gate and drain (F)
C_{DS}	Capacitance between drain and source (F)

C_{GS} Capacitance between gate and source (F)

C_{OX} Oxide capacitance per unit area (F/cm^2)

c_{OX} Oxide capacitance (F)

C_r Non-linear capacitance of Schottky diode (F)

E_C Critical breakdown electric field (kV/cm)

E_{max} Maximum electric field (V/cm)

E_k Peak electric field at the end of MOSFET channel (V/cm)

I_D Drain current (A)

I_{DSAT} Saturation drain current (A)

I_F Forward current of Schottky diode (A)

I_F Reverse current of Schottky diode (A)

I_{SCH} Current going through Schottky diode (A)

k Boltzmann's constant (eV/K)

L_D Thickness of drift region (cm)

L_{CH} Length of channel (cm)

L_{DRIFT} Length of drift region (cm)

L_{JFET} Length of JFET region (cm)

L_R Distance between adjacent nodes in JFET region (cm)

L_D Drain-to-source switching loop parasitic inductance (H)

L_{DD} Parasitic inductance of free-wheeling diode path (H)

L_G Gate-to-source switching loop parasitic gate inductance (H)

L_S MOSFET source-leg parasitic inductance (H)

n	Ideality factor
N_{DRIFT}, N_D	Doping concentration of drift region (cm^{-3})
N_{JFET}	Doping concentration of JFET region (cm^{-3})
q	Fundamental electronic charge (C)
R_{ai}	Accumulation layer resistance (Ω)
R_{DRIFT}	Drift region resistance (Ω)
R_G	Gate resistance (Ω)
R_{JFET}	JFET region resistance (Ω)
R_{J_net}	Resistance of JFET region network (Ω)
$R_{on,sp}$	Specific on-resistance ($\Omega \cdot cm^2$)
S_1	Slope of I-V curve for Schottky diode
S_2	Slope of $1/C^2$-V curve for Schottky diode
T	Absolute temperature (K)
v_{sat}	Carrier saturation velocity in silicon carbide (cm/s)
V_{bi}	Built-in voltage in gate source junction (V)
V_{BR}, V_B	Breakdown voltage (V)
V_{CH}	Channel voltage (V)
$V_{CH,SAT}$	Saturation voltage of the channel (V)
V_D	Voltage applied to Schottky diode (V)
V_{DR}	Voltage across Schottky diode (V)
V_{DS}	Voltage applied to drain and source (V)
V_{GS}	Voltage applied to gate and source (V)

V_{GD}	Voltage applied to gate and drain (V)
V_i	Voltage at the node of corresponding i resistor (V)
V_{JFET}	Total voltage in JFET region (V)
V_R	Reverse bias of Schottky diode (V)
V_T	Threshold voltage (V)
W'	Length of the depletion region under the gate oxide (cm)
W_{DRIFT}	Width of drift region (cm)
W_{DS}	Width of depletion region between drain and source (cm)
W_{GS}	Width of depletion region between gate and source (cm)
W_{JFET}	Depletion layer length of the depletion region under the gate which only begins to grow when $V_{DS}=V_{GS}$ (cm)
W_r	Depletion layer thickness of Schottky diode (cm)
x	Temperature coefficient of carrier mobility
Z	Length of device in vertical-to-paper dimension (cm)

CHAPTER 1

INTRODUCTION

1.1 SILICON CARBIDE MATERIAL PROPERTIES FOR POWER ELECTRONICS APPLICATIONS

With the widespread use of medium voltage motor drives, flexible AC transmission systems (FACTS), high voltage DC (HVDC) systems and hybrid electric vehicles, the efficiency and reliability of power electronic converters used in these applications is getting more and more important [1][2][3][4]. Some of these applications require large breakdown voltage capability, high power density and high temperature. Most present commercial power semiconductor devices such as p-i-n diodes, MOSFETs, IGBTs, GTOs and thyristors are silicon-based devices. The performance of these Si-based devices is approaching their theoretical limit in high power applications due to its intrinsic material properties, which make Si-based devices a limiting factor for high-voltage, high-efficiency and high-temperature applications. For high blocking voltages, IGBTs and GTOs are commonly used. However, these devices have relatively slow switching speed. MOSFETs are well-suited for high-switching-frequency applications up to MHz frequencies, but suffer from relatively high on-state resistance as the blocking voltage increases, which mean high on-state voltage drop and high conduction loss. Furthermore, the maximum operating temperature for silicon devices is around 150 ℃, which dictates the thermal management system size and

weight. Therefore, there is an urgent need to develop new power electronics devices for severe thermal environment or reduced cooling, high voltage and high efficiency systems.

Table 1-1 Physical characteristics of Si and 4H- SiC

Properties	Si	4H- SiC
Bandgap, Eg (eV)	1.12	3.26
Relative dielectric constant, ε_r	11.9	10.1
Critical electric field, E_C (kV/cm)	300	2200
Electron mobility, μ_n (cm^2/V·s)	1500	1000
Hole mobility, μ_h (cm^2/V·s)	600	115
Thermal conductivity, (W/cm·K)	1.5	4.9
Saturated electron drift velocity, v_{sat} ($\times 10^7$ cm/s)	1	2

In order to improve the performance of semiconductor devices, alternative semiconductor materials with better characteristics are being sought. In particular wide bandgap materials such as Silicon Carbide (SiC) appear particularly promising. Excellent electrical properties of silicon carbide (SiC) material, such as wider bandgap, higher thermal conductivity, and higher critical breakdown electric field, make it a very attractive semiconductor material for power switching devices with capabilities that are superior to those of devices based on silicon technology [1]-[10]. 4H-SiC MOSFET is one of the most promising candidates for high-speed and low-loss power switching applications. Table 1-1 compares the physical characteristics of Si and 4H- SiC materials [2]. As seen in Table 1-1, the band gap of 4H- SiC (3.26eV) is nearly three times that of Si. A large bandgap results in lower leakage currents than silicon, in a much higher operating temperature and higher radiation hardness. The higher critical electric field (2.2×10^6 V/cm, which is almost ten times larger than Si) allows the design of SiC power

devices with thinner and more highly doped voltage blocking layers and, as a consequence, a lower on-resistance for a given breakdown voltage is achievable. Especially for power unipolar devices like MOSFETs and Schottky diodes, specific on-resistance is mainly determined by a low-doped drift region, which is necessary to block high voltage.

Figure 1.1 shows electric field distribution in a drift region of thickness L_D. Electric field E_C is the critical breakdown electric field. The carrier concentration is optimized so that the maximum electric field E_{max} reaches the critical value E_C when the drift region is completely depleted as shown in Figure 1.1.

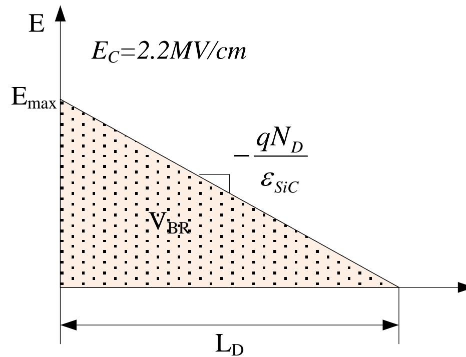


Figure 1.1 Electric field distribution in drift region for SiC

The breakdown voltage V_{BR} is the integral of the electric field and it is equal to the triangle area as shown in Figure 1.1 [11] [12]. When the maximum electric E_{max} is equal to the critical breakdown electric field E_C, which means that the drift region is blocking the largest possible voltage, this breakdown voltage V_{BR} is given by Equation 1-1.

$$V_{BR} = \frac{E_C \cdot L_D}{2} \quad \text{Equation 1-1}$$

According to Poisson equation, the slope of the electric field curve in Figure 1.1 is given by qN_D / ε_{SiC}, where N_D is the drift region doping concentration and ε_{SiC} is SiC

dielectric constant. Therefore, the maximum electric field E_C in the drift region shown in Figure 1.1 is given by:

$$E_C = \frac{qN_D L_D}{\varepsilon_{SiC}} \qquad \text{Equation 1-2}$$

The specific on-resistance of the drift region, which is defined as the ideal specific on-resistance, is given by

$$R_{on,sp(ideal)} = \frac{L_D}{q\mu_n N_D} \qquad \text{Equation 1-3}$$

where q is the electron charge and μ_n is the electron mobility. From Equation 1-1 and Equation 1-2, one can get the following equation for the doping concentration of drift region.

$$N_D = \frac{\varepsilon_{SiC} \cdot E_C^2}{2q \cdot V_{BR}}. \qquad \text{Equation 1-4}$$

Substituting Equation 1-1 and Equation 1-4 into Equation 1-3 gives the ideal specific on-resistance as Equation 1-5.

$$R_{on,sp(ideal)} = \frac{4V_{BR}{}^2}{\varepsilon_{SiC}\mu_n E_C^3} \qquad \text{Equation 1-5}$$

Equation 1-5 clearly shows that specific on-resistance of unipolar devices is inversely proportional to the cube of critical breakdown electric field E_C of the semiconductor material. The same equation applies for other semiconductor material such as Si. Because the critical breakdown electric field of SiC is almost 10 times more than that of Si, Equation 1-5 shows that the ideal specific on-resistance of SiC can be almost 1000 times smaller than that of Si. Figure 1.2 shows the comparison of the ideal specific on-resistance of 4H-SiC and Si devices as a function of breakdown voltage. The

specific on-resistance of SiC device is somewhat less than 1000 times smaller than that of Si due to the lower electron mobility of SiC with respect to Si.

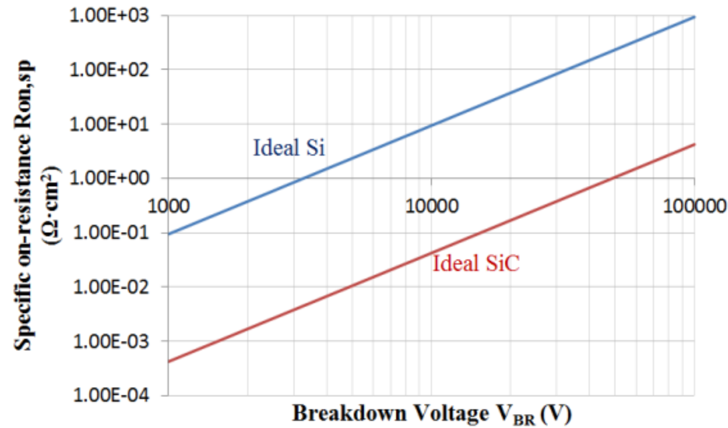


Figure 1.2 Ideal specific on-resistance of drift regions in 4H-SiC and Silicon.

Furthermore, the high thermal conductivity (4.9 W/cm·K) of SiC semiconductor material facilitates heat removal and avoids the need for bulky and expensive cooling systems in most applications. This, in turn, translates into high cost savings in mass critical applications.

All of the above advantages of SiC material make it an attractive material for high voltage, high power, high frequency, high temperature, and high efficiency converter systems.

1.2 Research Motivations and Objectives

Thanks to recent progress in SiC technology, SiC JFETs, MOSFETs and Schottky diodes are now commercially available from several companies such as Cree, GeneSiC and Infineon. Since power devices play important roles in power electronics applications, in order for the power electronics designers to fully utilize the performance advantages of power devices, compact power device models are needed in the circuit simulators used in the design process (P-spice, Saber, MATLAB Simulink, VTB and so on) [13].

Therefore, it is very important to create accurate device models to evaluate the performance of SiC prototype devices in different applications and guide the switching converter design process. This dissertation focuses on modeling of SiC power semiconductor devices such as power MOSFET and Schottky diode for switching converter applications.

In this dissertation, a new circuit-based SiC DMOSFET model that physically captures the mechanism of current saturation in power SiC DMOSFET is developed in PSpice software based on finite element simulation results. A simple SiC Schottky diode model is proposed together with a specific parameter extraction procedure. In order to validate the proposed SiC MOSFET and Schottky diode models, a double pulse test-bench was built to experimentally evaluate the resistive and inductive switching behavior of the devices. Both models have been verified by comparing simulation results with the experimental results.

Since both devices operate at a very fast switching transient, it is very important to capture the parasitic ringing during the switches of the devices. The extraction of parasitic inductances of the switching circuit is another focus of this dissertation besides the device models. A simple extraction method of parasitic inductances is developed for the PCB layout of the double pulse test-bench. The extracted parameters of the gate-to-source switching loop and drain-to-source switching loop of the PCB layout are used in the simulation circuit of the double pulse test-bench for model validation. Finally, based on the study of the effect of parasitic inductances in fast switching circuit, the factors that affect the accuracy of waveform prediction for switching converter are discussed for optimized circuit layout of SiC power devices in fast speed circuit applications.

1.3 DIFFICULTIES AND CHALLENGES

In order to accurately predict the switching behavior of SiC-based power switching converters, it is necessary to have accurate models for the SiC power devices and for the parasitic inductances in the switching loops of the converters. However, there are many challenges related to the development of suitable SiC power device models and the prediction of high- speed switching behavior.

1.3.1 SIC DEVICE MODELS

Due to the development of new power devices with new internal structure and new SiC semiconductor material, there are many challenges in developing accurate device models for these new power semiconductor devices. A good device model for circuit design should ideally satisfy the following basic rules:

1) The model should be able to predict static I-V characteristic with reasonable accuracy.
2) Since the built-in device parasitic capacitances play an important role in determining the device dynamic behavior, a good model should include an accurate model for all these parasitic capacitances.
3) The model should provide accurate device loss predictions during on- state and off- state.
4) The model should capture temperature-dependent behavior over the entire temperature operating range of the switching converter applications. In other words, the model should be temperature dependent.

5) The model should have as few parameters as needed to accurately capture device behavior including static characteristics and dynamic characteristics, and these parameters should be related to the device structure and fabrication processing (for example active area, oxide thickness, doping concentration, and the thickness of the device). Empirical parameters without physical meaning should be avoided as much as possible.

It is difficult to create a device model to meet all the rules above. In the literature several device models have been presented for SiC MOSFETs and Schottky diodes. They can be divided in two major groups: 1) analytical models based on the finite element solution of drift-diffusion carrier transport in two or three dimensions [14] - [16]; and 2) circuit-oriented models which employ equation-based description of device behavior. Analytical models provide very high accuracy but require long simulation time and detailed information about device fabrication, while circuit-based models require much less time for simulation with acceptably accurate results using model parameters that can be extracted from experimental measurements. An additional advantage of physics-based circuit-oriented models is that they are compatible with circuit simulators and can be used to simulate an entire switching converter. New physics-based circuit-oriented SiC MOSFET and Schottky diode models will be developed in this dissertation.

1.3.2 Parasitic Component Modeling

The significant advances in power electronics have led to improved performance of DC-DC converters. New applications of power electronic systems create a demand for high power density and high frequency converters. In order to realize high frequency

switching in a practical application, it is necessary to establish high speed switching techniques. However, there are many challenges that remain to be resolved. In particular, electromagnetic interference (EMI) issues and switching losses are still serious problems with high speed switching, due to the influence of the parasitic components of power electronics circuits, such as the parasitic inductance of both the power devices and printed circuit board (PCB) traces [17] - [23].

Different parasitic parameters affect the device stresses, switching energy losses, as well as electromagnetic interference (EMI) for very high frequency applications. One of the major challenges is to predict, with satisfactory accuracy the switching waveforms of the converter. To achieve this task, precise models of all components of the converter must be used. In particular, it is important to extract the layout parasitic parameters in Printed Circuit Board (PCB) and use them in the simulation. The main parasitic parameters include the switching loop impedances and the device output junction capacitances. All these parasitic parameters can help better understand the high switching-speed behavior of these SiC switches.

1.4 CONTRIBUTIONS

There are two original contributions in this dissertation.

One is the development of a new physics-based SiC DMOSFET model accounting for non-uniform current distribution in JFET region based on finite element simulation results. This model represents the non-uniform current distribution in the JFET region using a non-linear voltage source and a resistance network. Advantages of the proposed model are that a single set of equations describes operation in both the

linear and saturation regions, and that it provides a more physical description of MOSFET operation.

The other original contribution is the parameter extraction procedure for a simple physics-based SiC Schottky diode model. The developed procedure for the simple Schottky diode model includes the extraction of doping concentration, active area and thickness of drift region. The main advantage is that the developed procedure does not require any knowledge of device fabrication, which is usually not available to circuit designers. The only measurements required for the procedure are a set of static I-V characterization and C-V measurements.

Other contributions of this dissertation include:

1) A double pulse test-bench was built to characterize the resistive and inductive switching behavior of the SiC devices.
2) The parasitic inductances for resistive and inductive switching of SiC devices in this switching test circuit were modeled and analyzed using a three-dimensional (3-D) inductance extraction program FASTHENRY.
3) The gate-to-source switching loop and drain-to-source switching loop parasitic inductances of the PCB layout are extracted and simulated together with previously developed power SiC device models in Pspice under both resistive and inductive switching conditions.

1.5 SUMMARY

Silicon carbide (SiC) power devices are very promising in high-speed switching converter applications because of the superior material properties of SiC comparing with silicon. So far, SiC MOSFET and Schotkky diode are commercially available from

several companies, such as Cree, GeneSiC and SiCED. Modeling of these great devices is very important for circuit engineers to predict the switching behavior of the SiC-based converter applications. One focus of the dissertation is modeling of SiC power semiconductor devices such as power MOSFET and Schottky diode for fast switching applications. The extraction of parasitic inductances of the switching circuit is another focus of this dissertation to better predict the switching behavior of SiC devices.

CHAPTER 2

POWER SEMICONDUCTOR DEVICES

Power semiconductor devices are semiconductor devices used as a switch in power electronics. With the fast developments of medium voltage motor drives, flexible AC transmission systems (FACTS), high voltage DC (HVDC) systems, PV (photovoltaics) and hybrid electric vehicles, the requirements for power semiconductor devices include high voltage, high current, high switching speed and high efficiency. So far there are many kinds of power semiconductor devices commercially in the market, such as insulated gate bipolar transistor (IGBT), metal oxide semiconductor field effect transistor (MOSFET), PiN diode, Schottky diode, thyristor and integrated gate commutated thyristor (IGCT), and so on.

Power semiconductor devices can be divided into two different groups. There are minority carrier devices such as IGBT, PiN diode and thyristor, and majority carrier devices such as power MOSFET and Schottky diode which are discussed in this chapter.

2.1 Vertical Power MOSFET

Power MOSFET was the first commercially successful unipolar device developed using silicon material, after resolving the problems related to the metal oxide semiconductor interface for CMOS technology. The operation of power MOSFET is dependent on the formation of a conductive channel at the surface of the semiconductor

under the gate oxide layer [12]. There are several kinds of vertical power MOSFET structure so far, including VMOSFET which is named from the V-shaped gate region, DMOSFET which is named from the planar double-diffusion technology of the gate and UMOSFET whose channel is vertical because of the U-groove gate structure. Figure 2.1 shows the power DMOSFET structure. The thickness and doping concentration of drift region determine the blocking capability of the MOSFET. Higher blocking voltage requires lower doping concentration, which leads to higher on-resistance. Therefore, there is a trade-off between on-resistance and blocking voltage in power MOSFET design, as shown in Figure 1.2.

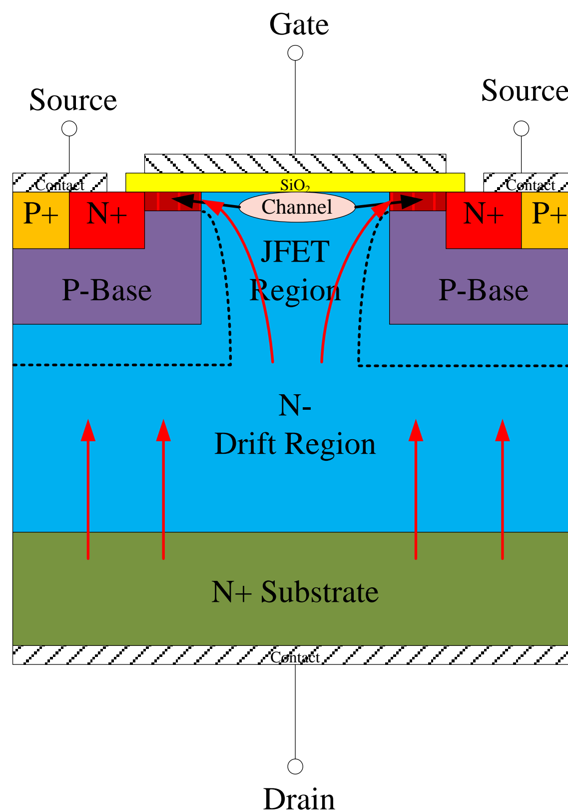


Figure 2.1 Power DMOSFET structure

From the structure shown in Figure 2.1, one can see that there is a parasitic NPN bipolar transistor in the MOSFET structure. This parasitic BJT should be kept in the off-

state in all operating modes of the MOSFET otherwise this could lead to device latch-up and loss of gate control. In order to satisfy this condition, the P-base region is shorted to the source contact through the P+ region, as shown in Figure 2.1. Besides the parasitic BJT in the structure, there is a P-N junction connecting the source region to the drain region, which is called built-in body diode of the MOSFET. This body diode is usually used as free-wheeling diode in some power electronic applications.

2.1.1 STATIC I-V CHARACTERISTICS

When a positive voltage is applied to the gate-to-source terminal, a conductive electron channel is formed at the surface of the semiconductor under the gate and connects the JFET region to N+ region at the source, as shown in Figure 2.1. This channel provides an electron current flow path between drain and source. The on-resistance during on-state is determined by the total resistance of the current path shown in the figure, which is comprised of resistances of the N+ substrate, the N- drift region, the JFET region, the channel resistance, and the N+ region connected to the source and. Usually one can neglect the resistances in the N+ substrate and the N+ region that is connected to the source because of the high doping concentrations in these regions. The on-resistance is a very important parameter of the MOSFET because it determines the current capability of the device [12]. It can be extracted from the slope of the I-V characteristics in the linear region at low voltage which is shown in Figure 2.2.

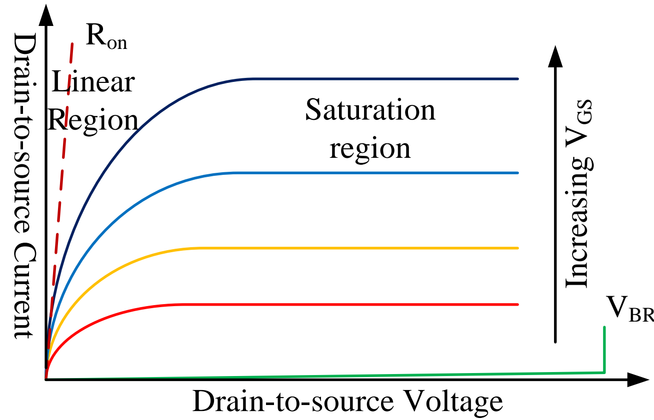


Figure 2.2 I-V Characteristics of Power DMOSFET

When drain-to-source voltage V_{DS} increases to a certain value, the device goes into the saturation region, where the drain-to-source current I_{DS} saturates as shown in Figure 2.2. In this region device losses are high, since significant voltage and current are both present at the same time. When the power MOSFET is working as a switch in switching converter application, it is necessary to avoid the device operating in the saturation region due to the limitation of high power dissipation of the device.

2.1.2 Blocking Characteristics

Power MOSFET has positive blocking voltage capability. When the gate-to-source voltage V_{GS} is zero or negative, the device can support a large drain-to-source voltage V_{DS} across the P-base/ N- drift region junction with a little leakage current going through the device (see the green line in Figure 2.2). Actually, during the off-state operation, the depletion layer (see the black dashed line in Figure 2.1) extends out from the P-base/ N-drift region junction to support the applied drain-to-source voltage. Figure 2.3 shows the depletion layer extension under off-state operation of power MOSFET for both low and high drain-to-source voltage V_{DS}. The blocking capability of power

MOSFET is not only limited by the thickness of the devices and the doping concentration of N-drift region, but also by the structure inside the devices, such as the P-well spacing.

According to the discussion of advantages of material properties for SiC compared with Si, SiC has almost 10 times larger critical breakdown electric field than Si. From Equation 2-1 which is the expression of breakdown voltage of semiconductor material, one can get almost 100 times higher breakdown voltage V_{BR} for SiC-based device than for Si-based device for the same doping concentration.

$$V_{BR} = \frac{\varepsilon_{SiC} \cdot E_C^2}{2q \cdot N_D} \qquad \text{Equation 2-1}$$

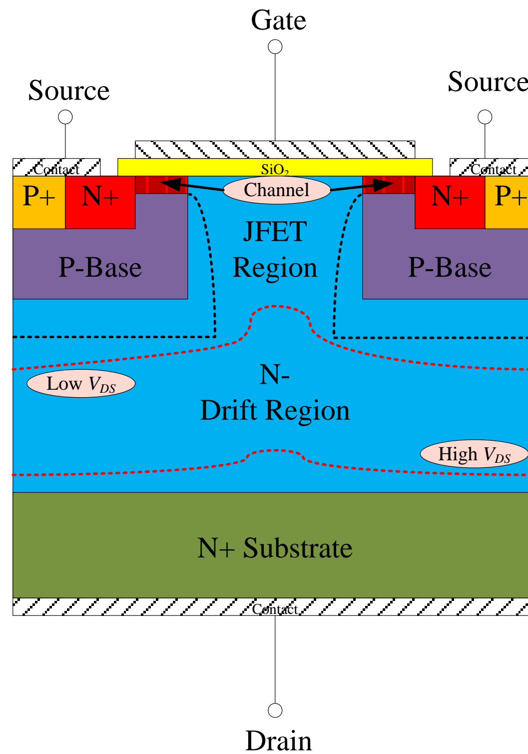


Figure 2.3 Depletion layer extension of power MOSFET

2.1.3 Dynamic Characteristics

There are three major parasitic capacitances in power MOSFET, which are the gate-to-source capacitance C_{GS}, the gate-to-drain capacitance C_{GD} and the drain-to-source

capacitance C_{DS}, as shown in Figure 2.4. It is very important to accurately model the inner parasitic capacitances of power MOSFET in order to accurately capture its dynamic characteristics, especially the modeling of the gate-to-drain capacitance (C_{GD}), which affects the output switching waveforms due to the “Miller” effect. The dynamic behavior of power MOSFET is usually dominated by the charging and discharging of the input capacitance seen from the controlling gate terminal. Because of the Miller effect of capacitance C_{GD}, the equivalent input capacitance of the MOSFET will be the gate-to-source capacitance C_{GS} in parallel with the amplified value of gate-to-drain capacitance C_{GD} during the switching transient.

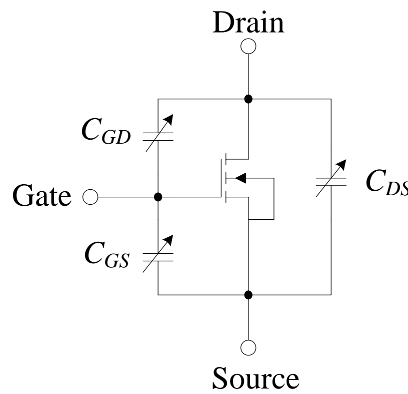


Figure 2.4 Inner parasitic capacitances of power MOSFET

There are two methods to improve the switching speed of the power MOSFET. One is reducing the gate resistance R_G, the other one is minimizing the parasitic capacitances C_{GS} and C_{GD}. Reducing the gate-to-source capacitance shortens the charging and discharging time of the MOSFET and decreasing the gate-to-drain capacitance C_{GD} reduces the Miller effect, so that the switching time can be faster.

Figure 2.5 shows the inner parasitic capacitances of a 1.2kV power MOSFET in ATLAS finite element simulation. One can see that the gate-to-source capacitance C_{GS} is almost constant with increasing drain bias. But the gate-to-drain capacitance C_{GD} changes

with increasing drain-to-source voltage. One can see that this Miller capacitance decreases abruptly at low voltage, which affects the dynamic behavior of the MOSFET severely during switching time. Therefore, in order to develop an accurate model for power MOSFET, it is very important to take into account the non-linear gate-to-drain capacitance C_{GD}.

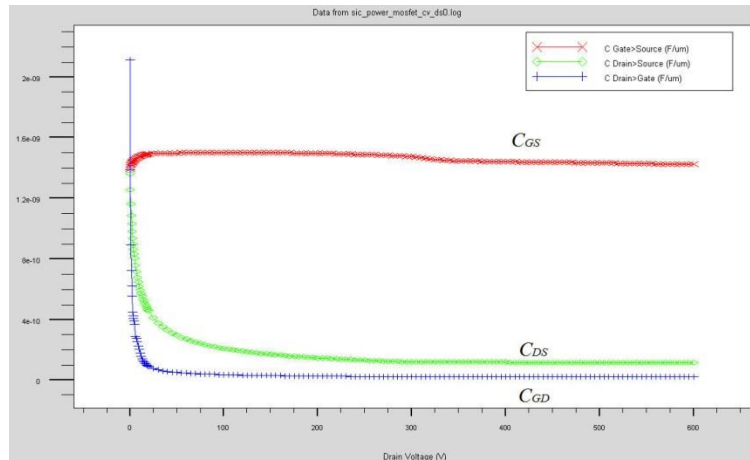


Figure 2.5 Inner capacitances of a 1.2kV power MOSFET in ATLAS simulation

2.2 POWER SCHOTTKY DIODE

Power Schottky diode has a Metal-Semiconductor (MS) junction, as shown in Figure 2.6. A metal–semiconductor junction is formed between a metal and a semiconductor, creating a Schottky barrier. Unlike the power P-i-N junction, power Schottky diode is majority carrier device which does not require a reverse recovery current to discharge the minority carriers in the depletion region in the device. Therefore, power Schottky diode is a very fast switching semiconductor device that can be used in higher frequency switching converter compared to power P-i-N diode.

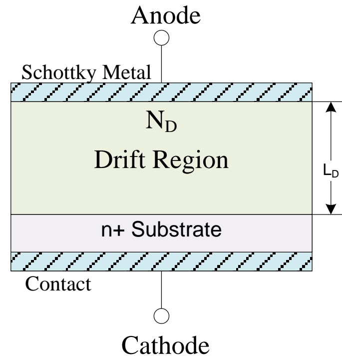


Figure 2.6 Power Schottky diode structure

2.2.1 FORWARD CHARACTERISTICS

When a positive voltage is applied to the metal contact with respect to the N-type semiconductor, the electrons in semiconductor side overcome the Schottky barrier to the metal side creating the forward conduction current [12]. The forward current can be calculated by using the thermionic emission theory.

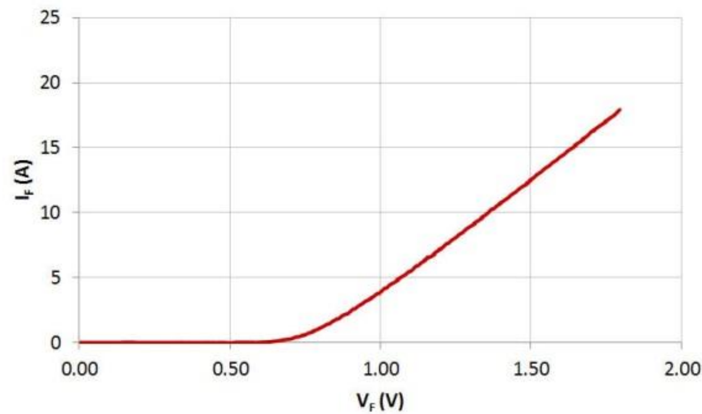


Figure 2.7 Typical forward characteristics of power Schottky diode

$$I_F = AA^*T^2e^{-(q\varphi_b/kT)}[e^{(qV/kT)} - 1] \quad \text{Equation 2-2}$$

where A is the active area, $A*$ is the effective Richardson constant, T is the absolute temperature, q is the electron charge, k is Boltzmann's constant, φ_b is the barrier height between the metal and N-type semiconductor, and V is the applied voltage. Figure 2.7 shows the typical forward I-V curve of power Schottky diode.

2.2.2 REVERSE CHARACTERISTICS

When a negative voltage V_R is applied to the metal contact with respect to the N-type semiconductor, a depletion layer will be formed in the semiconductor side to support the applied voltage. Since the N-type semiconductor holds all the blocking voltage, one can also use Equation 2-1 to calculate the breakdown voltage of the power Schottky diode at a certain doping concentration.

The leakage current of Schottky diode under reverse bias is also dominated by the thermionic current across the Schottky barrier, which can be calculated by Equation 2-3. From this equation, one can see that the leakage current of Schottky diode is dependent on temperature. This limits power Schottky diode operation in high temperature applications.

$$I_R = AA^*T^2e^{-(q\varphi_b/kT)}[e^{-(qV_R/kT)} - 1] \qquad \text{Equation 2-3}$$

2.2.3 POWER JUNCTION BARRIER SCHOTTKY (JBS) DIODE

High performance switching converter applications require minimized conduction loss and switching loss of power devices. Reducing the on-resistance of the device can reduce the conduction loss of power Schottky diode, but this means the device has higher doping concentration in drift region which corresponds to lower blocking voltage. Therefore, there is a trade-off between on-resistance and blocking voltage in designing the structure of power Schottky diode. Another way to reduce the conduction loss is to decrease the Schottky barrier height. However, a lower barrier height will cause higher leakage current during reverse bias and lower the maximum operating temperature of Schottky diode.

The junction barrier Schottky diode (JBS) is a Schottky diode structure with a P-N junction embedded into its N-drift region as shown in Figure 2.7. When a positive voltage is applied to the metal contact with respect to the N-type semiconductor and this voltage is not high enough to turn on the embedded P-i-N diode, the forward current just goes through the Schottky part as seen in Figure 2.8.

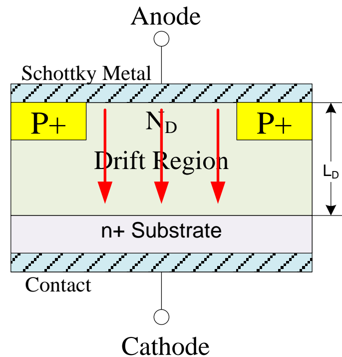


Figure 2.8 Power JBS diode structure

When a negative voltage is applied to the device, because of the existence of P-well under the Schottky barrier, a depletion layer will be formed at the P-N junction that will extend out to the current channel until the channel pinches off. After the channel pinches off, the Schottky barrier is shielded by the potential formed by the depletion layer. The further increase in the applied reverse bias is supported by the depletion layer extending towards the N+ substrate. Once the Schottky barrier is shielded, the leakage current stays almost constant, except for the little increasing current from the space-charge generation of the P-N junction, which means that the leakage current is independent of Schottky barrier height after pinch-off of the depletion layer. Therefore, the JBS diode can have lower leakage current than conventional Schottky diode with the same blocking voltage.

JBS structure is not commonly used in Si-based Schottky diode because the threshold voltage of the embedded P-i-N junction is just 0.7V which can make the diode operate in minority carrier conductivity modulation (bipolar) mode when the P-N junction turns on together with the Schottky barrier junction for a higher positive voltage bias. For SiC Schottky diode with wider bandgap than Si, the threshold voltage of SiC P-N junction is about 3V, which is higher than the Schottky barrier. Therefore, the Schottky barrier junction inside the SiC JBS diode, which turns on during forwards conduction mode, ensures that the P-N junction never turns on during this time.

2.3 SUMMARY

This chapter briefly discusses the operation of power MOSFET and power Schottky diode including the static characteristics and dynamic characteristics. Both of these devices are majority carrier device with no minority carrier modulation during conduction, which means fast switching speed during turn-off transient. Therefore, power MOSFET and power Schottky diode can be used in high performance switching converter applications.

CHAPTER 3

NEW PHYSICS- BASED SIC POWER DMOSFET MODEL

For switching converter applications at less than 200V, the silicon power MOSFET has become the device of choice due to its low on-resistance and fast switching speed. When designed for higher operating voltages, the use of silicon MOSFETs becomes impractical due to the very high drift region resistance. Excellent electrical properties of silicon carbide (SiC) material make it a very attractive semiconductor material for power switching devices with capabilities that are superior to those of devices based on silicon technology. In particular, 4H-SiC MOSFET is one of the most promising candidates for high-speed and low-loss power switching applications.

Recently, SiC MOSFETs have become commercially available from Cree Inc., including single package and bridge module with voltage rating at 1.2kV. Therefore, it is necessary to develop accurate models for SiC power devices so that electrical engineers can evaluate the performance of SiC prototype devices in different applications and guide the switching converter designs.

In this chapter, a new circuit-based SiC DMOSFET model that physically captures the mechanism of current saturation in power SiC DMOSFET is developed in PSpice software based on finite element simulation results. A significant advantage of the model is that a single set of equations describes operation in both the linear and saturation regions and no fitting parameters are needed in the model. The model describes the non-

uniform current distribution in the JFET region that causes current saturation, as shown by the finite element simulations. Finally, the model is validated by comparing simulated results with experimental results both under static and dynamic conditions.

3.1 LITERATURE REVIEW OF SIC MOSFET MODELING

As mentioned above, device models can be divided in two major groups: 1) analytical models based on the finite element solution of drift-diffusion carrier transport in two or three dimensions [14]- [16]; and 2) circuit-oriented models which employ equation-based description of device behavior. While extensive research has been done to develop analytical models for SiC MOSFET [24]- [26], there are very few publications addressing the implementation of circuit-oriented models in simulators such as PSpice [27]- [28].

The physics- based numerical model in [24], which accounts for incomplete ionization and the charging and discharging of interface states, is based on the drift-diffusion equations. This model could reveal the effects of surface phenomena, but it is quite complex and would require long simulation times. Moreover, the model is not suitable for implementation in a circuit simulator due to its complexity. The model presented in [28] is a simple SPICE behavioral model for SiC power DMOSFETs. The model is obtained by introducing specific modifications to the conventional level-1 Si power MOSFET model available in commercial SPICE simulators. The model in [27] is based on the latest version of the power MOSFET model utilized in the Hefner IGBT model [29], where the parameters of both the Si and SiC MOSFETs can be extracted using the IGBT Model Parameter ExtrACtion Tool (IMPACT) software [30]. Both these

models need to extract several fitting factors from device experimental output characteristics to obtain good matching.

3.2 Finite Element Simulation

Typical structure of a power SiC DMOSFET is shown in Figure 3.1. The physical dimensions and doping concentrations are for a 1.2kV device. It is a vertical device with a planar gate, the channel has a 1 μm length and the drift region has a 10 μm thickness. Applying a positive voltage to the gate larger than the threshold voltage, an inversion layer is created on top of the p-base region, forming an n-type conducting channel connecting the source to the JFET region. At the same time, an accumulation layer is formed under the gate oxide at the top of the JFET region, providing current spreading for the electron current flowing from the channel into the JFET region. For small values of drain-source voltage (linear or triode region), the device exhibits an approximately constant on-state resistance, which is determined by channel and drift region resistances. Ultimately, at a higher drain-source bias, the current saturates (saturation region). From standard analysis of power MOSFETs, it is known that there are at least three mechanisms that can contribute to current saturation in power MOSFET: channel pinch-off, carrier velocity saturation in high-electric-field regions, and the so-called parasitic JFET effect, i.e., the fact that the current does not flow uniformly in the JFET region but is constrained to flow in a narrow JFET channel. According to performed finite element simulations, carrier velocity saturation at the interface between the channel and the JFET region is the main reason for current saturation for the SiC DMOSFET structure of Figure 3.1. The JFET effect is also a significant contributing factor. The proposed physics-based circuit-oriented model captures these two effects.

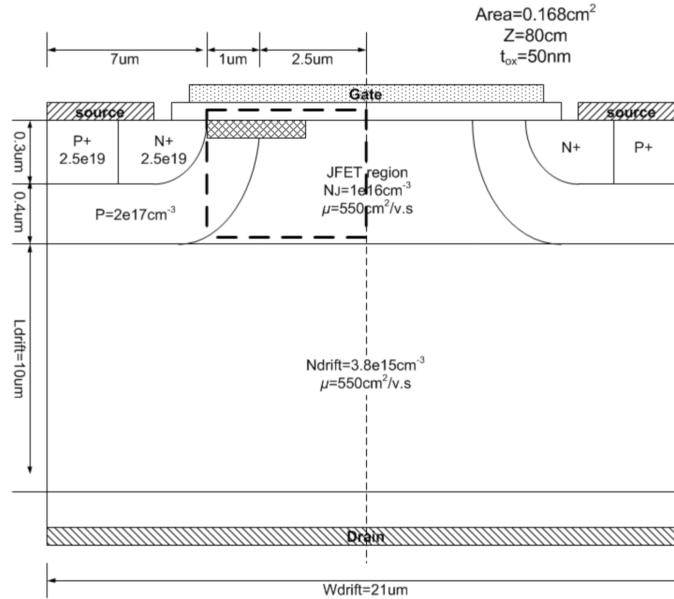


Figure 3.1 Structure of power SiC DMOSFET

Figure 3.2 shows the forward I-V characteristic obtained from finite element simulation of the device structure of Figure 3.1 using Silvaco ATLAS [31]. Gate-source voltage is constant (15V) for all drain-source voltages, ensuring that the device is fully on. Three values of drain-source voltage are considered: $V_{DS}=5V$, $15V$ *and* $30V$. For $V_{DS}=5V$ the device operates in the linear region, and for $V_{DS}=15V$, $30V$ it operates in the saturation region.

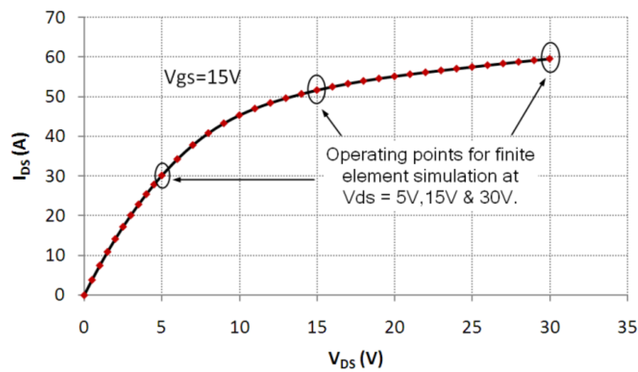
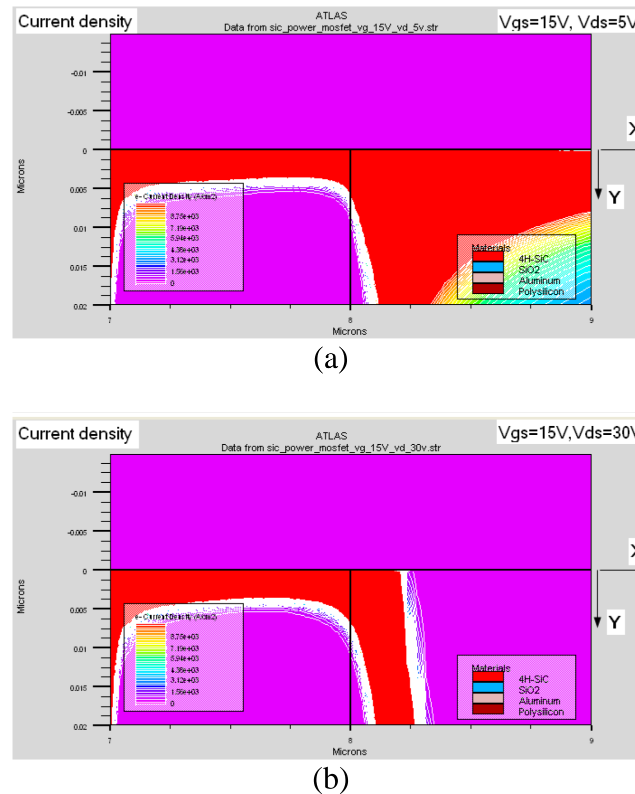


Figure 3.2 I-V characteristic of DMOSFET for $V_{GS}=15V$ obtained from finite element simulation.

Figure 3.3 (a-b) shows the current density distribution in a rectangular region encompassing the channel and the top portion of the JFET region for $V_{DS}=5V$ and for

V_{DS}=30V. This region extends for 2 μm in the x-direction and for 0.035 μm in the y-direction and is identified by the small hatched rectangular region in Figure 3.1. Notice that the thickness and the shape of the channel are very similar for the two drain-source voltages and no significant pinch-off is observed even when the device is in deep saturation (V_{DS}=30V). This shows that channel pinch-off is not a significant contributor to current saturation. The biggest difference between Figure 3.3 (a) and Figure 3.3 (b) is that for operation in the saturation region a depletion region forms in the JFET region and the current flows along a narrow vertical path adjacent to the p-base.



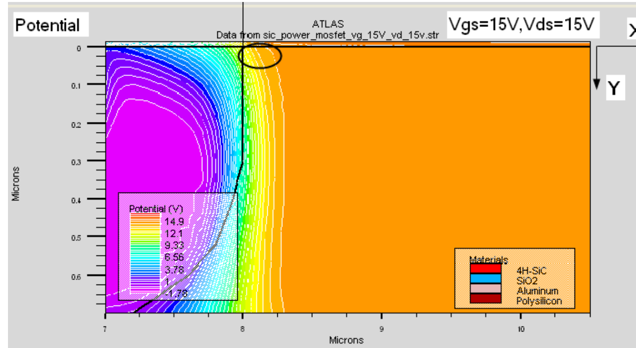
(a)

(b)

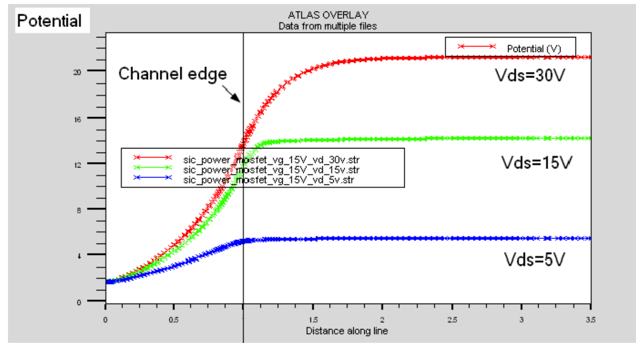
Figure 3.3 Finite element simulation results. Current density two-dimensional distribution along the channel for operation in the linear region, V_{DS}=5V (a) and in the saturation region, V_{DS}=30V (b).
Gate-source bias is V_{GS}=15V.

Figure 3.4 (a) shows two-dimensional finite element simulation results for the electric potential in the upper part of the SiC DMOSFET (rectangular dashed region in Figure 3.1). Figure 3.4 (b) shows the electric potential curve on a cutline along the channel (cutline: X=7 μm-10.5 μm, Y=1nm) for the three values of drain-source voltage of Figure 3.2. Figure 3.5 (a) shows the two-dimensional current transport and Figure 3.5 (b) shows the lateral (x-axis) electric field component along the same cutline.

From these simulation results one can draw some conclusions on saturation mechanism in a typical power SiC DMOSFET. Pinch-off of the channel was not observed under any drain-source bias: even at $V_{DS}=30V$ the channel retains its approximately rectangular shape and does not display channel pinch-off condition. Additional confirmation of this can be obtained by looking at Figure 3.4 (b), which shows that the potential drop in the channel does not change much (from 12V to 14V approximately) as V_{DS} increases from 15V to 30V. This shows that most of the voltage drop across the device in saturation does not occur in the channel, but somewhere else (in the JFET region). As the drain-source voltage increases, the lateral electric field shown in Figure 3.5 (b) becomes quite large at the end of the channel, where it reaches its peak value E_k when current goes to saturation regime. Detailed investigation of carrier transport in the channel region as predicted by the finite element simulations reveals that carrier velocity saturation is responsible for the large electric field E_k and consequently is the main contributor causing current saturation in the device.



(a)

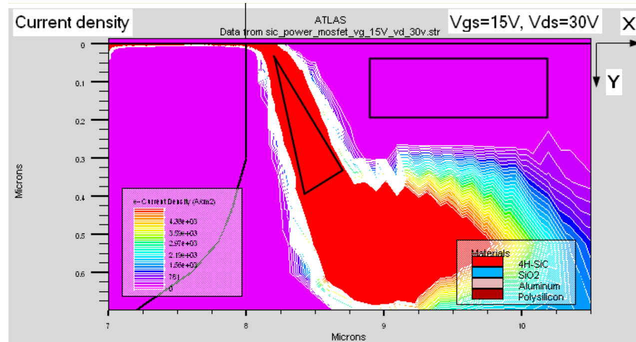


(b)

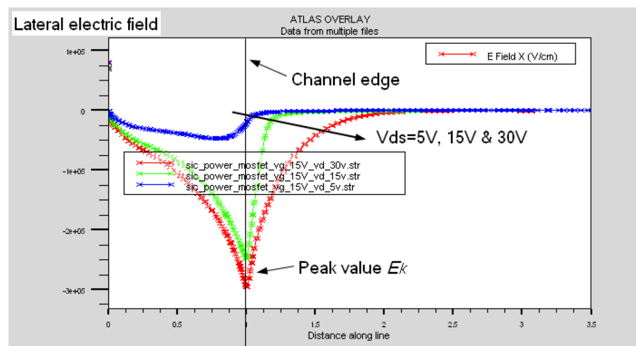
Figure 3.4 Finite element simulation results. (a) Electric potential two-dimensional distribution for $V_{GS}=15V$, $V_{DS}=15V$ and (b) electric potential along cutline for three drain-source voltages.

Traditionally, it is assumed that an accumulation layer is always formed under the gate oxide in the JFET region and further analysis of current transport in power MOSFET is based on this assumption. This accumulation layer helps spreading the electron current coming from the channel uniformly across the undepleted portion of the JFET region. As a result, the JFET region can be represented as a rectangular piece of semiconductor material whose width is modulated by change of depletion region width of p-base/n-JFET junction, with electron current flowing vertically from the JFET accumulation layer under the gate to the drift region. However, the finite element simulation of Figure 3.5 (a) tells a different story: the current distribution in the JFET region is highly non-uniform and current crowding occurs in the region adjacent to the p-base/n-JFET junction depletion

layer (see triangular region in Figure 3.5 (a) for $V_{DS} = 30V$). Notice that the accumulation layer disappears in the JFET region and is replaced by a depletion region (rectangular region in Figure 3.5 (a)). Notice also that the electric potential increases sharply at the end of the channel with drain voltage increasing. A significant portion of the voltage drop is localized in the current spreading region across the depleted portion of the JFET region (see circled region in Figure 3.4 (a)). So one can divide the JFET region into two parts: one is the current spreading region across the depleted portion, with electron current spreading out laterally; the other is the triangular region mentioned before, with electron current flowing vertically and non-uniformly. Based on this idea, a new circuit-based model is developed, which physically represents the mechanism of current saturation in power SiC DMOSFET.



(a)



(b)

Figure 3.5 Finite element simulation results. (a) Current density two-dimensional distribution and (b) lateral electric field along cutline.

The physical treatment of current spreading in DMOSFET proposed by Baliga considers accumulation and JFET region as two individual regions [12]. Resistance of accumulation region is determined by gate voltage only, while resistance of JFET region is a function of drain-source voltage only. However, based on the performed finite-element investigation, the resistance of the accumulation region is a strong function of both V_{GS} and V_{DS}, which is not considered in classical solutions for current transport of power DMOSFET. Moreover, the resistance of JFET region is not only determined by depletion width of p-base/JFET junction, but also and more predominantly by reduction of current conduction in the central part of JFET region caused by formation of a depletion region between adjacent p-base regions (rectangular region in Figure 3.5 (a)). For large values of gate-source voltage, such as the $V_{GS}=15V$ case, the JFET current channeling effect is significant only for large values of drain-source voltage, such as the $V_{DS}=30V$ case of Figure 3.5 (a), which are not of great practical interest, since power dissipation is exceedingly large. However, for smaller values of gate-source voltage, this effect becomes significant at correspondingly lower values of drain-source voltage. For this reason it is important to capture this effect in order to have an accurate device model.

3.3 Novel Model with Non-uniform Current Distribution in the JFET Region

The simple standard model of a power MOSFET is a piecewise model using different equations to describe operation in the linear region and saturation region. The two equivalent circuits are shown in Figure 3.6. For simplicity device capacitances and the gate terminal are not shown. When channel voltage $V_{CH} < V_{CH,SAT} = V_{GS}-V_T$ (V_T is saturation voltage), the MOSFET operates in the linear region and drain current I_D is

dependent on both gate- source voltage V_{GS} and channel voltage V_{CH}. When $V_{CH} \geq V_{CH,SAT}$, the MOSFET operates in the saturation region and I_D is a function of V_{GS} only and does not depend on V_{CH}. So there are two different equations for current I_D in the standard model, one for the linear region and another one for the saturation region.

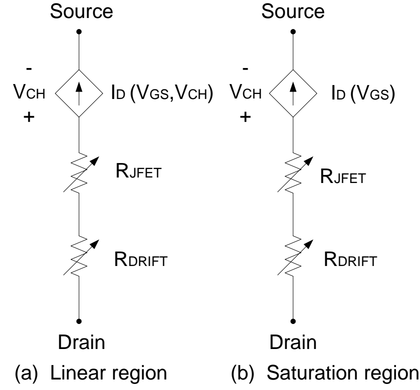


Figure 3.6 Standard power MOSFET static model structure.

For linear region, the drain current I_D is given by

$$I_D = \frac{\mu_{CH0} C_{OX} Z}{2L_{CH}} \left[2(V_{GS} - V_T)V_{CH} - V_{CH}^2 \right] \quad \text{Equation 3-1}$$

For saturation region, the drain current I_D is

$$I_{DSAT} = \frac{\mu_{CH0} C_{OX} Z}{2L_{CH}} V_{CH,SAT}^2 \quad \text{Equation 3-2}$$

The nonlinear resistors R_{JFET} and R_{DRIFT} are given by

$$R_{JFET} = \frac{L_{JFET}}{2 \cdot q \cdot \mu_{JFET} \cdot N_{JFET} \cdot Z \cdot (a - W_{JFET})} \quad \text{Equation 3-3}$$

$$R_{DRIFT} = \frac{L_{DRIFT} - W_{DS}}{2 \cdot q \cdot \mu_{n-drift} \cdot N_{DRIFT} \cdot Z \cdot W_{DRIFT}} \quad \text{Equation 3-4}$$

The structure of the new proposed model is shown in Figure 3.7. It consists of voltage-controlled current source I_D, voltage source V_{J2}, JFET region resistance net R_{J_net},

drift resistance R_{DRIFT}, and capacitances C_{GS}, C_{DS} and nonlinear capacitance C_{GD}. The novelty of this model is in how the JFET region is modeled by V_{J2} and R_{J_net}.

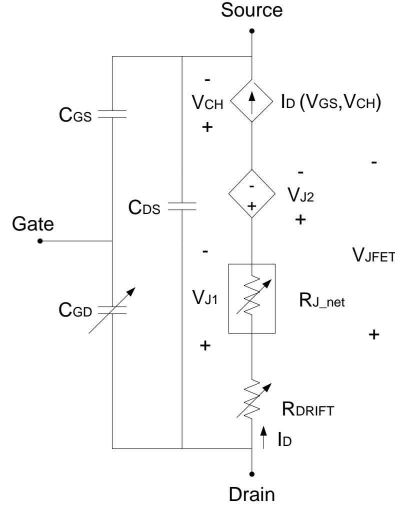


Figure 3.7 Proposed SiC DMOSFET model structure.

Taking into account that SiC MOSFET current saturation is due to a large voltage drop in JFET region and not to channel pinch- off, it is possible to use only one equation to describe the channel region forward I-V characteristic. This is the equation corresponding to linear region of operation in the standard model of Figure 3.6:

$$I_D = \frac{\mu_{CH} C_{OX} Z}{2L_{CH}} \left[2(V_{GS} - V_T)V_{CH} - V_{CH}^2 \right] \qquad \text{Equation 3-5}$$

Thus, channel region is represented by a voltage-controlled current source and channel voltage V_{CH} can be determined by subtracting voltage drop in JFET and drift region from total voltage applied to the device:

$$V_{CH} = V_{DS} - V_{JFET} - I_D R_{DRIFT} \qquad \text{Equation 3-6}$$

with

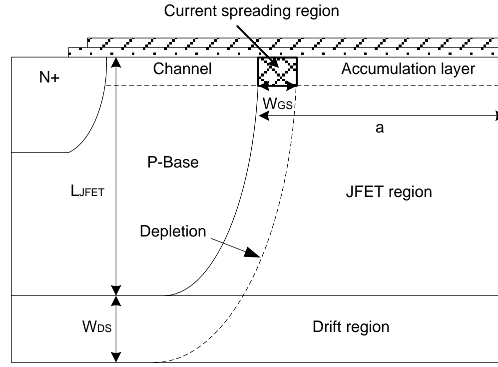
$$R_{DRIFT} = \frac{L_{DRIFT} - W_{DS}}{2 \cdot q \cdot \mu_{n-drift} \cdot N_{DRIFT} \cdot Z \cdot W_{DRIFT}} \quad \text{Equation 3-7}$$

$$W_{DS} = \sqrt{\frac{2\varepsilon_{sic}}{q \cdot N_{DRIFT}}(V_{bi} + V_{CH} + V_{JFET})} \quad \text{Equation 3-8}$$

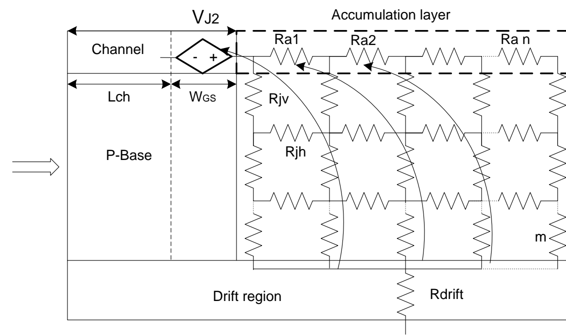
where V_{JFET} is the voltage drop in JFET region.

3.3.1 JFET REGION MODELING

The proposed method to capture the current saturation in the discussed DMOSFET is to represent JFET region as two parts: a voltage source and a matrix of resistors as in Figure 3.7. The specific structure is shown in Figure 3.8. Voltage source V_{J2} represents the voltage drop in the current spreading region and the resistor network allows for a non-uniform current distribution in the JFET region. This approach takes into account JFET region voltage drop in both lateral and vertical directions, therefore capturing the two-dimensional nature of current spreading in this region. The top row of resistors represents the accumulation layer while the remaining matrix resistors represent the main body of JFET region. The main feature of this approach is that values of the resistors in the accumulation layer are function of both V_{GS} and V_{DS}. Let us consider a resistor R_{ai} in the top row. Due to the voltage drop on the resistors to its left, the voltage V_{Gai} between the gate and the resistor node i is decreased, causing reduction of accumulation layer thickness. As a result, it is $R_{a1} < \ldots < R_{ai} < \ldots < R_{an}$. This effect contributes to current crowding at the depletion layer edge in the JFET region.



(a)



(b)

Figure 3.8 Model description of JFET region. (a) Specific structure of channel and JFET region and (b) Circuit representation of JFET region.

To model the voltage drop in vertical direction inside the JFET region, a resistor matrix with n-columns and m-rows is used. First top row of resistors R_{ai} represents accumulation region and can be expressed as:

$$R_{ai} = \frac{L_R}{Z\mu_A C_{OX}(V_{GS} - V_T - V_i)} \qquad \text{Equation 3-9}$$

where μ_A is accumulation layer mobility, V_i is voltage at the node of corresponding i resistor and L_R is the distance between adjacent nodes:

$$L_R = \frac{a - W_{GS}}{n} \qquad \text{Equation 3-10}$$

$$W_{GS} = \sqrt{\frac{2\varepsilon_{sic}}{q \cdot N_{JFET}}(V_{bi} + V_{CH} + V_{J2})}$$ Equation 3-11

When V_i is smaller than $(V_{GS}\text{-}V_T)$, R_i has a finite positive value, representing the accumulation layer resistance. With V_i increasing, the voltage drop $(V_{GS} - V_T - V_i)$ goes to zero and R_i tends to infinity. From a physical point of view, a depletion region forms, replacing the rightmost portion of the accumulation layer (rectangular region in Figure 3.5 (a)).

JFET region resistive net is represented by horizontal and vertical resistors (see Figure 3.8 (b)):

$$R_{jh} = \frac{L_R m}{q\mu_{JFET} N_{JFET} Z L_{JFET}}$$ Equation 3-12

$$R_{jv} = \frac{L_{JFET}}{q\mu_{JFET} N_{JFET} Z L_R m}$$ Equation 3-13

The voltage source V_{J2} represents the voltage drop in the current spreading region. It is a critical element in the proposed model, because when the current saturates, this portion supports most of the increased applied voltage. From the finite element simulation of Figure 3.5 (b) it can be seen that the electric field reaches its peak value E_k at the end of the channel and decreases approximately linearly to 0 along W_{GS}. Therefore, the amplitude of the voltage source V_{J2} can be obtained by integrating the triangular electric field in the current spreading region, which has a peak value E_k and a length W_{GS}.

$$V_{J2} = \frac{1}{2} E_k W_{GS}$$ Equation 3-14

The peak electric field E_k in the current spreading region can be calculated as follows. The drain current equation at the end of the channel is given by

$I_D = C_{OX} \cdot (V_{GS} - V_T - V_{CH}) \cdot Z \cdot v_1$, where v_1 is the electron carrier velocity, which is given by $v_1 = \mu_{CH}(E_k) \cdot E_k$. Combining these two equations, one obtains Equation 3-15.

$$I_D = C_{OX}(V_{GS} - V_T - V_{CH})Z \cdot \mu_{CH}(E_k) \cdot E_k \qquad \text{Equation 3-15}$$

This implicit equation can be used to calculate peak electric field E_k in the presence of carrier velocity saturation by using Equation 3-16 to express the field-dependent carrier mobility at the end of the channel.

$$\mu_{CH}(E_k) = \mu_{CH0} \cdot \left[1 + \left(\frac{\mu_{CH0} E_k}{v_{sat}}\right)^{\beta}\right]^{-1/\beta} \qquad \text{Equation 3-16}$$

where μ_{CH0} is the low-field mobility in the inversion layer and v_{sat} is the carrier saturation velocity. Because the peak electric field E_k increases with increasing drain-source voltage, for low voltage V_{J2} is so small that it does not affect the linear region characteristic. But for high voltage, V_{J2} supports most of the applied voltage because of the strong electric field due to carrier velocity saturation. As a result, the channel voltage V_{CH} reaches a constant maximum value and the device current saturates. As a result, Equation 3-5 describing channel region conduction is valid under all operating conditions with the non-saturated mobility, because the channel region always operates in the linear operating regime with low electric field. This fact has been verified through finite element simulations.

3.3.2 Nonlinear Capacitance Model

In order to model the dynamic performances of power SiC DMOSFET, nonlinear gate- drain capacitance C_{GD} is introduced in the proposed model shown in Figure 3.7. This capacitance is both current and voltage dependent and is comprised of the gate oxide

capacitance $C_{OX}Aa_i$ in series with the depletion layer capacitance under gate oxide $C_{dep} = \varepsilon_{SiC} Aa_i / W'$ [32]. Nonlinear capacitance C_{GD} is given below.

$$C_{GD} = \frac{C_{OX} Aa_i C_{dep}}{C_{OX} Aa_i + C_{dep}} = \frac{C_{OX} Aa_i}{1 + C_{OX} \frac{W'}{\varepsilon_{SiC}}} \quad \text{Equation 3-17}$$

where W' is the length of the depletion region under the gate oxide, a_i is the ratio of intercell area to total die area, C_{OX} is the oxide capacitance per unit area, and A is the total die area.

$$W' = W_{DS} - W_{JFET} - a \quad \text{Equation 3-18}$$

and

$$W_{JFET} = \sqrt{\frac{2\varepsilon_{sic} V_{GS}}{q \cdot N_{JFET}}} \quad \text{Equation 3-19}$$

where W_{JFET} is the depletion layer length of the depletion region under the gate, which only begins to grow when V_{DS}=V_{GS}, and a is half the width of channel region. Figure 3.9 shows the comparison of non-linear capacitances obtained from experiment, Atlas finite element simulation and Pspice simulation. The figure shows that they match with each other reasonably well. Atlas simulation matches the experiment a little better than Pspice simulation at high voltage. However, there are some discrepancies between the simulation and experiment at low voltage which may affect the prediction of switching behavior during the device turn-on and turn-off transients.

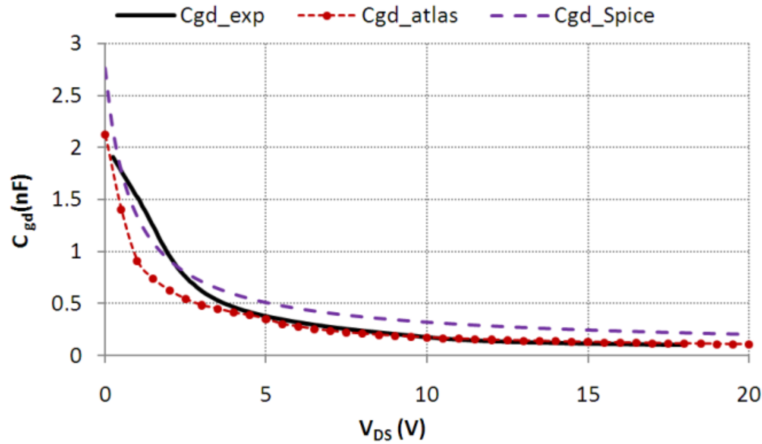


Figure 3.9 Comparison of C_{GD}-V characteristics of experiment, finite-element simulation and PSpice simulation.

3.4 Model Validation

The model is implemented in the circuit simulator PSpice and is validated by comparison with Atlas finite element simulations and experimental measurements. A high power SiC DMOSFET from CREE Inc., rated at 1200V 20A, is used for experimental validation. The device inner construction details are not available from the manufacturer. On the basis of experimental parameter extraction and literature published by CREE [33], the geometrical and doping characteristics of Figure 3.1 have been derived. These characteristics are used both for the finite element simulation model and for the PSpice model. A full set of experimental measurements is performed in order to assist model validation, including: static I-V characteristics, C-V characteristics and dynamic characterization under resistive switching conditions.

3.4.1 Proposed Model vs Atlas Model

Figure 3.10 shows comparison of C-V characteristics between experimental results and finite-element simulated results at $V_{GS}=0V$ and at measurement frequency f

$=1MHz$. The finite element simulation results are accurate for large drain-source voltages, but show discrepancies for lower voltages. Figure 3.11 shows comparison of forward characteristics for the proposed new model, standard model and Atlas model of SiC DMOSFET. Static characteristics obtained using the standard model of Figure 3.6 are included for comparison. Figure 3.11 (a) shows a good match between the proposed model and the Atlas model static characteristics, whereas the standard model predicts significantly larger currents for large gate-source voltages when drain-source voltage V_{DS} is low. For completeness, Figure 3.11 (b) shows the forward characteristic up to $V_{DS}=30V$, showing that for large gate-source voltages ($V_{GS}=15V$) the standard model forward characteristic eventually saturates, but it is quite inaccurate in the range $V_{DS}=3$-$25V$.

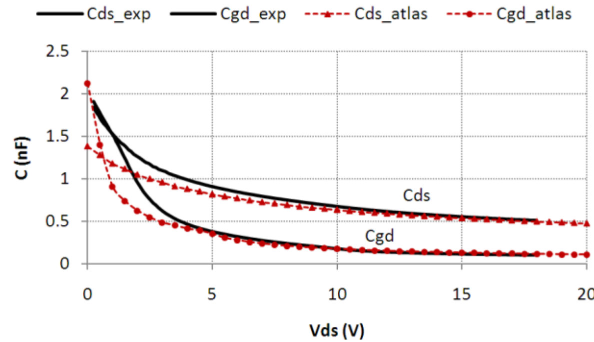


Figure 3.10 Comparison of C-V characteristics obtained experimentally and from finite-element simulation.

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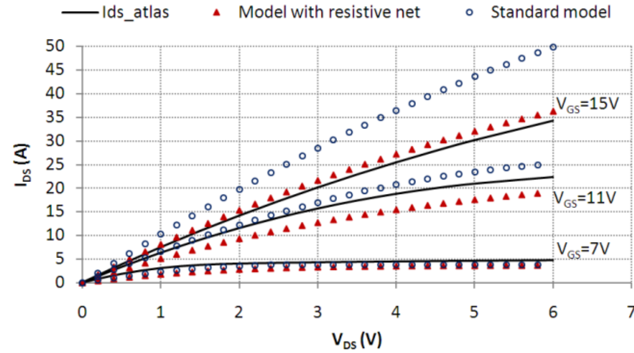
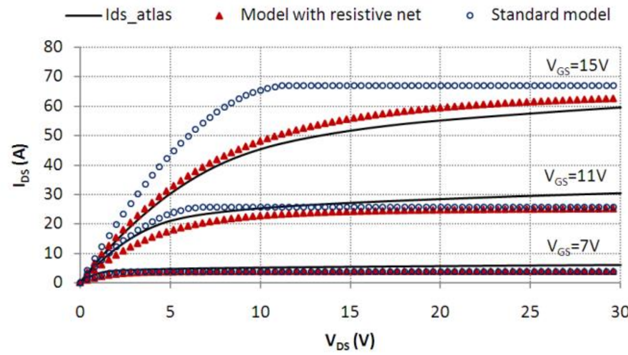


(a)



(b)

Figure 3.11 Comparisons of proposed model, Atlas model and standard model forward characteristics of SiC DMOSFET for $V_{DS} = 0 - 7V$ (a) and for $V_{DS} = 0 - 30V$ (b).

3.4.2 PROPOSED MODEL VS EXPERIMENT

Static forward characteristics were measured using a Tektronix 371A power curve tracer for four values of gate-source voltage: 7V, 11V, 15V, 19V. The experimental static characteristic of the device are compared with model predictions in Figure 3.12. Static characteristics obtained using the standard model of Fig. 6 are included for comparison. Figure 3.13 shows simulated result of the current in the individual resistors of the accumulation layer as a function of drain-source voltage (shown for a four- column resistive net). As it can be seen, when drain-source voltage increases, current tends to flow through resistors that are closer to the channel. This current crowding effect contributes to device current saturation. Figure 3.14 shows the channel voltage V_{CH} and

current spreading region voltage V_{J2} in JFET region at $V_{GS}= 7V$. The forward characteristic for $V_{GS}= 7V$ shown in Figure 3.12 exhibits current saturation as voltage V_{DS} increases. Looking at Figure 3.14 one can see that, as drain-source voltage increases, channel voltage tends to saturate while V_{J2} supports most of the voltage drop, and, as a result, device current saturates.

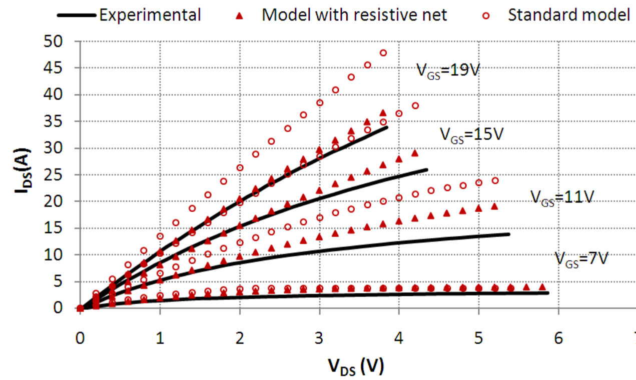


Figure 3.12 Comparison of experimental and simulated forward characteristic of SiC DMOSFET.

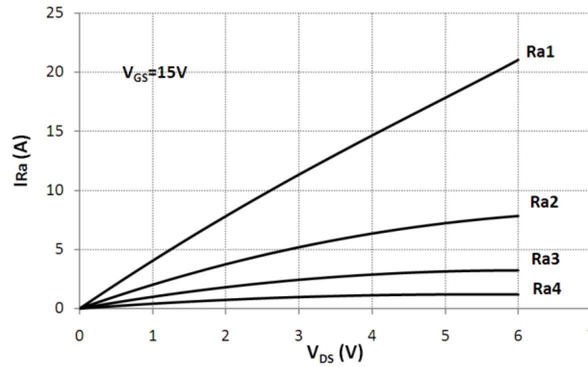


Figure 3.13 Model current in accumulation resistors of SiC DMOSFET.

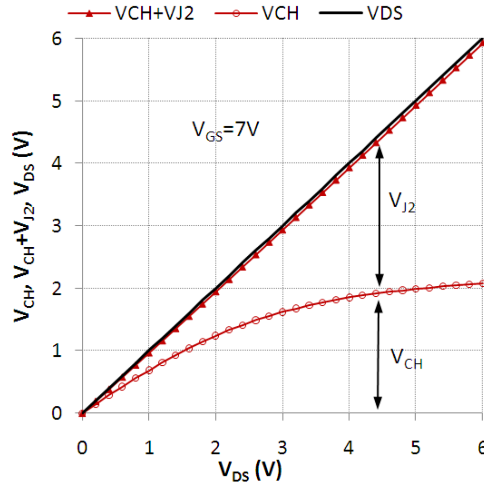


Figure 3.14 Channel voltage V_{CH}, voltage source V_{J2} in JFET region and drain to source voltage V_{DS} at $V_{GS}=7V$.

A printed circuit board (PCB) testbed was built to perform resistive switching experiments on the SiC DMOSFET. Figure 3.15 shows the corresponding resistive switching circuit used in simulation, which includes parasitic inductors, L_s, L_d and L_g [34]. Inductor L_d represents the switching loop inductance. Inductor L_s is the MOSFET source-leg parasitic inductance and provides a feedback path from MOSFET drain current to gate-source voltage during transitions. Inductor L_g is the gate circuit loop inductance. Comparison between experimental and simulation results are shown in Figure 3.16 for resistive turn-on and in Figure 3.17 for resistive turn-off. The simulation results are in good agreement, even if there are some differences, especially in the waveforms of gate-source voltage V_{gs}. A possible explanation for the discrepancy is that the nonlinear capacitance description in the model has some limitation for small values of drain-source voltages as can be seen in Figure 3.10. Further improvements of this capacitance model are left as future work. Figure 3.18 and Figure 3.19 show the turn-on and turn-off waveforms of nonlinear capacitance C_{GD} under resistive switching and the constant value of oxide capacitance c_{OX}. These figures show how capacitance C_{GD} varies

as a function of drain-source voltage, reaching a maximum value of c_{OX} when drain-source voltage goes to zero.

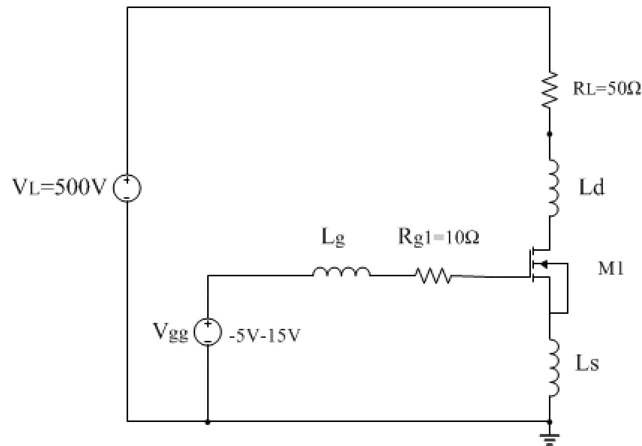
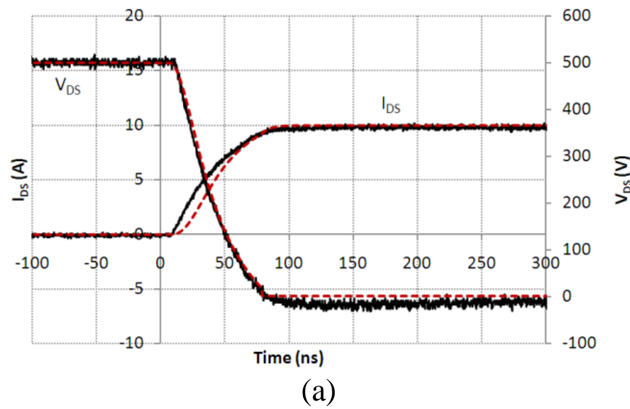


Figure 3.15 Equivalent circuit used for resistive switching simulation using the proposed model.



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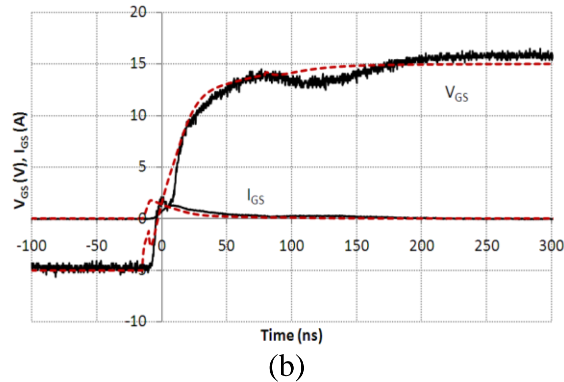
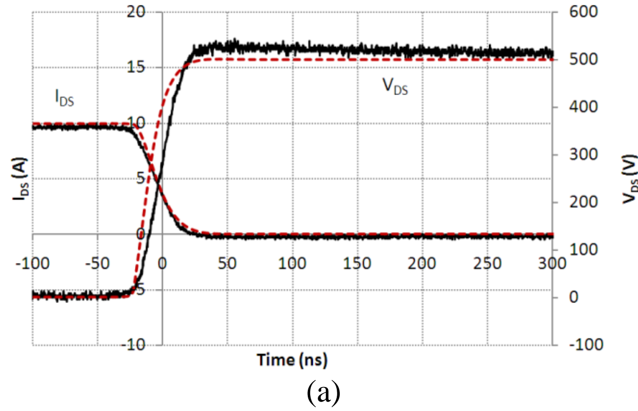
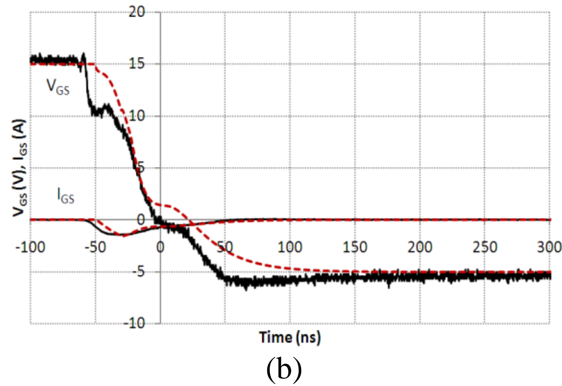


(b)

Figure 3.16 SiC DMOSFET simulated (dashed) and experimental (solid) turn-on waveforms of resistive switching, (a) Comparison of V_{DS} and I_{DS} and (b) Comparison of V_{GS} and I_{GS}.



(a)



(b)

Figure 3.17 SiC DMOSFET simulated (dashed) and experimental (solid) turn-off waveforms of resistive switching, (a) Comparison of V_{DS} and I_{DS} and (b) Comparison of V_{GS} and I_{GS}.

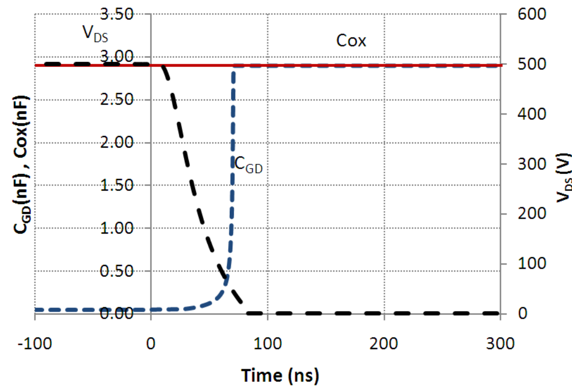


Figure 3.18 Time evolution during turn-on of the instantaneous values of nonlinear capacitance C_{GD} and of the oxide capacitance c_{OX} under resistive switching.

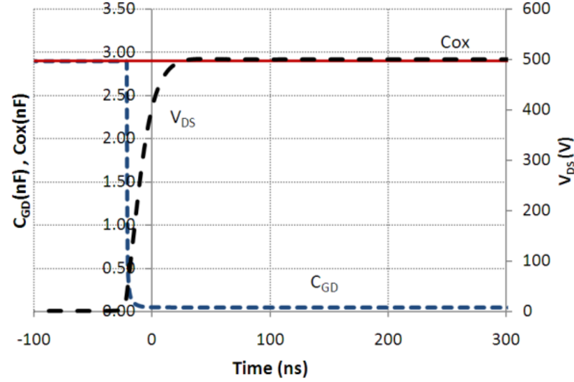


Figure 3.19 Time evolution during turn-off of the instantaneous values of nonlinear capacitance C_{GD} and of the oxide capacitance c_{OX} under resistive switching.

3.5 DISCUSSION

The proposed model provides a more physical description of the saturation phenomenon in SiC MOSFETs and is motivated by the presented finite-element simulation results, which show that current saturation is due to carrier velocity saturation at the interface between the channel and the JFET region and to non-uniform current flow in the JFET region as shown in Figure 3.4 and Figure 3.5. A significant advantage of the proposed model with respect to the conventional MOSFET model is that a single set of equations is valid both in the linear and the saturation region. The conventional piecewise model shown in Figure 3.6 is unsatisfactory from the point of view of physically describing the current saturation phenomenon while the proposed model in this dissertation provides a more physical description of MOSFET operation.

The experimental validation shows that the model is capable of accurately describing device operation under both static and dynamic conditions. The actual geometrical dimensions and doping profile for the CREE DMOSFET are not exactly known, as is frequently the case in practice. However, the fact that the static characteristics of the PSpice model match those of the finite element model indicates that

the proposed model captures the physical behavior of the device as described by the finite element simulation.

However, there are some discrepancies of C-V curves between experiments, finite element simulation and PSpice simulation as shown in Figure 3.9. Better modeling the depletion layer shape in JFET region and drift region may improve the non-linear capacitance model because at low blocking voltage levels the depletion layer edge exhibits two-dimensional characteristic related to gate region geometry and varying doping concentration.

Figure 3.14 shows the distribution of voltage across different parts of the proposed model including the channel voltage V_{CH}, voltage source V_{J2} in JFET region and drain-to-source voltage V_{DS} at gate-to-source voltage V_{GS}=7V. One can see from the figure that most of the voltage drop is supported by the voltage source V_{J2} at JFET region as drain-to-source voltage increases. The JFET region corresponds to the current spreading region in the finite element simulation results shown in Figure 3.4. One also can see that the resistance network in JFET region supports a comparatively small voltage in the whole voltage range, which means that this region has a limited effect on current saturation and most of the voltage drop occurs in the current spreading region.

Figure 3.16 and Figure 3.17 show the resistive switching validation of the proposed model. The figures show that the simulation results are in good agreements with experimental results for both turn-on switching transient and turn-off switching transient, which can also capture the Miller effects during switching time.

In conclusion, this new DMOSFET model provides a more physics-based description of the current saturation phenomenon in state-of-the-art SiC DMOSFETs and can be implemented in circuit based simulation such as PSpice.

3.6 SUMMARY

In this chapter, a novel physics-based SiC DMOSFET model that physically captures the mechanism of current saturation in power SiC DMOSFET is developed in PSpice software based on finite element simulation results. The finite element simulation shows that the current saturation is due to carrier velocity saturation at the interface between the channel and the JFET region. Compared to the simple MOSFET model, the proposed model provides a more physical description of the saturation phenomenon. The newly proposed model represents the non-uniform current distribution in the JFET region using a non-linear voltage source and a resistance network. Finally, the model is validated by comparing simulated results with experimental results under both static and dynamic conditions.

CHAPTER 4

PHYSICS-BASED POWER SIC SCHOTTKY DIODE MODEL

The material properties of silicon limit the fabrication of practical Si unipolar diodes (Schottky diodes) to a range up to 150V, with relatively high on-resistance and leakage current. On the other hand, SiC Schottky diodes can reach a much higher breakdown voltage because of SiC excellent electrical properties such as wider bandgap, much higher critical breakdown electric field and higher thermal conductivity compared with Si-based device. SiC Schottky diodes are now commercially available from several companies such as Cree, GeneSiC and Infineon.

In this chapter, a detailed parameter extraction procedure for a simple physics-based power SiC Schottky diode model is presented. The detailed parameter extraction procedure introduced here does not require any knowledge of device fabrication. The only measurements required for the parameter extraction are a simple static I-V characterization and C-V measurement. This model is used to describe the characteristics of several SiC power diodes from different companies. Model results will be presented for:

1) A 600V, 50A Schottky diode from GeneSiC Inc.;
2) A 1200V, 3A Schottky diode from GeneSiC Inc.;
3) A 1200V, 7A Schottky diode from GeneSiC Inc.;
4) A 1200V, 20A Schottky diode from Cree Inc.

4.1 LITERATURE REVIEW OF SIC SCHOTTKY DIODE MODELING

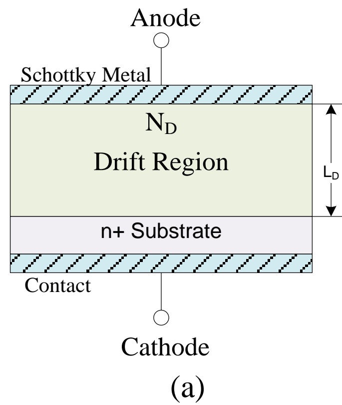
Presently, SiC Schottky diodes are commercially available up to 1200 V/50 A or 600 V/20 A. Accurate device models are required to evaluate the performance of SiC Schottky diodes in different applications and guide system design. So far several models have been developed for SiC Schottky diodes, most of them based either on device physics or on experimental behavior. Physics-based models provide more accuracy but at a cost: they usually require a number of device parameters to be used in the model, sometimes the model itself is complicated, and may have convergence issues or require a long computation time. Behavioral models require less time for simulation but a large number of experiments are needed for parameter extraction and sometimes the parameter extraction process is complicated and requires the use of dedicated parameter extraction software, such as DIode Model Parameter extrACtion Tools (DIMPACT) [13].

The behavior- based (or behavioral) model in [8], which accounts for temperature dependent factor, is based on a piecewise linear (PWL) model of a diode, which includes a dc voltage drop V_D and a series resistor R_D in the equivalent circuit. This model is simple and has a reasonably good match with experiments. But it cannot accurately reproduce the ringing in the circuit, which is very important in high performance applications. The models presented in [10] [13][35][36] are based on thermionic-emission mechanism. Some of them include analytical temperature dependence and some of them include reverse characteristics. In these models a large number of parameters are needed and the equations are fairly complicated. The conclusion from this literature review is that it is necessary to find a model for SiC

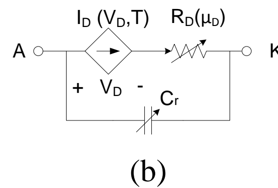
Schottky power diodes amenable to system- level modeling. This work is to address this need.

4.2 SIMPLE PHYSICS- BASED SCHOTTKY DIODE MODEL

The structure of the power SiC Schottky diode with the metal – semiconductor Schottky contact is shown in Figure 4.1 (a). The simple physics- based Schottky diode model (shown in Figure 4.1 (b)) is developed by using thermionic emission theory, which describes the dominant carrier transport mechanism in Schottky power rectifiers [12]. The model is comprised of three elements: a voltage controlled current source I_D, a mobility dependent (and therefore temperature dependent) drift region resistance R_D and a nonlinear capacitance C_r.



(a)



(b)

Figure 4.1 (a) Structure of power Schottky diode (b) Simple physics- based Schottky diode model.

In a SiC Schottky diode, the thermionic emission process dominates in the current transport across the metal semiconductor contact. Under forward bias condition, the current across the Schottky barrier is given by

$$I_D = AA^*T^2 e^{-(q\varphi_b/kT)}\left[e^{(qV_D/nkT)} - 1\right] = I_S[e^{(qV_D/nkT)} - 1] \qquad \text{Equation 4-1}$$

where I_S is the saturation current, A is the active area of the diode, A^* is Richardson's constant, φ_b is the barrier height between the metal and N-type semiconductor, n is the ideality factor, T is the absolute temperature, q is the electron charge, k is Boltzmann's constant and V_D is voltage drop across the Schottky barrier. The saturation current is $I_S = AA^*T^2 e^{-(q\varphi_b/kT)}$.

The series drift region resistance R_D is given by

$$R_D = \frac{L_D}{q\mu_D(T)N_D \times A} \qquad \text{Equation 4-2}$$

where N_D is the drift region doping concentration, L_D is the thickness of drift region and $\mu_D(T)$ is the temperature dependent electron mobility. Mobility can be expressed as shown in [37].

$$\mu_D(T) = \mu_{300}(\frac{T}{300})^{-x} \qquad \text{Equation 4-3}$$

where μ_{300} is the carrier mobility at room temperature $T=300K$.

Since Schottky diode is a majority carrier device, there is no minority carrier injection in the drift region. The depletion layer capacitance determines the diode switching behavior. When a reverse bias voltage V_R is applied to the Schottky diode, a depletion region forms under the metal semiconductor interface and the depletion layer thickness W_r can be calculated as shown in [12].

$$W_r = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_D}(V_R + V_{bi})} \approx \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_D}(V_R + \varphi_b)} \quad \text{Equation 4-4}$$

Because all the applied bias voltage is supported in the semiconductor, this depletion width can be used to calculate the nonlinear capacitance C_r of the Schottky diode as

$$C_r = \frac{\varepsilon_0\varepsilon_r A}{W_r} = A \times \sqrt{\frac{qN_D\varepsilon_0\varepsilon_r}{2(V_R + \varphi_b)}} \quad \text{Equation 4-5}$$

The complete list of the needed parameters for the considered device model is shown in Table I.

Table 4-1 Schottky diode model parameters

N_D	Drift region doping concentration.
L_D	Thickness of drift region.
A	Active area of the diode.
φ_b	Barrier height between the metal and N-type semiconductor.
x	Temperature coefficient of carrier mobility.
A^*	Richardson's constant.
μ_{300}	Carrier mobility at room temperature T=300K.
n	Ideality factor.

4.3 Parameter Extraction Procedure

The parameter extraction approach discussed in this paper is based on the assumption that the carrier mobility at room temperature μ_{300} is known.

4.3.1 Drift Region Parameter N_D, L_D, and A

To extract the drift region parameters N_D, L_D and A, the static I-V characterization and C-V measurements of the Schottky diode are needed. The I-V measurements in this work are performed using a Tektronix 371A power curve tracer. The value of series

resistance R_D can be obtained directly from the slope of the I-V characteristics at high currents shown in Figure 4.2 for the 600V, 20A GeneSiC Schottky diode.

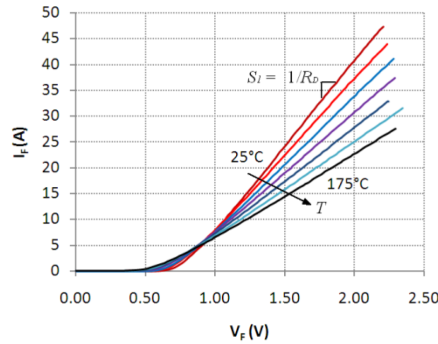
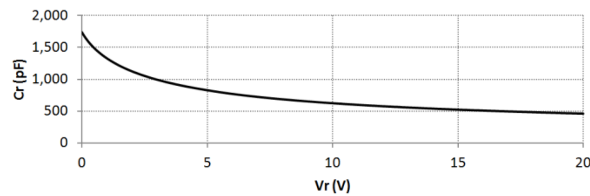


Figure 4.2 I-V characteristics from 25 ℃ to 175 °for 600V, 50A GeneSiC Schottky diode.

Therefore, the slope S_1 of the I-V characteristics at a certain temperature can be calculated from Equation 4-6.

$$S_1 = \frac{1}{R_D} = \frac{q\mu_D N_D \cdot A}{L_D} \quad \text{Equation 4-6}$$



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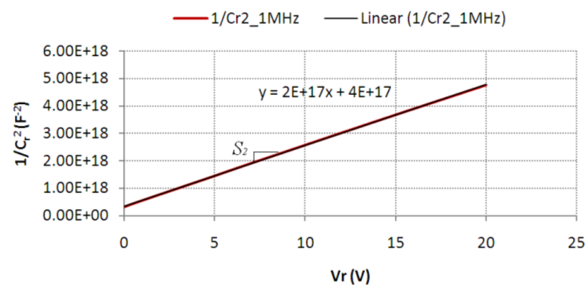


(b)

Figure 4.3 C-V measurement of 600V, 50A GeneSiC Schottky diode.
(a) C_r versus V_r and (b) $1/C_r^2$ versus V_r.

Besides the I-V characteristics of the Schottky diode, C-V measurement is needed for the extraction procedure. A Keithley CV analyzer 590 is used to perform

measurements in this work. Figure 4.3 shows C-V characteristics of 600V, 50A GeneSiC Schottky diode at measurement frequency $f = 1MHz$.

Rewriting Equation 4-5 one obtains

$$\frac{1}{C_r^2} = \frac{2}{A^2 q N_D \varepsilon_0 \varepsilon_r}(V_R + V_{bi})$$ Equation 4-7

So the slope S_2 of $1/C_r^2$ versus V_R is given by equation

$$S_2 = \frac{2}{A^2 q N_D \varepsilon_0 \varepsilon_r}$$ Equation 4-8

Assuming a triangular electric field distribution at breakdown and using Equation 4-4, one can calculate the device thickness based on the breakdown voltage V_B as

$$L_D = \sqrt{\frac{2\varepsilon_0 \varepsilon_r V_B}{q N_D}}$$ Equation 4-9

Substituting Equation 4-9 into Equation 4-6 and squaring both sides, one gets

$$S_1^2 = \frac{q^3 N_D^3 \mu_D^2 A^2}{2\varepsilon_0 \varepsilon_r V_B}$$ Equation 4-10

Rewriting Equation 4-8 to get an expression for A^2, then substituting it into Equation 4-10, an expression for carrier concentration as a function of applied voltage and slopes S_1 and S_2 can be obtained.

$$N_D = \frac{S_1 \varepsilon_0 \varepsilon_r \sqrt{V_B S_2}}{q \mu_D}$$ Equation 4-11

Then substituting the value for N_D found using Equation 4-11 back into Equation 4-8, the active area A can be calculated as below.

$$A = \sqrt{\frac{2}{S_2 q N_D \varepsilon_0 \varepsilon_r}}$$ Equation 4-12

For a specific device with known breakdown voltage, by capturing I-V characteristics and C-V measurements of the Schottky diode at room temperature, the drift region parameters N_D, L_D and A can be extracted using Equation 4-11, Equation 4-9 and Equation 4-12 respectively. Breakdown voltage can either be estimated from the data sheets or measured with a power curve tracer.

4.3.2 BARRIER HEIGHT Φ_B AND TEMPERATURE COEFFICIENT X

The barrier height φ_b, is defined as the potential difference between the metal Fermi level and the majority carrier band edge of the semiconductor. Barrier height of Schottky diodes depends on the fabrication process and semiconductor material. Any surface contamination introduced during the diode fabrication process can affect the barrier height of the diodes. The barrier height φ_b can be extracted using the following steps.

Rewrite Equation 4-1 for $V >> kT/q$ as below:

$$\ln(I) = \ln(I_s) + \frac{qV}{nkT}$$ Equation 4-13

From the plot of $ln(I)$ vs V, the intercept of the current axis at $V = 0$ gives the saturation current I_s. From Equation 4.1 the barrier height φ_b can be expressed as:

$$\varphi_b = \frac{kT}{q}\ln(\frac{AA^*T^2}{I_s})$$ Equation 4-14

and can be calculated from the saturation current I_S.

Based on the assumption that the carrier mobility at room temperature μ_{300} is known, the temperature coefficient of carrier mobility x can be calculated by using the value of mobility extracted from static characteristics at an elevated temperature T_1 as shown in [37]:

$$x = -\frac{\ln(\mu(T_1)/\mu_{300})}{\ln(T_1/300)}$$ Equation 4-15

For 4H-SiC, the theoretical value of Richardson's constant A^* is 146 A•cm-2•K-2 [10][12]. For simplicity, the ideality factor n is assumed to be unity.

In conclusion, the parameter extraction procedure consists of the following steps:

1) Assume that the Richardson's constant is $A^* = 146$ A cm^{-2} K^{-2}, the ideality factor is $n=1$, and the carrier mobility at room temperature μ_{300} has a known value.
2) Obtain slope S_1 from the I-V characteristics and slope S_2 from C-V measurement (see Figure 4.2 and Figure 4.3 (b)).
3) Calculate the drift region parameters N_D, L_D and A by using Equation 4-11, Equation 4-9 and Equation 4-12 respectively.
4) Extract barrier height φ_b from the I-V characteristics by using Equation 4-14.
5) Calculate the corresponding carrier mobility $\mu(T_1)$ at one elevated temperature T_1 and extract the temperature coefficient x of carrier mobility by using Equation 4-15.

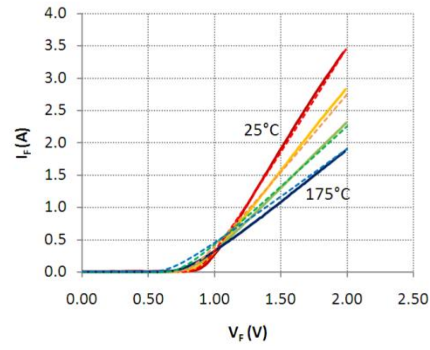
4.4 Validation of Parameter Extraction Procedure and Diode Model

The parameter extraction procedure is applied to several SiC Schottky diodes: a 600V, 50A, a 1200V, 3A and a 1200V, 7A Schottky diodes from GeneSiC Inc.; and a 1200V, 20A Schottky diode from Cree Inc. Table II gives the extracted parameters of the four devices with the assumption that electron mobility is 550 cm^2/V•s. The temperature coefficient x is extracted based on the corresponding mobility at 25 ^{o} C (room

temperature) and that at 75 °C. After all Schottky diode parameters are extracted, the model defined by Equation 4-1, Equation 4-2 and Equation 4-5, can be validated. Figure 4.4 shows the comparison of simulated (dashed lines) I-V characteristics of SiC Schottky diode based on extracted parameters with experimental (solid lines) static characteristics measured at temperature from 25 ℃ to 175 ℃. The temperature step is $\Delta T = 50$ ℃. The simulated I-V curves are in fairly good agreement with experimental results for the four devices. Figure 4.5 shows the comparison of simulated (dashed lines) with experimental C-V characteristics of SiC Schottky diode measured at frequency $f = 1MHz$. Figure 4.6 shows comparison of the corresponding curves of $1/C_r^2$ versus reverse voltage V_r. Figure 4.5 and Figure 4.6 demonstrate that the simulated C-V curves have fairly good agreement with the experimental results, which is very important for switching performance, even if some discrepancy can be seen at low voltages.

Table 4-2 Extracted parameters

Devices	N_D (cm^{-3})	L_D (μm)	A (cm^2)	φ_b (V)	x
GeneSiC 1200V, 3A	3.53E15	19.1	0.0203	1.25	1.9
GeneSiC 1200V, 7A	3.27E15	19.9	0.0472	1.25	1.8
Cree 1200V, 20A	4.85E15	16.3	0.1000	1.22	1.6
GeneSiC 600V, 50A	3.55E15	13.5	0.1433	1.06	1.7



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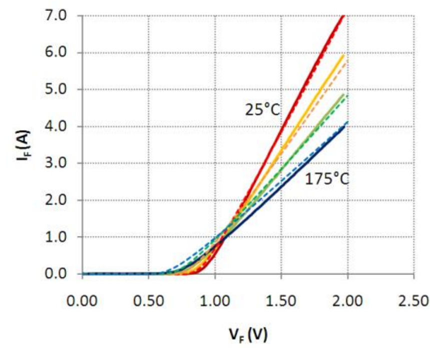

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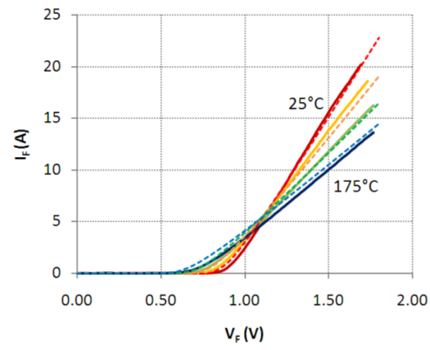

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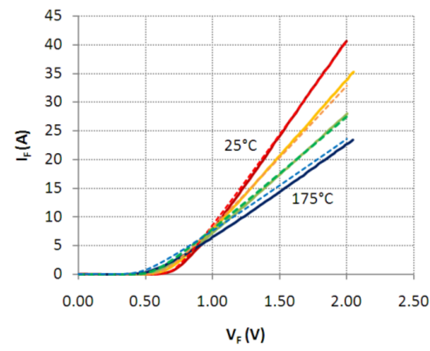

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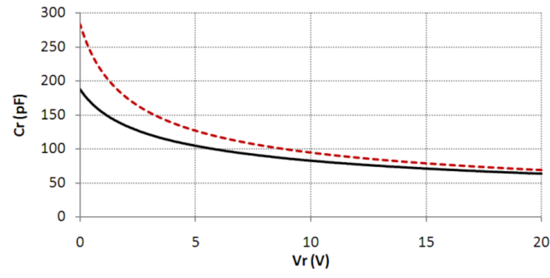
Figure 4.4 Comparison of simulated (dashed lines) with experimental (solid lines) static characteristics of SiC Schottky diodes measured at temperature from 25 ℃ to 175 ℃. (a) GeneSiC 1200V, 3A. (b) GeneSiC 1200, 7A. (c) Cree 1200V, 20A. (d) GeneSiC 600V, 50A.



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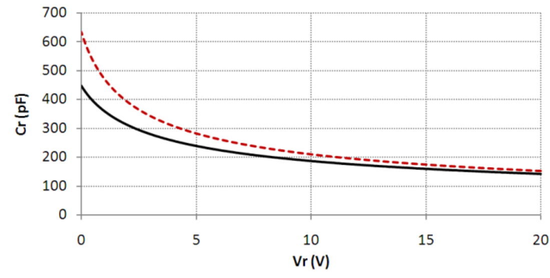

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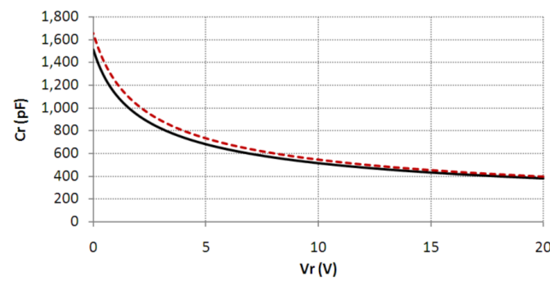

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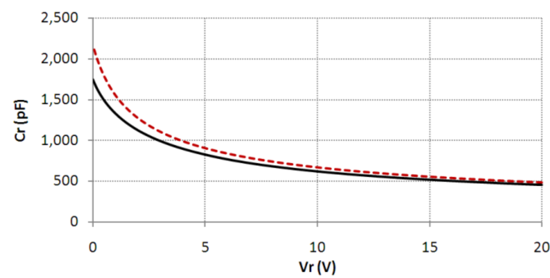

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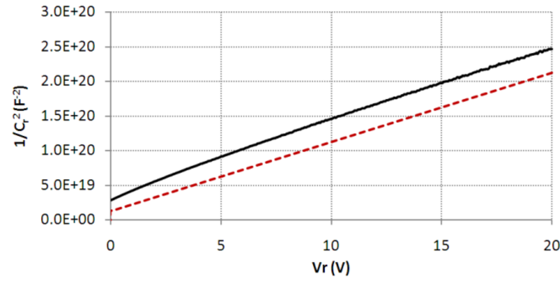
Figure 4.5 Comparison of simulated (dashed lines) with experimental (solid lines) C-V characteristics of SiC Schottky diodes measured at frequency $f = 1MHz$.
(a) GeneSiC 1200V, 3A. (b) GeneSiC 1200, 7A. (c) Cree 1200V, 20A. (d) GeneSiC 600V, 50A.



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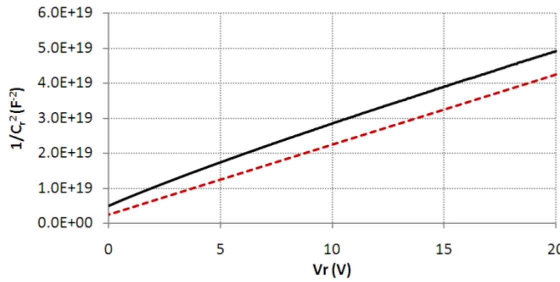

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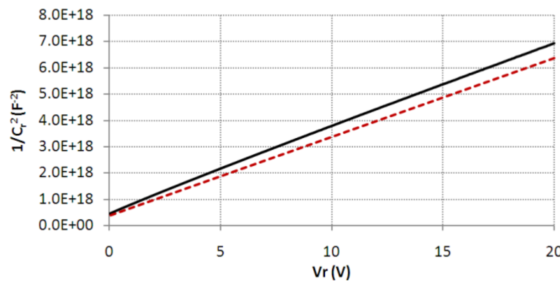

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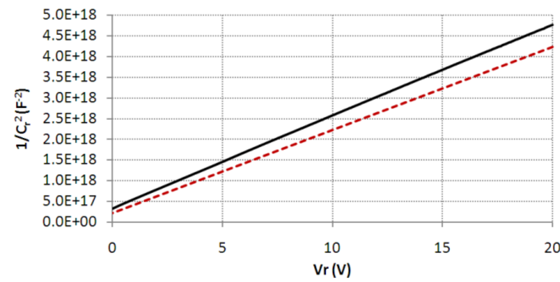

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Figure 4.6 Corresponding comparisons of simulated (dashed lines) with experimental (solid lines) $1/C^2$-V characteristics of SiC Schottky diodes measured at frequency f = *1MHz*. (a) GeneSiC 1200V, 3A. (b) GeneSiC 1200, 7A. (c) Cree 1200V, 20A. (d) GeneSiC 600V, 50A.

For dynamic characteristic validation, a double pulse testbed was built to perform inductive switching experiments on these four SiC Schottky diodes. Figure 4.7 shows the corresponding inductive circuit used in simulation, which includes various parasitic

inductances. The gate-to-source switching loop and drain-to-source switching loop parasitic inductances of the PCB layout are extracted by the 3-D inductance extraction program FastHenry, which is a program for magneto- quasistatic analysis of three-dimensional packages and interconnects [38]. The simulation uses the MOSFET model proposed in CHAPTER 3, which accounts for non-uniform current distribution in the JFET region by using a nonlinear voltage source and a resistance network. V_{DR} is the voltage across the Schottky diode, and I_{SCH} denotes the current through the diode, which are both shown in the figure. Comparisons between experimental and simulated results are shown in Figure 4.8 for inductive switching of the device GeneSiC 1200V, 3A. Figure 4.9, Figure 4.10 and Figure 4.11 are the inductive switching comparisons of the devices GeneSiC 1200, 7A, Cree 1200V, 20A and GeneSiC 600V, 50A respectively.

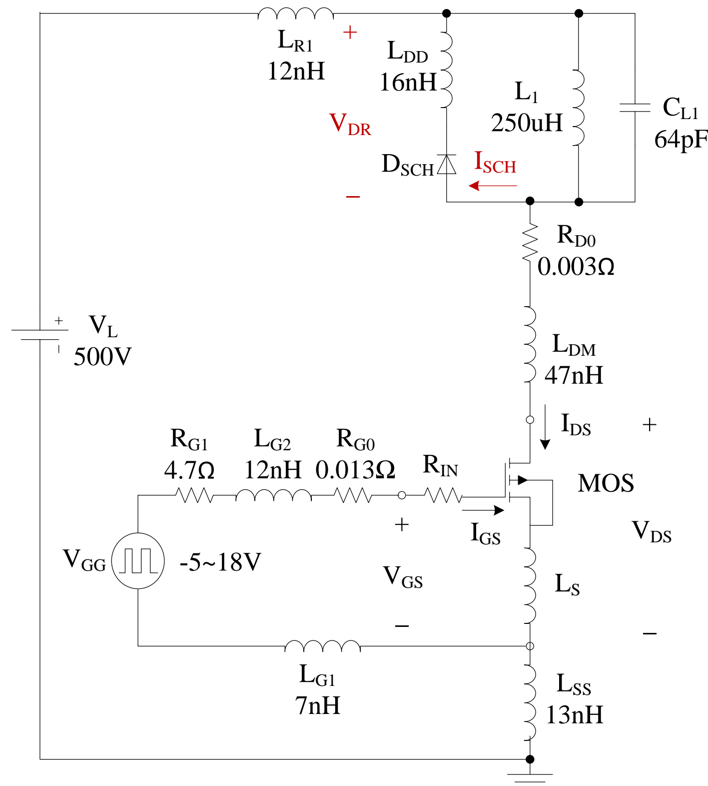
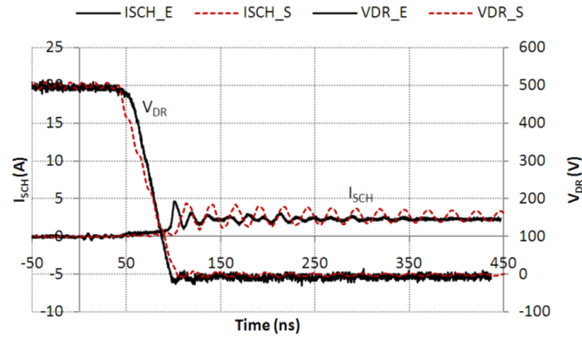


Figure 4.7 Equivalent circuit used for inductive switching simulation.



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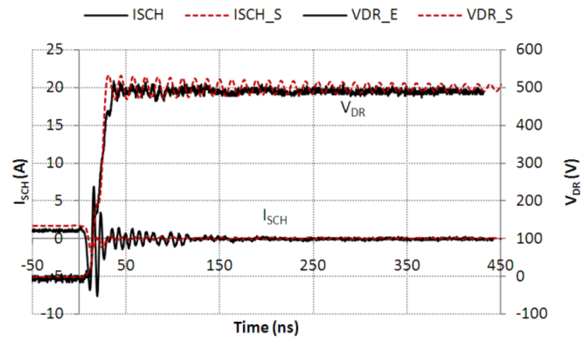

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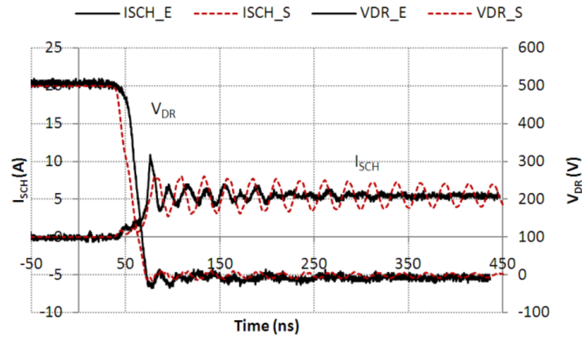
Figure 4.8 Simulated (dashed) and experimental (solid) waveforms of inductive switching for Schottky diode GeneSiC 1200V, 3A. (a) Turn- on; (b) Turn- off.



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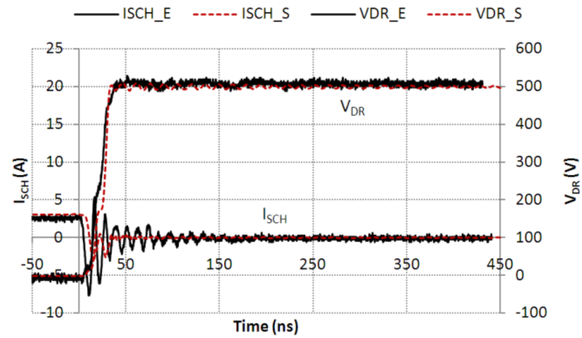

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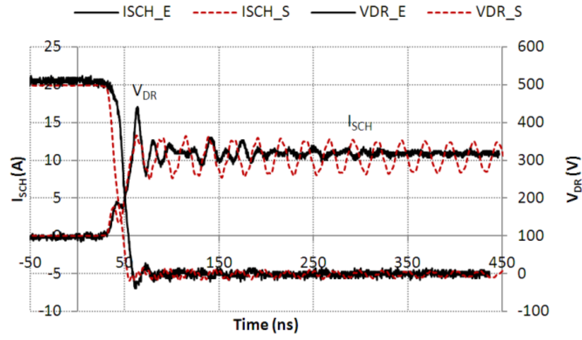
Figure 4.9 Simulated (dashed) and experimental (solid) waveforms of inductive switching for Schottky diode GeneSiC 1200V, 7A. (a) Turn- on; (b) Turn- off.



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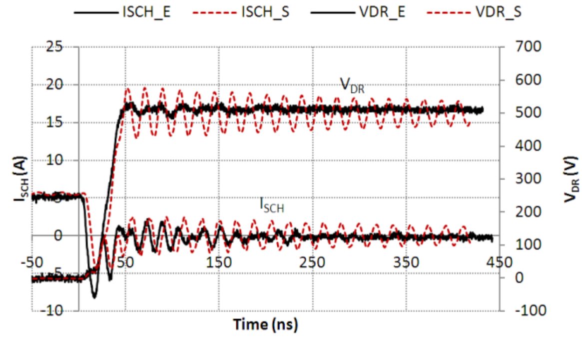

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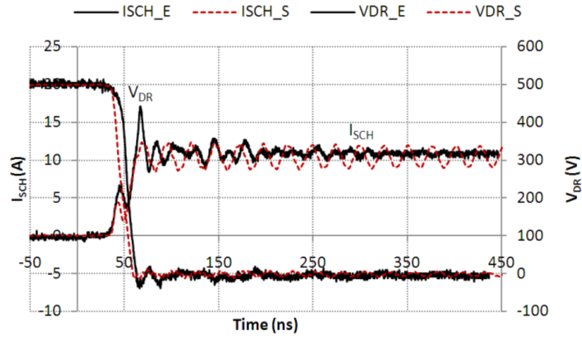
Figure 4.10 Simulated (dashed) and experimental (solid) waveforms of inductive switching for Schottky diode Cree 1200V, 20A. (a) Turn- on; (b) Turn- off.



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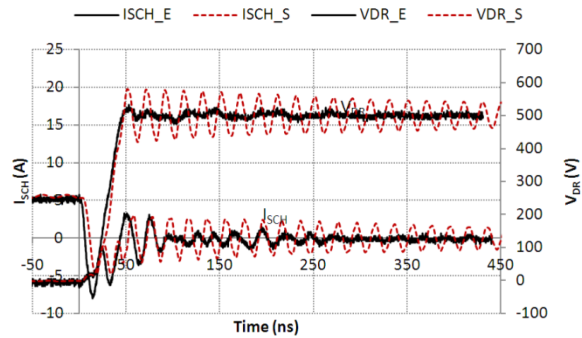

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Figure 4.11 Simulated (dashed) and experimental (solid) waveforms of inductive switching for Schottky diode GeneSiC 600V, 50A. (a) Turn- on; (b) Turn- off.

4.5 DISCUSSION

The proposed Schottky diode model is a simple physics-based model whose parameters are extracted using a combination of I-V characteristics and C-V measurements, without the need for device manufacturing information.

The parameter extraction procedure proposed in this dissertation is based on the assumption that the carrier mobility at room temperature μ_{300} in drift region is known. The critical point of the procedure is to obtain the slope S_1 from the I-V characteristics and S_2 from C-V measurement, so that the drift region parameters N_D, L_D and A can be extracted, which are very important for the accuracy of the proposed Schottky diode model under both static and dynamic conditions.

Figure 4.4 shows pretty good agreement between simulated and experimental results of I-V static characteristics for several devices at different temperatures at high current. At low current some discrepancies appear in the figure. These discrepancies could be reduced by using a non-unity ideality factor n extracted from the I-V characteristics, whereas the ideality factor n of the model is chosen to be unity for simplicity in this dissertation.

Figure 4.5 and Figure 4.6 show the comparisons between simulated and experimental results of C-V measurements of four different SiC Schottky diodes. Some discrepancies appear at low voltage in Figure 4.5. One reason for this is, over-estimating the active area of the Schottky diodes by using the proposed parameter extraction procedure based on a pure Schottky diode structure while some tested Schottky diode are actually Junction Barrier Schottky (JBS) structure. Another reason may be that the quantity used in the extraction procedure is the slope of the curves $1/C_r^2$ versus V_r, and

not the absolute capacitance values. Some non-linear features appear in Figure 4.6 at low voltage. To optimize the Schottky diode model, one should take into account the non-linear feature at low voltage in the parameter extraction procedure. This is left as future work.

The inductive switching validation in Figure 4.8, Figure 4.9, Figure 4.10 and Figure 4.11 for the four different Schottky diodes shows good agreements in the turn-on and turn-off transient. The simulation results in Figure 4.10 and Figure 4.11 show more ringing compared with the experimental results. This ringing may be caused by the nonlinear capacitance models in the MOSFET model or the extracted parasitic inductances. The measurement method could also affect the switching behavior of the devices.

In conclusion, the proposed Schottky diode model can be generally used for devices with different voltage and current ratings and is capable of accurately describing device operation under static and dynamic conditions.

4.6 SUMMARY

The proposed parameter extraction procedure includes the extraction of doping concentration, active area and thickness of drift region, which are needed for the proposed physics-based power Schottky diode model. The main advantage is that this procedure does not require any knowledge of device fabrication. The only measurements required for the parameter extraction are a simple static I-V characterization and C-V measurements. Validity of the approach is verified by comparison of simulated and experimental results at temperatures from 25 ℃ to 175 ℃ for four different devices from two different manufacturers. Inductive switching validation also shows that the model has

a fairly good match with experiments. This means that the model presented in this dissertation can be used for devices with widely different voltage and current ratings.

CHAPTER 5

PARASITICS MODELING FOR

FAST SWITCHING BEHAVIOR OF SIC DEVICES

5.1 INTRODUCTION

Rapid developments have occurred in the field of power electronics due to the development of power semiconductor devices and novel circuit topologies. The demands of high power and high efficiency power electronic switching converters require the power semiconductor devices to have very low conduction loss and switching loss. Very low conduction loss means that the devices must have very small on-state voltage and on-resistance. Low switching loss means that the devices switch very fast to minimize the lossy transition time, when both large voltages and currents are present in the semiconductor devices.

Thanks to recent progress of SiC technology, SiC MOSFETs and Schottky diodes are now commercially available from various manufacturers, such as Cree, GeneSiC and Infineon. SiC devices hold the promise of faster switching speed compared to Si devices, which can lead to superior converter performance, because the converter can operate at higher switching frequencies with acceptable switching losses, so that passive filter size is reduced. However, the ultimate achievable switching speed is determined not only by internal semiconductor device physics, but also by circuit

parasitic elements. Therefore, in order to accurately predict switching losses and actual switching waveforms, including overshoot and ringing, accurate models are needed not only for the semiconductor devices, but also for the circuit parasitics. Given the higher switching speed of SiC devices, the relative importance of circuit parasitics is increased. The objective of this chapter is to develop a procedure to accurately model circuit parasitics and to demonstrate experimentally that the parasitic models so obtained, together with previously developed semiconductor device models, allow accurate prediction of converter switching waveforms.

Parasitic impedances like parasitic inductances and parasitic capacitances exist everywhere in a switching converter, including the power semiconductor devices, ICs, sensors, power capacitors, power inductors, PCB layouts and connectors, etc. [17] [39] [40]. Specifically, parasitic inductances appear to be the main concern in high-performance switching converters. Frequently parasitic inductances are distributed inductances that account for the presence of physical loops. However, in this work lumped equivalent inductances are considered. Parasitic inductance stores energy when current flows through it. When the device is turning off, the stored energy in the parasitic inductance needs to be discharged and a voltage spike rated at *Ldi/dt* appears across the parasitic inductor. If the parasitic inductor is part of the converter inductive switching loop, the *Ldi/dt* voltage spice is added to the drain-to-source voltage of power devices, which increases their voltage stress. The effects of parasitic inductances get worse at higher frequencies, and limit the maximum operating switching frequency of power devices. To optimize the performance of switching converter, parasitic inductances should be minimized as much as possible.

Many publications have proposed methods for extracting parasitic parameters in switching converters [17][39][40][41]. They can be divided in two different groups. The first one is the measurement-based method, such as the time domain reflectometry (TDR) based measurement [41] and the method based on impedance measurement [40], which are complicated and time consuming or just suitable for simple circuit geometries. The second one is the simulation-based method, which extracts the parasitic parameters using finite element analysis like Maxwell Field Solver 3D or partial element equivalent circuit (PEEC) methods like Maxwell Q3D Extractor and 3-D inductance extraction program FastHenry, which is used in this dissertation.

In this chapter, the parasitic inductances for a double pulse test-bench based on SiC devices were extracted and analyzed using 3-D inductance extraction program FastHenry. The double pulse test-bench was built to capture the resistive and inductive switching behavior of the SiC devices. In order to capture the parasitic ringing in the fast switching transient, the gate-to-source switching loop and drain-to-source switching loop parasitic inductances of the PCB layout are extracted by the 3-D inductance extraction program FastHenry. Then the extracted parasitic inductances are combined together with SiC MOSFET model in CHAPTER 3 and SiC Schottky diode model in CHAPTER 4 in Pspice to predict the device switching waveforms. Finally, simulation results are compared with the experimental results to verify the effectiveness of the parasitics modeling method.

5.2 Double Pulse Test-bench Experimental Setup

A printed circuit board (PCB) double pulse test-bench was built to perform the resistive and inductive switching experiments on the SiC devices including MOSFET and

Schottky diode. There are two different high current paths in the PCB layout: one for resistive switching and one for inductive switching. Figure 5.1 shows the PCB layout of the double pulse test-bench and identifies the gate-to-source switching loop (yellow solid line), resistive drain-to-source switching loop (black dashed line) and inductive drain-to-source switching loop (red solid line).

Figure 5.2 is the experimental setup of inductive switching for the double pulse testing. The test-bench includes a test socket for the MOSFET, a test socket for Schottky diode, gate driver, capacitor bank, freewheeling diode, and a Pearson coil for current measurement. Nine polypropylene film capacitors are used to provide a low inductance voltage source for the test-bench. The MOSFET is SiC MOSFET CMF10120D from CREE Inc. rated at 1200V/24A. The free-wheeling diode is a SiC Schottky diode C4D20120A rated at 1200V/20A from CREE Inc. An IXD_609 chip from IXYS Corporation is used as the MOSFET gate driver with 9A maximum drive current. The gate resistor R_{G1} is 4.7Ω. The gate voltage switches from -5V to 18V. A Pearson coil is used to measure the drain current I_{DS}.

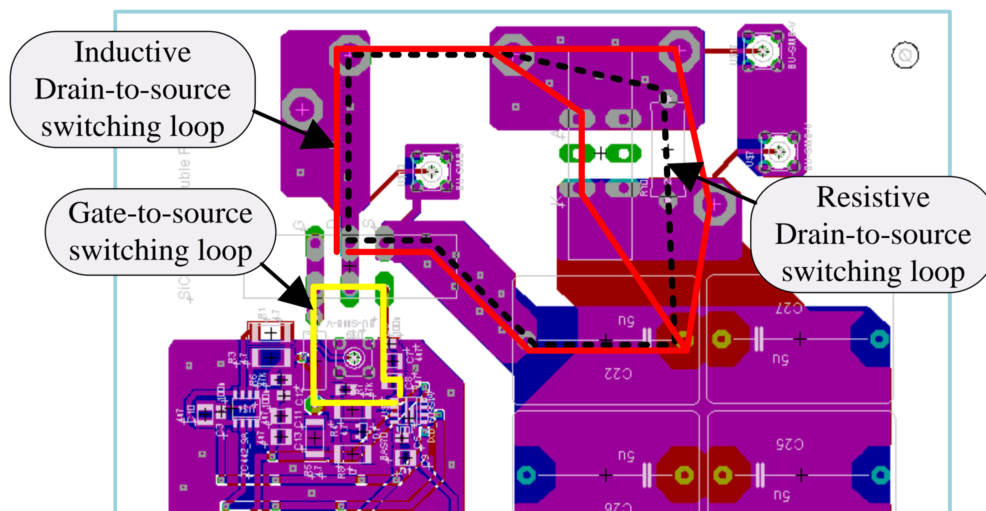


Figure 5.1 Part of the PCB layout of the double pulse test-bench.

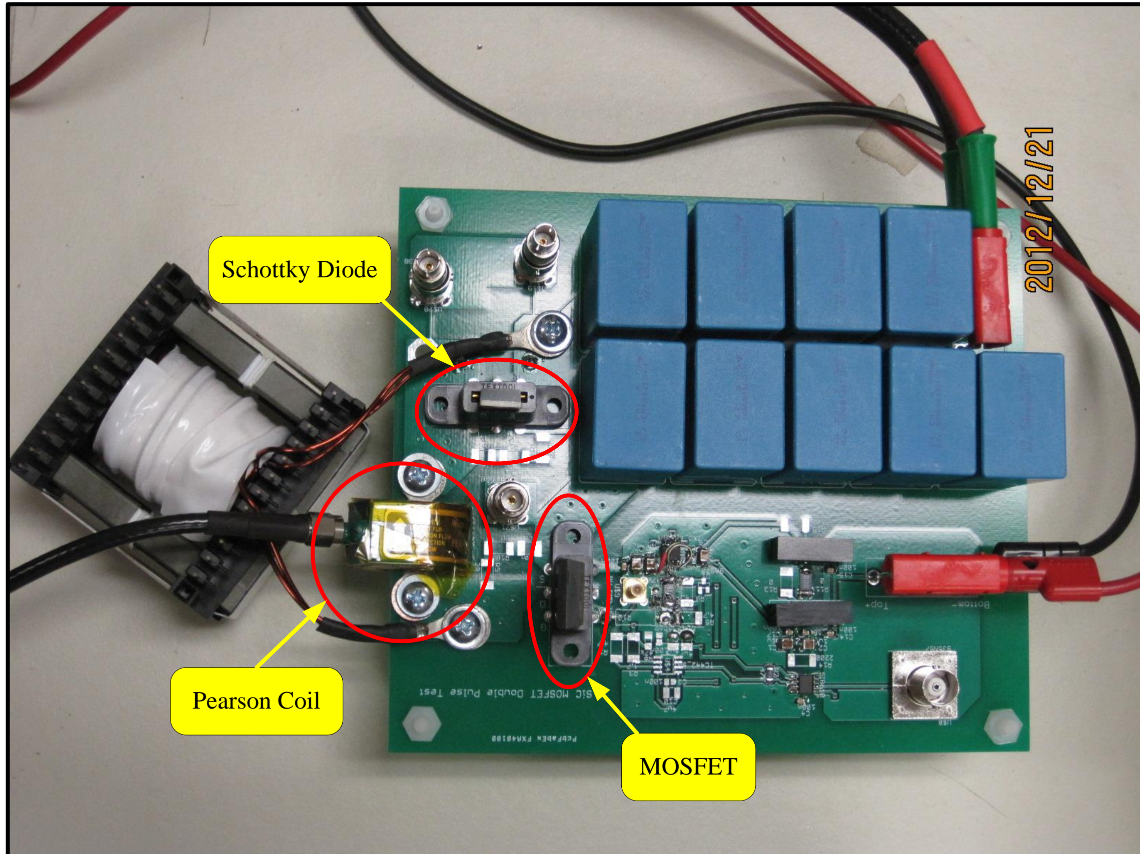


Figure 5.2 Experimental setup of double pulse test-bench.

5.3 Effects of Parasitic Inductances on Switching Behavior

In any switching circuit, parasitic impedances exist everywhere including the semiconductor devices, the interconnections, the sensors, and PCB layout etc. As mentioned in Section 5.1, parasitic inductances are a big concern and limit high performance of switching converters, especially for fast switching SiC devices. Figure 5.3 shows the typical inductive switching loop with main parasitic inductances. L_D represents the drain-to-source switching loop parasitic inductance. L_S is the MOSFET source-leg parasitic inductance and provides a feedback path from MOSFET drain current to gate-source voltage during transitions. L_G is the gate-to-source switching loop parasitic inductance. L_{DD} is the parasitic inductance of free-wheeling diode path.

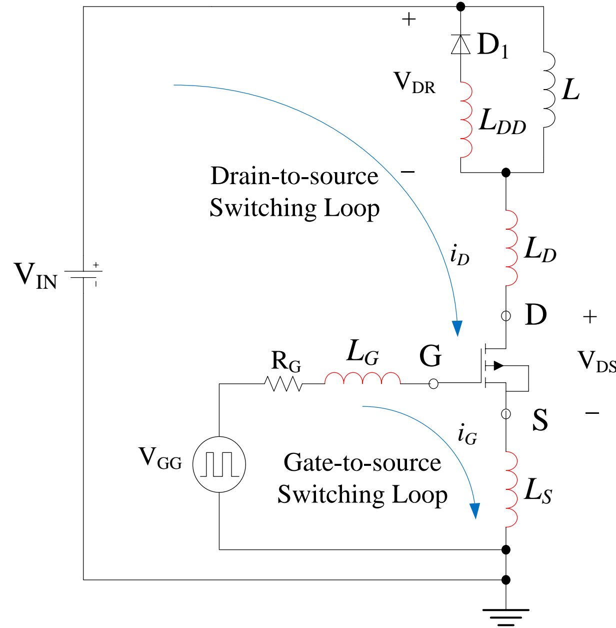


Figure 5.3 Typical inductive switching circuit with main parasitic inductances.

During MOSFET turn on, free-wheeling diode is turning off. The gate-to- source voltage and drain-to-source voltage across the device can be calculated by Equation 5-1and Equation 5-2 respectively.

$$V_{GS} = V_{GG} - R_G i_G - L_G \frac{di_G}{dt} - L_S \frac{d(i_G + i_D)}{dt} \quad \text{Equation 5-1}$$

$$V_{DS} = V_{IN} - V_{DR} - L_D \frac{di_D}{dt} - L_S \frac{d(i_G + i_D)}{dt} \quad \text{Equation 5-2}$$

According to Equation 5-1, during MOSFET turn-on the dynamic gate-to-source voltage V_{GS} decreases with increasing parasitic inductances L_G and L_S, because the voltages across these two inductances are positive with increasing current, which means that the turn-on switching time of the device is slowed down by the presence of these devices. Another way to say this is that there is a negative feedback effect from the drain-to-source switching loop into the gate-to-source switching loop, which opposes device commutation.

During MOSFET turn-off, the free-wheeling diode is turning on. The gate-to-source voltage and drain-to-source voltage across the device can also be calculated by Equation 5-1 and Equation 5-2 respectively. However, because the current is getting smaller, the voltages across the inductances are negative, which means increasing the voltage V_{GS} and V_{DS} across the devices. This can cause overshoot and ripple in the voltage which means increasing the voltage stress of the switching device.

In this chapter, the focus is on the extraction of parasitic inductances due to the PCB layout, which are typically the largest in magnitude and have the largest effect on device switching performance and losses. The other parasitic inductances, such as the parasitic inductances of device package, interconnection and sensor, are not discussed in the dissertation.

5.4 EXTRACTION OF PARASITIC INDUCTANCES OF PCB LAYOUT

In order to obtain the gate-to-source and drain-to-source switching parasitic inductances of the PCB layout, the 3-D inductance extraction program FastHenry was used. FastHenry is a software program which computes the frequency-dependent resistances and inductances of complicated three-dimensional packages and interconnects, assuming operating frequencies up to the multi-gigahertz range [42]. Figure 5.4 shows the X-Y image of PCB traces of the switching loops in FastHenry with the copper thickness of 2.1 mils. Figure 5.5 shows the extracted resistances in gate-to-source and drain-to-source switching loop. Figure 5.6 and Figure 5.7 show the extracted self-inductances in gate-to-source switching loop and drain-to-source switching loop, respectively. L_{R1} is the inductance coming from the trace connected to the input capacitor. L_{DM} is the total trace inductance from the inductor or resistor load to the SiC MOSFET

socket. L_{DD} is the trace inductance from the SiC MOSFET socket to the SiC Schottky diode socket which is the parasitic inductance of the free-wheeling diode current path. L_{SS} is the trace inductance from the SiC MOSFET socket to the input capacitor. L_{G1} is the total parasitic inductance from the driver to the device and L_{G2} is the inductance from the device to the driver. R_{D0} is the total drain-to-source loop parasitic resistance and R_{G0} is the total gate-to-source loop parasitic resistance, which can damp the oscillations in drain-to-source switching loop and gate-to-source switching loop respectively.

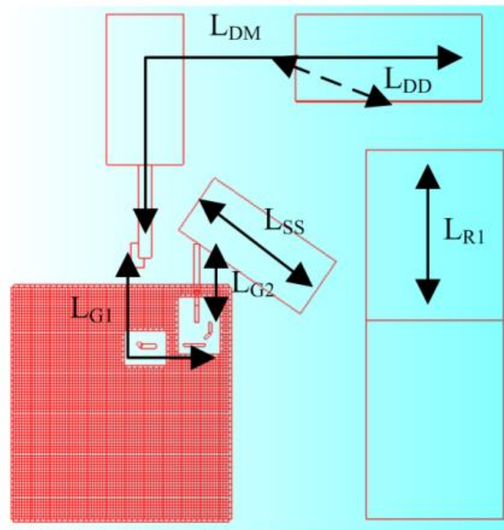


Figure 5.4 X-Y image of PCB traces of the switching loops in FastHenry.

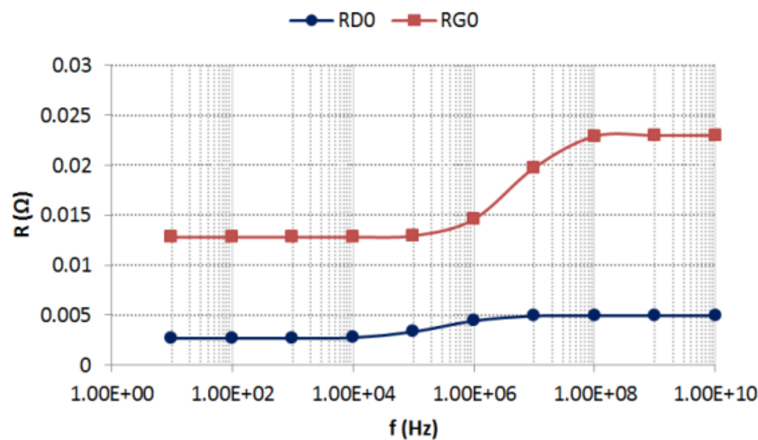


Figure 5.5 Extracted resistances in the switching loop.

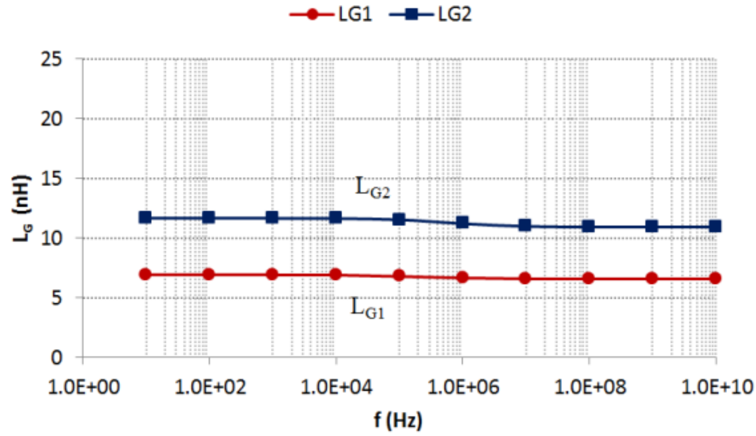


Figure 5.6 Extracted inductances in gate-to-source switching loop.

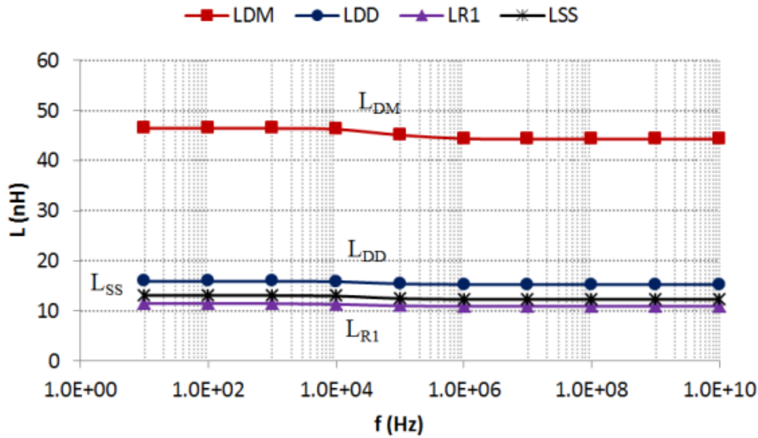


Figure 5.7 Extracted inductances in drain-to-source switching loop.

Figure 5.5, Figure 5.6 and Figure 5.7 show us that at low frequencies the parasitic resistances and inductances are almost constants. However, with frequency increasing and the current crowding on the surface, the parasitic resistances increase and the parasitic inductances decrease. In FastHenry, both the self-inductances and coupling inductances are extracted based on the PCB layout structure. For simplicity, only the self-inductances are taken into account in the switching circuit simulation in this dissertation. The parasitic parameters used in the simulation circuit are the extracted values at low frequencies, which are the parasitic gate resistance $R_{G0}=0.013\Omega$, parasitic drain resistance $R_{D0}=0.003\Omega$, gate-to-source loop parasitic inductances $L_{G1}=7nH$ and $L_{G2}=12nH$ and

drain-to-source loop parasitic inductances $L_{DM}=47nH$, $L_{DD}=16nH$, $L_{R1}=12nH$ and $L_{SS}=13nH$. The inductances are shown in the equivalent circuits of Figure 5.8 and 5.11.

5.5 Model Validation

In this section, the extracted gate-to-source switching loop and drain-to-source switching loop parasitic parameters of the PCB layout are used in Pspice simulation circuit together with the SiC MOSFET and SiC Schottky diode models to validate the resistive and inductive switching behavior of the power devices. The SiC MOSFET model used in this simulation is the physics-based model shown in Figure 3.7, which accounts for non-uniform current distribution in JFET region by using a nonlinear voltage source and a resistance network. The SiC Schottky diode model used in the simulation is the simple model shown in Figure 4.1 (b).

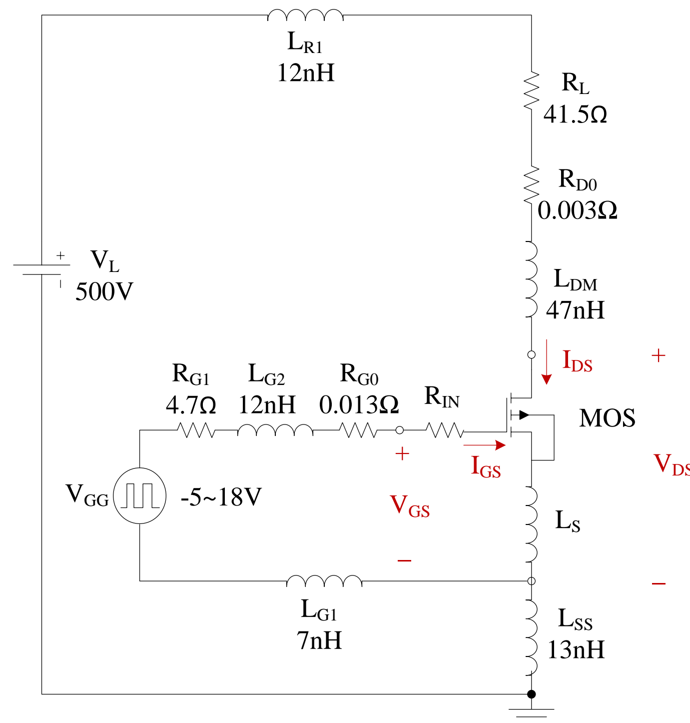


Figure 5.8 Equivalent circuit used for resistive switching circuit.

5.5.1 RESISTIVE SWITCHING VALIDATION

Figure 5.8 shows the resistive simulation circuit corresponding to the experimental double pulse test-bench shown in Figure 5.1, which includes the parasitic parameters extracted in section 5.4. The comparison between simulation and experiment was performed at 500V and 12A at room temperature. The SiC MOSFET is CMF10120D from Cree Inc., which is rated at 1200V. The resistive load is 41.5Ω. The drain current I_{DS} is measured by Pearson coil. The gate current I_{GS} is measured by an AC current probe P6022 from Tektronix with bandwidth of 120MHz. The resistance R_{IN} in the simulation circuit is 13.6Ω, which is the internal gate resistance of the SiC MOSFET.

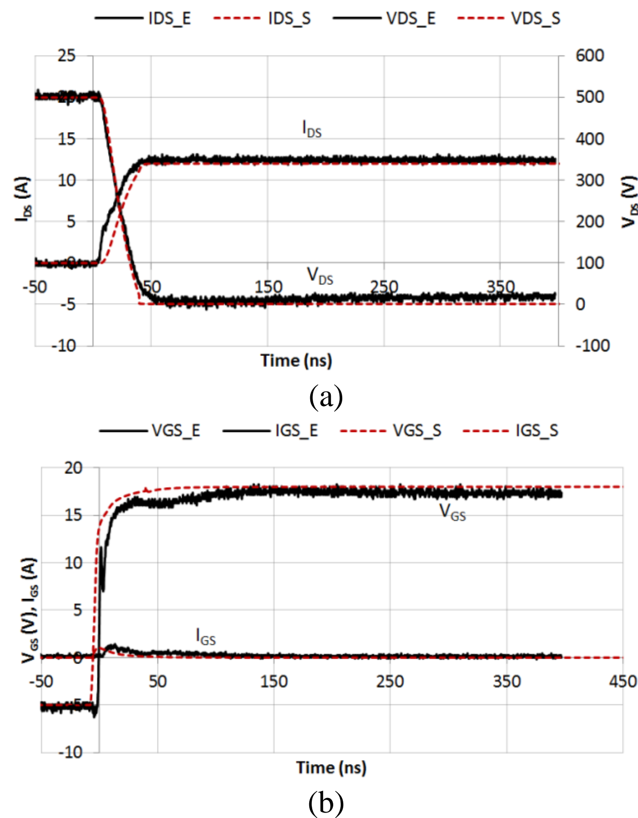


Figure 5.9 SiC DMOSFET simulated (dashed) and experimental (solid) turn-on transient of resistive switching. (a) Comparison of V_{DS} and I_{DS}; (b) comparison of V_{GS} and I_{GS}.

Comparisons between experimental and simulated results are shown in Figure 5.9 for turn-on transient of resistive switching and in Figure 5.10 for turn-off transient. The

figures show that the simulation results are in good agreement with the experimental results. The reason of the small difference in gate-to-source voltage V_{GS} waveform between simulated results and experimental results is that the nonlinear capacitance model C_{GD} does not capture too well the Miller effect of the device when the device is turning on.

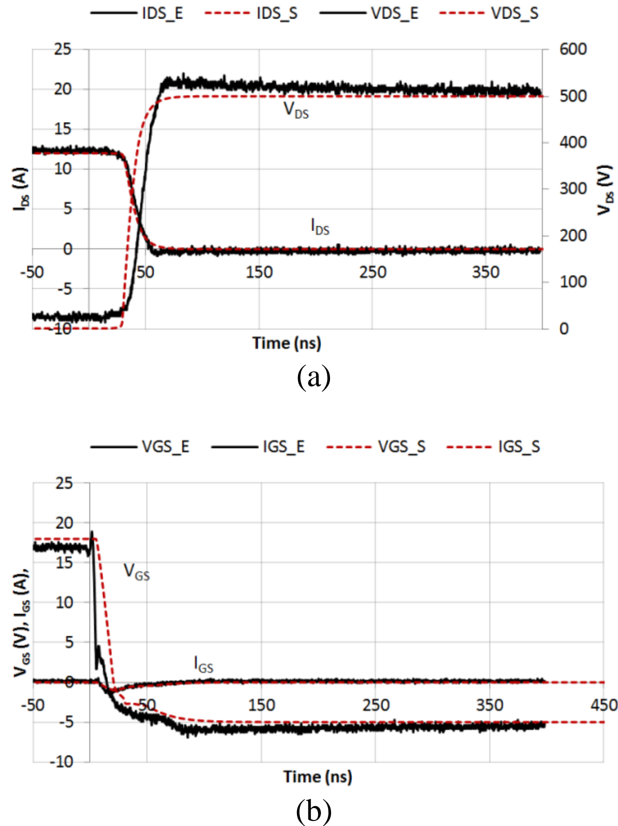


Figure 5.10 SiC DMOSFET simulated (dashed) and experimental (solid) turn-off transient of resistive switching. (a) Comparison of V_{DS} and I_{DS}; (b) comparison of V_{GS} and I_{GS}.

5.5.2 Inductive Switching Validation

As for the resistive switching validation, Figure 5.11 shows the inductive simulation circuit corresponding to the experimental double pulse test-bench shown in Figure 5.1, which includes the parasitic parameters extracted in Section 5.4. In the inductive circuit, the resistance load is replaced by an inductor L_1 and a free-wheeling

SiC Schottky diode in parallel. The free-wheeling diode is a SiC Schottky diode C4D20120A rated at 1200V/20A from CREE Inc. The circuit parameters are as follow: input voltage V_L*=500V*, inductor L_1*=250µH* and pulse generator V_{GG} *=-5~18V*. Figure 5.12 shows the Bode plot of the impedance of inductor L_1, which was measured by Network Analyzer. Notice the self-resonance at 1.26MHz. From the resonant frequency f_0*=1.26MHz* shown in the figure, the parasitic capacitance C_{L1} of the inductor can be calculated by Equation 5-3.

$$C_{L1} = \frac{1}{(2\pi f)^2 L_1} = \frac{1}{(2\pi \times 1.26 \times 10^6)^2 \times 250 \times 10^{-6}} = 64pF \qquad \text{Equation 5-3}$$

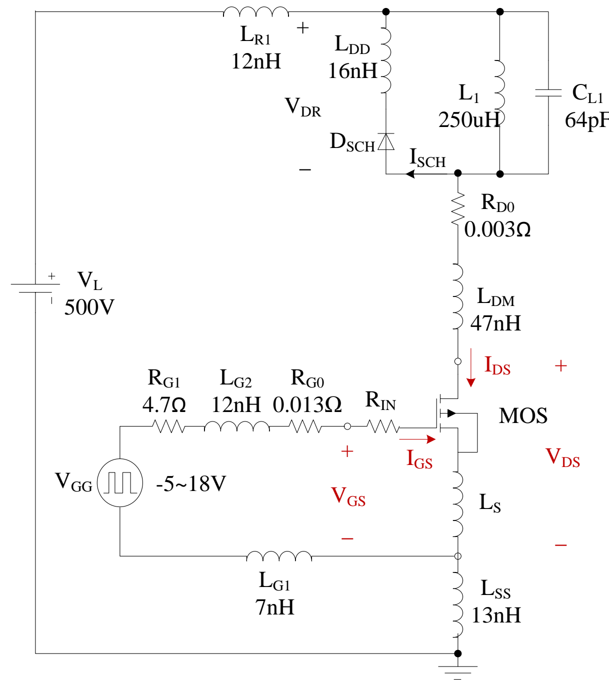


Figure 5.11 Equivalent circuit used for inductive switching circuit.

Using the extracted parasitic inductances and parasitic capacitance C_{L1} of the inductor, the inductive switching simulation was performed in PSpice simulator. Comparisons between experimental and simulated results are shown in Figure 5.13 for turn-on transient of inductive switching and in Figure 5.14 for turn-off transient. As seen

from the figures, the simulation results are in good agreement with the experimental results and the simulation captures the high frequency oscillation ripples.

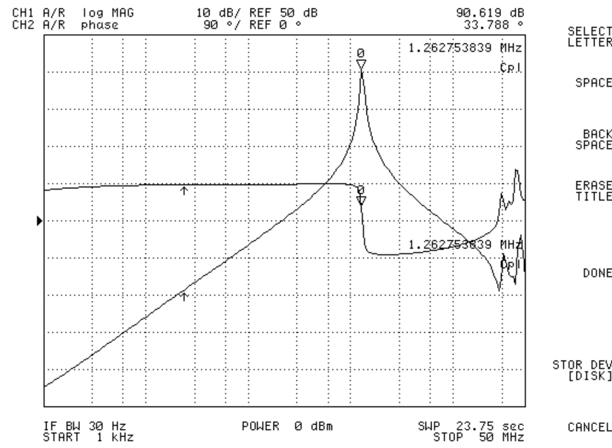
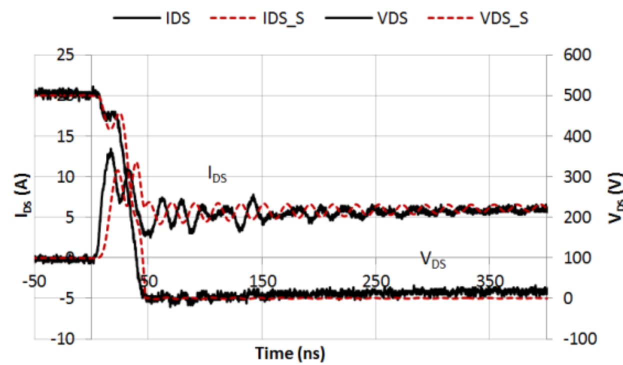
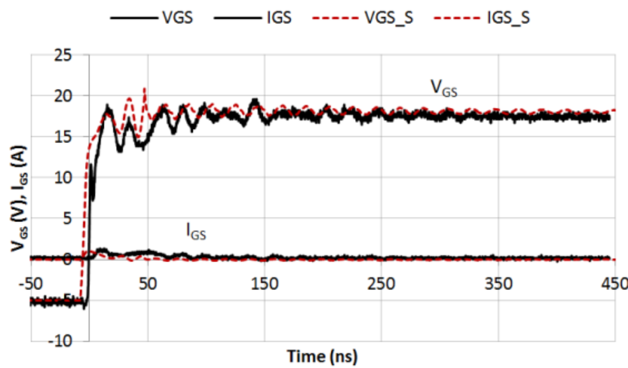


Figure 5.12 Bode plot of inductor L_1.



(a)



(b)

Figure 5.13 SiC DMOSFET simulated (dashed) and experimental (solid) turn-on transient of inductive switching. (a) Comparison of V_{DS} and I_{DS}; (b) comparison of V_{GS} and I_{GS}.

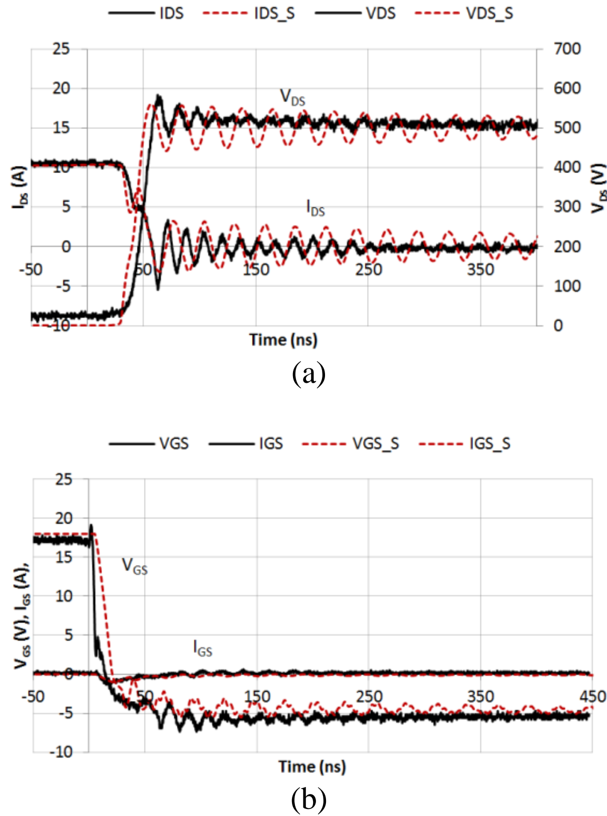


Figure 5.14 SiC DMOSFET simulated (dashed) and experimental (solid) turn-off transient of inductive switching. (a) Comparison of V_{DS} and I_{DS}; (b) comparison of V_{GS} and I_{GS}.

5.6 DISCUSSION

As mentioned before, the effects of parasitic impedances such as parasitic inductances and parasitic capacitances are very important in high frequency and high efficiency switching converter. In order to accurately predict the performance of the switching converter, besides the accurate device model, it is also necessary to extract the specific parasitic impedances in the switching loop, including the parasitic parameters of the semiconductor devices, IC chips, sensors, interconnectors and PCB layout. In other words, the factors that affect the accuracy of the prediction include:

1) The accuracy of the semiconductor device model. A good estimation of the switching circuit needs good models for the semiconductor devices both in

static characteristics and dynamic behavior. The non-linear capacitance model of SiC MOSFET model shown in Figure 3.9 has some discrepancies at low voltage and over-estimates the capacitance for high voltage, which may cause some errors in switching validation for double pulse test-bench.

2) The accuracy of extracted parasitic impedances. In this work, just the parasitic inductances and resistances of PCB layout are estimated by the 3-D inductance extraction program FastHenry. The other parasitic parameters are not specifically discussed and modeled. Also mutual coupling bethween traces is not included. This may also cause some errors during the modeling of double pulse test-bench circuit.

3) The accuracy of measurements of current and voltage. The choice of test instruments and methods may produce some errors too. For good prediction, good models of sensors are also needed in the simulation circuit.

There are some discrepancies in inductive switching validation shown in Figure 5.13 for turn-on transient and Figure 5.14 for turn-off transient. The reasons for these are some of the factors described above. The non-perfect non-linear capacitance model for SiC MOSFET and the parasitic inductance models for the switching loop could be further developed to improve matching.

5.7 SUMMARY

In this chapter, a double pulse test-bench was built to test the switching behavior for SiC devices including SiC MOSFET and SiC Schottky diode both rated at 1200V. In order to capture the parasitic ringing in the fast switching transient, the gate-to-source switching loop and drain-to-source switching loop parasitic inductances and resistances

of the PCB layout are extracted and analyzed using the 3-D inductance extraction program FastHenry. The extracted parameters were used together with the SiC device models developed in the prior chapters for resistive and inductive switching in Pspice simulation and compared with the experimental results. The comparisons show reasonably good agreement between simulated and experimental results in both resistive and inductive switching.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

This dissertation specifically discusses the static and dynamic characteristics of two SiC power devices: SiC DMOSFET and SiC Schottky diode. Two power SiC DMOSFETs are studied in this work including the sample from Cree Inc. rated at 1200V/20A which is validated in CHAPTER 3 and the commercial single package SiC MOSFET CMF10120D also from CREE Inc. rated at 1200V/24A which is validated in CHAPTER 5. There are four power SiC Schottky diodes studied in this work, which includes: A 600V, 50A Schottky diode from GeneSiC Inc.; A 1200V, 3A Schottky diode from GeneSiC Inc.; A 1200V, 7A Schottky diode from GeneSiC Inc.; and A 1200V, 20A Schottky diode from Cree Inc..

Two physics-based SiC device models are presented in this dissertation. One is the new SiC DMOSFET model, the other one is the simple physics-based SiC Schottky diode model with proposed parameter extraction procedure.

For the power SiC DMOSFET, a novel physics-based model accounting for non-uniform current distribution in JFET region is presented. The new feature of the model is that it provides a more physical description of the saturation phenomenon in power MOSFETs, which accounts for JFET region non-uniform current distribution. The physical basis of the proposed model is motivated by finite element simulations. The

finite element simulation shows that current saturation for typical device geometry is due to 2-D carier distribution effects in JFET region caused by current spreading from the channel to the JFET region. For high drain-source voltages, most of the voltage- drop occurs in the current-spreading region located in the JFET region close to the channel. The model is validated both statically and under resistive switching conditions for SiC DMOSFET showing overall good matching with experimental results and finite element simulations.

The power Schottky diode model is a simple physics-based model comprised of a voltage controlled current source, a temperature dependent drift region resistance and a nonlinear capacitance. A detailed parameter extraction procedure for a simple physics-based power SiC Schottky diode model is presented. The proposed parameter extraction procedure includes the extraction of doping concentration, active area and thickness of drift region, which are needed for the proposed physics-based power Schottky diode model. The main advantage is that this procedure does not require any knowledge of device fabrication. The only measurements required for the parameter extraction are a simple static I-V characterization and C-V measurements. Validity of the approach is verified by comparison of simulated and experimental results at temperatures from 25 ℃ to 175 ℃ for four different devices from two different manufacturers which are shown in the first paragraph. Inductive switching validation also shows that the model has a fairly good match with experiments. This means that the model presented in this dissertation is general and can be used for devices with widely different voltage and current ratings.

In CHAPTER 5, the parasitic inductances for resistive and inductive switching of SiC devices in a switching test circuit were modeled and analyzed using a 3-D inductance

extraction program. A double pulse test-bench was built to characterize the resistive and inductive switching behavior of the SiC devices. In order to capture the parasitic ringing in the fast switching transient, the gate-to-source switching loop and drain-to-source switching loop parasitic inductances of the PCB layout are extracted by the 3-D inductance extraction program. The system model in Pspice includes SiC device models and the extracted parasitic elements. Simulation results are compared with experimental results. The comparison shows good agreement between simulation and experimental results under both resistive and inductive switching conditions.

Based on the studies of the effects of parasitic impedances in the switching circuit presented in CHAPTER 5, the following guidelines can be given for optimized switching converter layout circuit design for high- frequency high- performance converter applications.

1) Choose the power devices with smaller inner parasitic capacitances to reduce the parasitic ringing during switching time. Especially for power MOSFETs, the Miller capacitance C_{GD} should be as small as possible to guarantee faster switching transients.
2) When designing the PCB layout, always keep the high frequency switching loop of the circuit as short as possible. Since the source parasitic impedance L_{ss} plays a critical role in the switching transient, it is necessary to minimize this path to reduce the ringing of the switching circuit and decrease the voltage overshoot of the devices.
3) Use the best possible measurement method to avoid introducing parasitic impedances into the circuit. For voltage measurement, minimize the ground

path test point. Use a suitable current sensor in the switching circuit to avoid introducing parasitic inductance in the switching loop which worsens the parasitic ringing of the waveforms.

6.2 FUTURE WORK

The superior material properties of SiC material for power electronics applications are its wide bandgap and high thermal conductivity, which make SiC-based devices attractive in high voltage, high power and high temperature applications. Therefore, for better simulation-based predictions of performance in switching converter applications, the SiC power devices need to be modeled and validated at high temperature as well.

There are two physics-based SiC device models presented in this dissertation. One is the new SiC DMOSFET model accounting for non-uniform current distribution in JFET region, the other one is the simple physics-based SiC Schottky diode model with proposed parameter extraction procedure. Both of these models are validated at room temperature, but just the Schottky diode model is validated at high temperature for static characteristics. The validation of SiC DMOSFET model is left for future work.

As seen in Figure 3.9 in CHAPTER 3, the parasitic capacitances used in the proposed SiC DMOSFET model are not accurate enough for very good prediction. It is necessary to model the parasitic capacitances in a better way.

The 3-D inductance extraction program FastHenry used in this work is better for simple assessment of parasitic inductances compared to the Maxwell Q3D Extractor or the Ansoft Q3D Extractor. The parasitic inductances discussed in CHAPTER 5 for

switching behavior of SiC devices are just self-inductances. The mutual inductances of the PCB layout are not included in this dissertation.

Therefore, future work for SiC device modeling includes:

1. Resistive and inductive switching experiments at higher temperature. The experiment temperature is limited by package of SiC devices, which has much lower temperature range compared to SiC material and devices.
2. Resistive and inductive switching validation of physics- based SiC power device models at higher temperature;
3. Improve the parasitic non-linear capacitances of SiC MOSFET, which has strong effect on dynamic characteristics of SiC MOSFET.
4. Consideration of the effect of parasitic mutual coupling on switching waveforms.
5. A high-performance commercial SiC MOSFET power module rated at 1,200V, 50A will be characterized and compared with the double pulse test-bench described in this work. The module is expected to have significantly smaller parasitic inductances and be capable to operate at higher switching speeds.

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