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***Abstract*—The breakdown voltages in unpassivated nonfield-plated AlGaN/GaN HFETs on sapphire substrates were studied. These studies reveal that the breakdown is limited by the surface flashover rather than by the AlGaN/GaN channel. After elimination of the surface flashover in air, the breakdown voltage scaled linearly with the gate–drain spacing reaching 1.6 kV at 20 μm. The corresponding static ON-resistance was as low as 3.4 m$\Omega \cdot$ cm^2. This translates to a power device figure-of-merit $V_{\rm BR}^2/R_{\rm ON} = 7.5 \times 10^8$ V$^2 \cdot \Omega^{-1}$ cm^{-2}, which, to date, is among the best reported values for an AlGaN/GaN HFET.**

***Index Terms*—AlGaN/GaN HFET, breakdown voltage, high-electron mobility transistor (HEMT), high-voltage power device, surface flashover.**

I. Introduction

III-NITRIDE HFETs are promising devices for high-power energy converters. Compared with SiC FETs, GaN HFETs have lower specific ON-resistance due to the high-density two-dimensional electron gas (2-DEG), i.e., above 10^{13} cm^{-2}, and high electron mobility, i.e., above 1500 cm^2/V $\cdot$ s. For AlGaN/GaN HFETs, the contact resistance R_C can be a significant portion of the total device resistance. The expression for the minimal specific ON-resistance $(R_{\rm ON})$ accounting for R_C can be derived from [1] as follows:

$$R_{\rm ON} \times A = \left(2R_C + R_{\rm SH} \times \frac{V_{BR}}{E_C}\right) \times \left(\frac{V_{\rm BR}}{E_C} + \frac{2R_C}{R_{\rm SH}}\right) \quad (1)$$

where R_C and $R_{\rm SH}$ are the specific contact resistance and the sheet resistance of the 2-DEG channel, respectively; $V_{\rm BR}$ is the breakdown voltage; E_C is the breakdown field; and A is the device area. For vertical-geometry SiC- and Si-based devices, the $R_{\rm ON}$ resistance is given by $(R_{\rm ON} \times A) = 4V_{\rm BR}^2/(\varepsilon_r \mu E_{C,({\rm SiC,Si})}^3)$ [2]. The $(R_{\rm ON} \times A){-}V_{\rm BR}$ dependences for AlGaN/GaN HFETs, SiC, and Si devices are compared in Fig. 1. As shown, for typical values of contact resistances in AlGaN/GaN HFETs, the contribution of R_C is significant for devices with $V_{\rm BR}$ below 1000 V, whereas for devices with higher $V_{\rm BR}$, the channel resistance dominates. Thus, the challenge in achieving the lowest $R_{\rm ON}$ values in the kilovolt-range III-N HFETs is to maximize the breakdown voltage at minimal electrode spacing. The gate–drain spacing $L_{\rm GD}$ is the critical dimension affecting the breakdown voltage [3]–[8], [14] as it accommodates most of the applied voltage. The $V_{\rm BR}{-}L_{\rm GD}$ dependences reported in the past saturate at large $L_{\rm GD}$, limiting the achievable $V_{\rm BR}$ values to 400–600 V. Insulated gate [5], [9] and multiple field-plate [7] designs were used to obtain $V_{\rm BR} = 1300$ and 900 V correspondingly, but no $L_{\rm GD}$ dependence was reported. The reasons for the $V_{\rm BR}{-}L_{\rm GD}$ saturation and device scaling approaches to obtain low $R_{\rm ON}$ devices with the breakdown voltages above 600 V still remain unclear. In this letter, we present a study aimed at understanding the breakdown mechanism and the $V_{\rm BR}{-}L_{\rm GD}$ dependence in AlGaN/GaN HFETs. To filter out other effects affecting the breakdown, unpassivated nonfield-plated devices were used.

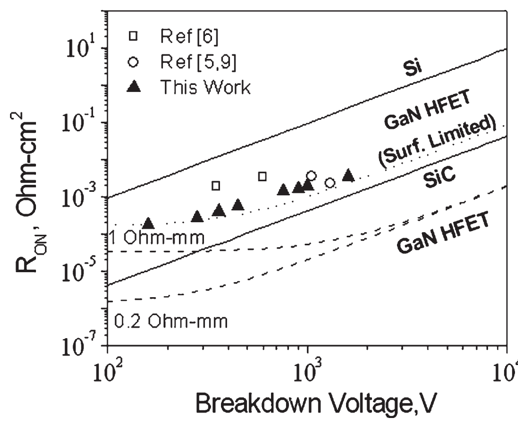

Fig. 1. Comparison of $V_{\rm BR}{-}R_{\rm ON}$ of the fabricated AlGaN/GaN HFET devices to the previously reported values and theoretical GaN limits. Dashed lines show the dependences according to (1) for two values of specific contact resistance. The dotted line shows the dependence according to (1), with $R_C = 1\ \Omega \cdot$ mm and $E_C = 0.8$ MV/cm corresponding to the surface- or buffer-limited breakdown.

II. Experimental Details and Discussion

The AlGaN/GaN HFETs with 25-nm $Al_{0.25}Ga_{0.75}N$ barrier layer were grown on sapphire substrates by low-pressure metal–organic chemical vapor deposition (MOCVD). The device epilayer structure consisted of a 15-nm-thick low-temperature-grown AlN buffer layer followed by a 1.5-μm-thick undoped GaN layer, which was capped with the barrier layer. The devices were fabricated using mesa etching, Ti/Al/Ti/Au ohmic contact deposition, and annealing followed by Ni/Au gate formation. The gate length $L_G = 2$ μm and gate–source spacing $L_{\rm GS} = 2$ μm were kept constant, whereas the gate–drain spacing $L_{\rm GD}$ varied from 2 to 20 μm. The gate width was $W_G = 100$ μm. The $R_{\rm SH} = 350$ Ω/sq and $R_C = 1\ \Omega \cdot$ mm values were obtained using a standard transmission line method (TLM) procedure. The threshold voltage was $V_T = -4.5$ V. The breakdown voltage was defined as the drain voltage at which the drain–current reaches 1 mA/mm with the gate biased below the threshold voltage. The devices were first

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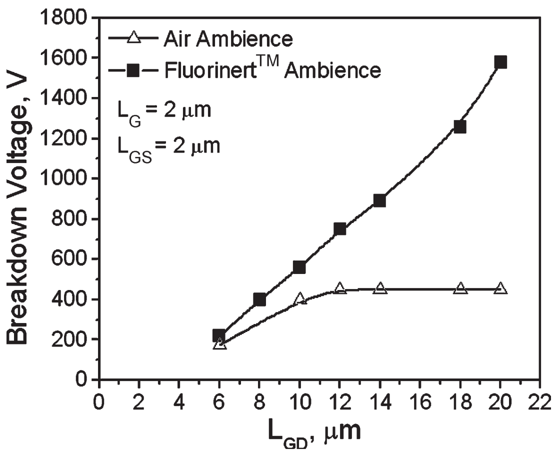

Fig. 2. $L_{\rm GD}-V_{\rm BR}$ dependence of the devices measured in air ambience and Fluorinert ambience.

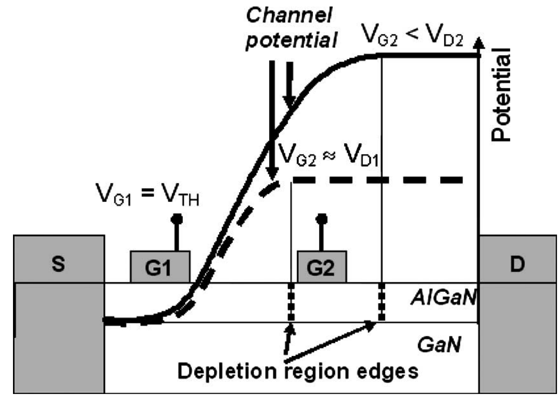

Fig. 3. Layout of devices with the probe gates used for channel potential profiling. The potential variation in the channel at different drain voltages is shown.

tested in the air ambient. As shown in Fig. 2, $V_{\rm BR}$ increased linearly with $L_{\rm GD}$ for $L_{\rm GD} \leq 12$ μm and saturates at $V_{\rm BR} =$ 450 V. An analysis of the devices after breakdown revealed that the gate metal evaporation was the main reason for the device failure in all the cases. This is similar to the observations of Sudarshan *et al.* [10], suggesting that the breakdown was premature and resulted from the surface flashover. Note that the saturation breakdown voltage of around 450 V is above the Paschen's minimum voltage of 325 V [11] for the air breakdown. A correlation between the obtained HFET $V_{\rm BR}-L_{\rm GD}$ curve and that for the air [11] leads us to a speculation that the surface flashover is responsible for the premature HFET breakdown. To verify this assertion, the HFETs were measured immersed in the Fluorinert solution. Fluorinert solution has a high dielectric strength of 18 MV/m as compared with 3 MV/m for the air. As shown in Fig. 2 (square symbols), with Fluorinert immersion, no $V_{\rm BR}-L_{\rm GD}$ dependence saturation was observed even for $L_{\rm GD} = 20$ μm, where the $V_{\rm BR}$ was 1600 V. For this spacing, the measured device static ON-resistance was 3.4 m$\Omega \cdot$ cm^2, giving the device figure-of-merit $V_{\rm BR}^2/R_{\rm ON} = 7.5 \times 10^8\ V^2 \cdot \Omega^{-1}$ cm^{-2}.

Next, we verified the nature of the device breakdown in the Fluorinert ambient. We compared the breakdown voltages for devices with completely pinched-off ($V_{\rm GS} = -6$ V) and partially open ($V_{\rm GS} = -4.25$ V) channels. For $L_{\rm GD} = 10$ μm, a pinched-off channel breakdown voltage was 560 V, whereas for $V_{\rm GS} = -4.25$ V, it had a higher value of 610 V. If the breakdown was initiated by an avalanche process in the channel, the breakdown voltage should have decreased [12]. Defect ionization in the buffer may contribute in the breakdown; in this case, higher channel concentration at $V_{\rm GS} = -4.25$ V may be screening the electric field in the buffer, leading to a higher $V_{\rm BR}$. Therefore, even in the Fluorinert, the breakdown is still not limited by the 2-D channel avalanche. Note that the $V_{\rm BR}-L_{\rm GD}$ slope in the Fluorinert ambient corresponds to a critical field $E_C \approx 0.8$ MV/cm, which exceeds the value of 0.18 MV/cm specified for the Fluorinert; this suggests that the breakdown can still be surface limited. Hence, further optimization of the surface conditions and buffer quality would lead to high breakdown voltages at even smaller gate–drain spacing. The dotted line in Fig. 1 is plotted using (1), with $E_C = 0.8$ MV/cm as found from above experiments; other parameters are the same as those used above for the GaN HFETs (dashed lines). Symbols in Fig. 1 show the results of this letter and other published data. As shown, these results lie close to the dotted line, suggesting that surface or buffer breakdown is the limiting factor for most of the reported data. Unpassivated HFET devices cannot be directly used as switching elements due to the high dynamic ON-resistance caused by current collapse. After SiN passivation, our devices showed high gate leakage currents, leading to lower breakdown voltages. However, subsequent field-plate deposition limited the gate currents and increased the $V_{\rm BR}$ values close to those of unpassivated HFETs. Detailed results on the passivated and field-plated HFETs will be published elsewhere.

We further analyzed the reasons for the absence of avalanche breakdown in the HFET channel. The gate-channel separation in these devices is only about $d \approx 250$ Å. Ignoring the gate edge fields and the depletion region extension, the average electric field in the channel at $V_{\rm DS} = 1$ kV would be $E_A \approx V_{\rm DS}/d \approx$ 400 MV/cm, which well exceeds the GaN breakdown field of ~ 3 MV/cm [1]. Thus, the depletion region extension toward the drain must be significant to maintain the electric fields below the critical values. To verify this, we used additional Schottky electrode probes that were deposited on the AlGaN barrier between the gate and the drain (Fig. 3) [13]. The gate to probe distance was varied from 2 to 6 μm. The channel potential was measured by balancing the voltage induced in the probe gate electrodes by an external voltage until the probe gate current became zero. The channel potential was used to estimate the depletion region propagation. When the probe electrode is located outside the depletion region, its potential is close to that of the drain (see Fig. 3). Once the depletion region reaches the probe gate, its potential becomes considerably lower than the drain voltage.

In the above experiments, the gate voltage was below the threshold ($V_{\rm GS} = -6$ V). The difference between the probe potential V_{G2} and the drain voltage $V_{\rm DS}$ as a function of $V_{\rm DS}$ is shown in Fig. 4. The drain voltage at which $V_{\rm DS} - V_{G2}$ starts departing from zero is the voltage at which the depletion region edge has reached the probe gate. The depletion region

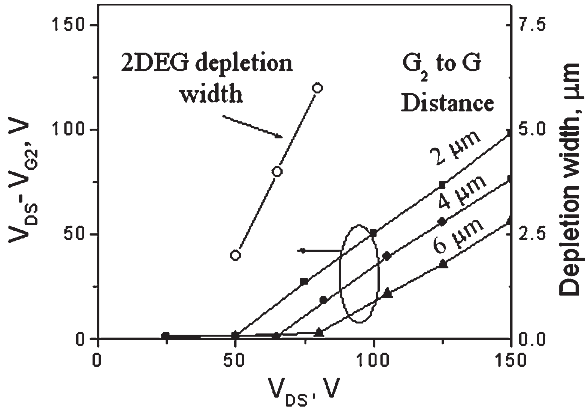

Fig. 4. Left axis: Difference between the drain and the balanced probe gate voltages ($V_{\mathrm{DS}}-V_{G2}$) against drain bias (V_{DS}) for 2, 4, and 6 μm spacing between the main and the probe gates. Right axis: Depletion region width against the drain voltage.

width–drain voltage dependence extracted from these data is plotted in Fig. 4. As shown, the depletion region width can be as high as 6 μm at the drain bias $V_{DS} = 80$ V, showing that the depletion width extension decreases the field in the channel and prevents the channel breakdown. The width of the HFET depletion region is also a strong function of the surface conditions, barrier doping, etc. More studies of the factors affecting the depletion width are needed to optimize high-voltage AlGaN/GaN HFETs.

III. Conclusion

The surface flashover has been identified as one of the key limiting factors for the breakdown in unpassivated nonfield-plated AlGaN/GaN HFETs. A breakdown voltage of 1600 V was achieved for HFETs with the gate–drain spacing of 20 μm in a Fluorinert ambient. For such a high-voltage device, the static specific ON-resistance was 3.4 m$\Omega \cdot$ cm^2, which is among the lowest reported values to date. We show that elimination of surface- or buffer-limited breakdown allows for even higher voltages with lower R_{ON} values in AlGaN/GaN HFETs.

References

[1] S. Karmalkar, J. Deng, M. S. Shur, and R. Gaska, "RESURF AlGaN–GaN HEMT for high voltage power switching," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 373–375, Aug. 2001.

[2] B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1717–1731, Oct. 1996.

[3] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. Denbaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 421–423, Sep. 2000.

[4] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang, M. Asif Khan, R. Gaska, and M. S. Shur, "A 7.5 kW/mm^2 current switch using AlGaN/GaN metal–oxide–semiconductor heterostructure field effect transistors on SiC substrates," *Electron. Lett.*, vol. 36, no. 24, pp. 2043–2044, Nov. 2000.

[5] N.-Q. Zhang, B. Moran, S. P. Denbaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Kilovolt AlGaN/GaN HEMTs as switching devices," *Phys. Status Solidi A*, vol. 188, no. 1, pp. 213–217, 2001.

[6] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN–GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.

[7] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN–GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 161–163, Apr. 2004.

[8] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan, and M. S. Shur, "AlGaN/GaN heterostructure FET's with offset gate design," *Electron. Lett.*, vol. 33, no. 14, pp. 1255–1257, Jul. 1997.

[9] N. Zhang, V. Mehrotra, S. Chandrasekaran, B. Moran, L. Shen, U. Mishra, E. Etzkorn, and D. Clarke, "Large area GaN HEMT power devices for power electronic applications: Switching and temperature characteristics," in *Proc. PESC*, 2003, pp. 233–237.

[10] T. S. Sudarshan, G. Gradinaru, J. Yang, and M. A. Khan, "Surface flashover effects in AlGaN/GaN HFETs," *Electron. Lett.*, vol. 34, no. 9, pp. 927–928, 1998.

[11] P. G. Slade and E. D. Taylor, "Electrical breakdown in atmospheric air between closely spaced (0.2 μm–40 μm) electrical contacts," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 3, pp. 390–396, Sep. 2002.

[12] M. H. Somerville, R. Blanchard, J. A. del Alamo, K. G. Duh, and P. C. Chao, "On-state breakdown in power HEMT's: Measurements and modeling," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1087–1093, Jun. 1999.

[13] R. Vetury, Y. F. Wu, P. T. Fini, G. Parish, S. Keller, S. DenBaars, and U. K. Mishra, "Direct measurement of gate depletion in high breakdown (405 V) AlGaN/GaN heterostructure field effect transistors," in *IEDM Tech. Dig.*, San Francisco, CA, Dec. 6–9, 1998, pp. 55–58.

[14] S. Yagi, M. Shimizu, Y. Yamamoto, G. Piao, Y. Yano, and H. Okumura, "High breakdown voltage AlGaN/GaN MIS-HEMT with SiN and TiO$_2$ gate insulator," in *Proc. Int. Semicond. Device Res. Symp.*, Washington, DC, Dec. 2005, pp. 280–281.