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3510-V 390-m$\Omega \cdot$ cm^2 4H-SiC Lateral JFET on a Semi-Insulating Substrate

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***Abstract*—The performance of high-voltage 4H-SiC lateral JFETs on a semi-insulating substrate is reported in this letter. The design of the voltage-supporting layers is based on the charge compensation of p- and n-type epilayers. The best measured breakdown voltage is 3510 V, which, to the authors' knowledge, is the highest value ever reported for SiC lateral switching devices. The $R_{\rm on}$ of this device is 390 m$\Omega \cdot$ cm^2, in which 61% is due to the drift-region resistance. The $BV^2/R_{\rm on}$ is 32 MW/cm^2, which is typical among other reported SiC lateral devices.**

***Index Terms*—High voltage, JFETs, lateral, silicon carbide.**

I. Introduction

SILICON carbide (SiC) devices are potential candidates for the next generation of power devices. Both prototype and commercialized SiC devices have demonstrated a higher voltage blocking capability with a lower ON-state resistance compared to their Si counterparts. For the same blocking voltage, SiC devices can switch faster, consume less power, and handle a greater power density because of their superior material properties, such as high critical electrical field and high thermal conductivity. Most previous research has been focused on vertical devices because they can operate at higher current densities. However, there are applications where lateral structures are more attractive, particularly in the area of power integrated circuits (PICs). Although PICs in silicon have been developed and commercialized over the decades, high-voltage SiC lateral devices have only begun to attract attention in recent years. Lateral SiC MOSFETs and JFETs have demonstrated blocking voltages as high as 2700 V and $BV^2/R_{\rm on}$ numbers that far exceed the limit of vertical Si devices [1]–[6]. Compared with SiC MOSFETs, SiC JFETs have an advantage in that they do not suffer from gate-oxide quality issues and poor inversion channel properties. Significant progress in the development of SiC JFETs has been made in the past few years. In 2004, a normally on RESURF-type lateral SiC JFET was reported to achieve a blocking voltage of 800 V and an $R_{\rm on}$ of 50 m$\Omega \cdot$ cm^2 [5]. In 2007, a vertical channel lateral JFET based on RESURF design was reported to achieve a blocking voltage of 1000 V and an $R_{\rm on}$ of 9.1 m$\Omega \cdot$ cm^2 [6]. These results are very promising. However, since the depletion region expands both laterally and vertically under reverse biases, these devices require a thick and lightly doped p-layer on a conducting substrate, which is limited by current SiC epitaxy technology.

In our previous work, a 4H-SiC lateral p-n diode that achieved a breakdown voltage of 3130 V was demonstrated, showing the advantage of using a semi-insulating substrate with relatively thin charge-compensated p-n layers stacked as the voltage-supporting region [7]. This letter reports the performance of 4H-SiC lateral JFETs that are based on the same design concept. The breakdown voltage is 3510 V, which is more than three times that of the highest value previously reported for SiC lateral JFETs. The $R_{\rm on}$ of this device is 390 m$\Omega \cdot$ cm^2, resulting in a $BV^2/R_{\rm on}$ of 32 MW/cm^2.

II. Device Design and Fabrication

An n- and a p-layer were grown on the Si face of an off-axis 4H-SiC vanadium-doped semi-insulating wafer. Doses in both layers were designed to deplete each other under high reverse bias. Without the participation of dopants in the substrate, charge compensation can be much more precisely controlled in the drift region. The nominal doping/thickness values of the n- and p-layers were 1.4×10^{17} cm^{-3}/0.5 μm and 6×10^{16} cm^{-3}/1 μm, respectively. Aluminum was implanted at 650 °C, with a plasma-enhanced chemical vapor deposition (PECVD) oxide being used as the mask to form the p+ sinker and the p+ gate. The implant doses/energies were 1×10^{12} cm^{-2}/50 keV and 1×10^{14} cm^{-2}/360 keV. The p+ sinker region was etched to a depth of 0.12 μm before implantation to ensure that it would reach the bottom p-layer. The p+ gate region was masked with a 500-nm oxide, and the resulting junction depth was estimated to be 0.27 μm, leaving a channel width of about 0.19 μm at zero gate bias. Nitrogen was then implanted at room temperature to form the source/drain regions. Implant species were activated at 1650 °C for 30 min in argon. RIE was performed to create 1.9-μm-deep isolation trenches around the devices. A layer of oxide was grown at 1180 °C in a dry ambient for 6 h to passivate the surface. The contact areas were then selectively etched using BOE. A 100-nm/20-nm Ni/Ti layer was thermally evaporated and lifted off as the n- and p-type contact metals. Contacts were annealed at 1100 °C for 3 min in vacuum. A 500-nm PECVD oxide layer

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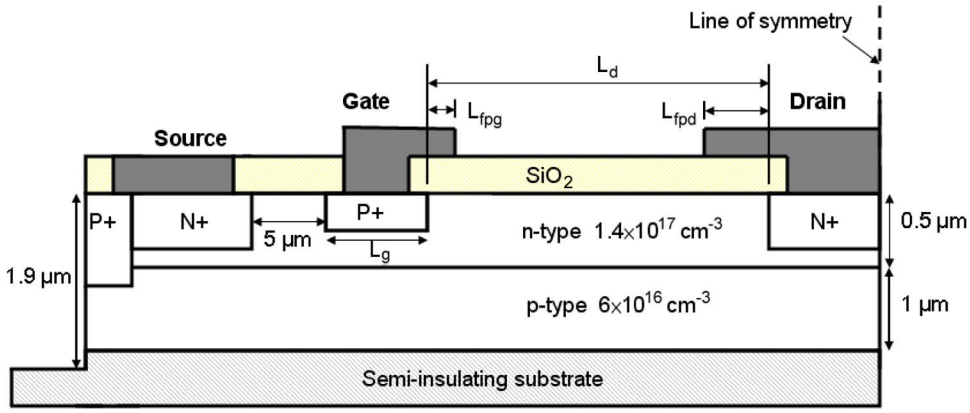

Fig. 1. Schematic cross section of a 4H-SiC lateral JFET on a semi-insulating substrate.

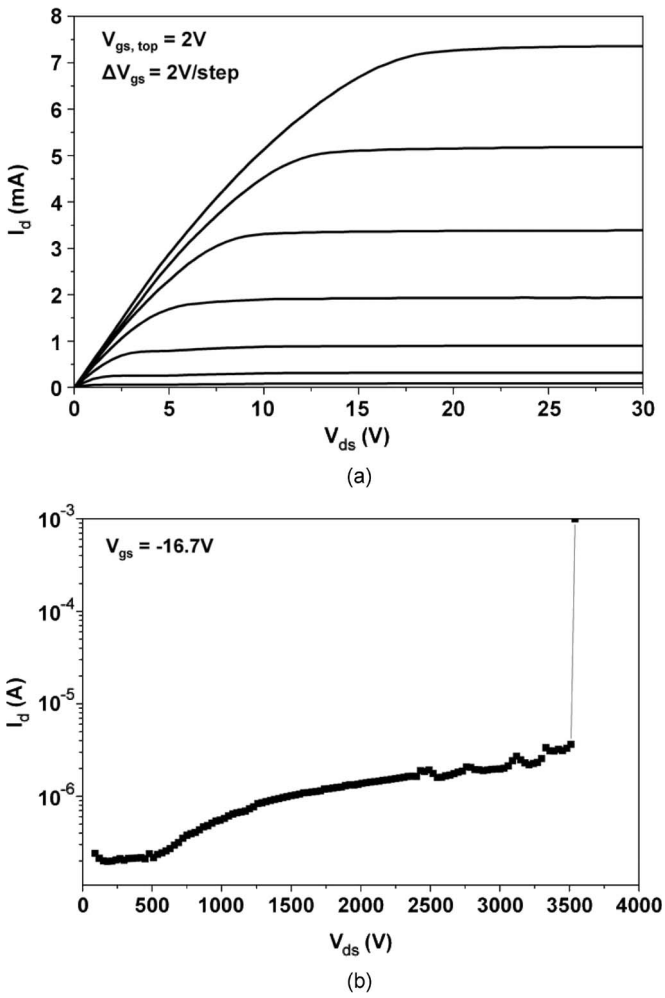

Fig. 2. (a) Forward and (b) reverse characteristics of a device with $L_g = 9$ μm, $L_d = 100$ μm, $L_{\rm fpg} = 10$ μm, and $L_{\rm fpd} = 25$ μm.

was deposited as the field oxide. Windows were opened, and an Al/Ti layer was patterned to form the gate metal, the pads, and the field plates. Fig. 1 shows the schematic cross section of the devices.

III. Results and Discussion

All devices were probe tested on wafer. Breakdown voltage tests were carried out with the sample immersed in Fluorinert.

TABLE I
Device Characteristics for Different L_d's

L_d (μm)	R_{on} (mΩ-cm^2)	BV (kV)
25	66	1.27
50	145	1.51
80	291	2.32
100	390	3.51

Fig. 2 is a plot of the forward and reverse characteristics of a device with $L_g = 9$ μm, $L_d = 100$ μm, $L_{\rm fpg} = 10$ μm, and $L_{\rm fpd} = 25$ μm. The width of the device is 200 μm, and the active area is 0.0228 mm^2. This device exhibits normally on characteristics with a pinchoff voltage of about -11 V. The extracted $R_{\rm on}$ of this device at room temperature is 390 m$\Omega \cdot$ cm^2 when $V_{\rm gs} = 2$ V and $V_{\rm ds} = 1$ V. $R_{\rm on}$ increases monotonically with temperature to 744 m$\Omega \cdot$ cm^2 at 125 °C, following a $T^{2.2}$ relationship, which implies that the total resistance is governed by the electron drift current in the channel and the n-layer since the bulk electron mobility has a $T^{-2.4}$ relationship in 4H-SiC [8]. A comparison of the $R_{\rm on}$ for devices with $L_d = 25, 50, 80, \text{and } 100$ μm indicates that the drift region contributes about 61% of the total resistance in the $L_d = 100$ μm device. By comparing the $R_{\rm on}$ for devices with $L_g = 9$ and 15 μm, it can be seen that the channel resistance comprises about 18.6% of the total resistance. During the reverse bias sweep, -16.7 V was applied to the gate. The drain leakage current was below 4×10^{-6} A until the device experienced a catastrophic breakdown at 3510 V. Table I is a summary of the BV and $R_{\rm on}$ for devices with different L_d's. Fig. 3 shows the transfer characteristics at $V_{\rm ds} = 25$ V. The gate leakage current was below 1×10^{-8} A until the gate junction turns on at $V_{\rm gs} = 3$ V. The maximum transconductance g_m is 1.21 mS at $V_{\rm gs} = 2.5$ V. The trapping effects that have been identified in 4H-SiC MESFETs on semi-insulating substrates are also observed in these devices [9]–[11]. Fig. 4 is a plot showing the I_d–V_d curves for a device with $L_g = 15$ μm and $L_d = 100$ μm. The solid curves represent the I–V's measured after the device reaches an equilibrium state—without applying any bias for a long period. The dashed curves represent the I–V's measured immediately after. A clear discrepancy exists between these curves and can be explained by the trapping of electrons at the SiO_2/SiC interface, in the defects in the p-layer, and in the deep levels in the substrate. The trapped

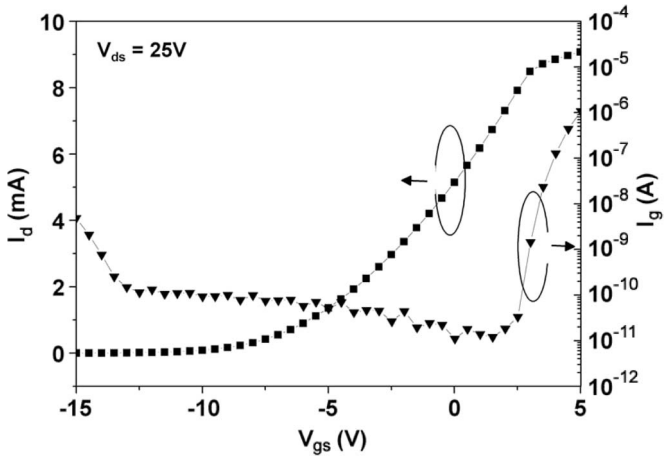

Fig. 3. Plot of I_d and I_g versus $V_{\rm gs}$ at $V_{\rm ds} = 25$ V for the device shown in Fig. 2.

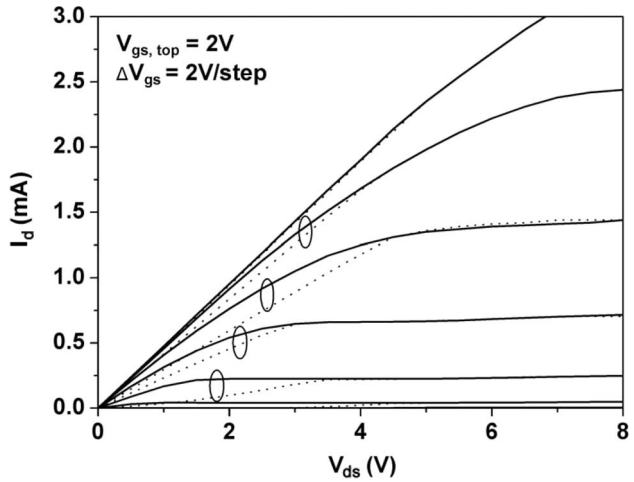

Fig. 4. I_d–$V_{\rm ds}$ of a device with $L_g = 15$ μm and $L_d = 100$ μm. The solid curves represent the first measured I–V's after the device reaches an equilibrium state—without applying any bias for a long period. The dashed curves are the I–V's measured immediately after.

electrons deplete the channel and the lightly doped n-type layer, reducing its conductance when the device is turned on. After the electrons are released from the traps and the device returns to an equilibrium state, the I–V curves resume their original trajectory. The fact that there is little drain-current reduction (less than 8%) at $V_{\rm gs} = 0$ V suggests that the trapped electron density is much less than the dose of the n-layer. However, its effect on the charge balance and the BV is not clear at this point. This problem can be alleviated by using a high-purity semi-insulating substrate and an improved passivation scheme [11].

IV. Conclusion

High-voltage 4H-SiC lateral JFETs on a semi-insulating substrate have been demonstrated for the first time. The best measured breakdown voltage was 3510 V, which, to the authors' knowledge, was the highest value ever reported for SiC lateral switching devices. The $R_{\rm on}$ was 390 m$\Omega \cdot$ cm^2, and the $BV^2/R_{\rm on}$ was 32 MW/cm^2. The drain-current drift was observed and attributed to trapping effects similar to those of SiC MESFETs. Further improvement to fully realize the potential of this lateral device technology is under investigation.

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References

[1] T. Kimoto, H. Kawano, and J. Suda, "1330 V, 67m$\Omega \cdot$ cm^2 4H-SiC (0001) RESURF MOSFET," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 649–651, Sep. 2005.

[2] J. Spitz, M. R. Melloch, J. A. Cooper, Jr., and M. A. Capano, "2.6 kV 4H-SiC Lateral DMOSFETs," *IEEE Electron Device Lett.*, vol. 19, no. 4, pp. 100–102, Apr. 1998.

[3] W. Wang, S. Banerjee, T. P. Chow, and R. J. Gutmann, "970-V 170-m$\Omega \cdot$ cm^2 lateral two-zone RESURF MOSFETs in 4H-SiC with NO annealing," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 185–187, Apr. 2004.

[4] M. Noborio, J. Suda, and T. Kimoto, "4H-SiC lateral double RESURF MOSFETs with low on resistance," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 1216–1223, May 2007.

[5] K. Fujikawa, K. Shibata, T. Masuda, S. Shikata, and H. Hayashi, "800 V 4H-SiC RESURF-type lateral JFETs," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 790–791, Dec. 2004.

[6] Y. Zhang, K. Sheng, M. Su, J. Zhao, P. Alexandrov, and L. Fursin, "1000-V 9.1-m$\Omega \cdot$ cm^2 normally off 4H-SiC lateral RESURF JFET for power integrated circuit applications," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 404–407, May 2007.

[7] C. F. Huang, J. R. Kuo, and C. C. Tsai, "High voltage (3130 V) 4H-SiC lateral p-n diodes on a semiinsulating substrate," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 83–85, Jan. 2008.

[8] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1442–1447, Jul. 2001.

[9] N. Sghaier, J. M. Bluet, A. Souifi, G. Guillot, E. Morvan, and C. Brylinski, "Study of trapping phenomenon in 4H-SiC MESFETs: Dependence on substrate purity," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 297–302, Feb. 2003.

[10] H. Cha, C. I. Thomas, G. Koley, L. F. Eastman, and M. G. Spencer, "Reduced trapping effects and improved electrical performance in buried-gate 4H-SiC MESFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1569–1574, Jul. 2003.

[11] F. Villard, J.-P. Prigent, E. Morvan, C. Dua, C. Brylinski, F. Temcamani, and P. Pouvil, "Trap-free process and thermal limitations on large-periphery SiC MESFET for RF and microwave power," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1129–1134, Apr. 2003.